

Fig. 4. Forward voltage drop distribution of GTO segments, measured under current of 0.8 A.

radiation intensity versus current dependence as correct. This relation only can be infringed upon by the above mentioned decrease of spatial resolution and dispersion of a pixel's charge to neighboring ones. To avoid these problems, a linear CCD structure should be useful.

According to the observed dependence of the radiation intensity on the forward voltage drop, the segments with lower radiation intensity have a lower forward current and a higher voltage drop. If we assume that elements with the lowest forward current are the first to turn off, the turn-off failure region for the case of an increasing anode current or repetition rate applied to the GTO can be predicted. This way, the influence of static parameter nonuniformity on local turn-off overloading can be investigated.

Although the sample was intentionally chosen with a high non-uniformity degree, in the case of a large-current GTO, when it seems difficult to prevent nonuniformity of the on-state voltage of unit GTO's [3], our approach can assist in researching current redistribution effects.

Our method was verified on many samples and can serve as a tool for instant integral information about GTO in a routine manner. Under GTO manufacturing conditions, image digitization is not necessary because data acquisition via photosignal discrimination together with direct TV imaging is efficient for the localization of technological imperfections.

IV. CONCLUSIONS

The method described in this brief can significantly simplify and speed up the basic diagnostic of a high-power GTO under a state closely approximating that of actual operation.

Unpretentious changes make possible valuable applications to other prospective high-power devices with highly interdigitated structures and/or during the development of large-current devices.

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Hot-Carrier Degradation in Bipolar Transistors at 300 and 110 K—Effect on BiCMOS Inverter Performance

J. DAVID BURNETT AND CHENMING HU

Abstract—The degradation of bipolar transistors at 300 and 110 K under dc base-emitter reverse-bias stress has been measured. It is found that, for the same reverse voltage, the reverse current is about three to four times smaller at 110 than at 300 K, but the rate of base current degradation is several times larger. A method for modeling the degradation due to the stress from a periodic signal is proposed. The resulting expression for degradation is compatible with the SPICE bipolar model and has been used to simulate the degradation of a BiCMOS inverter operating at 300 and 110 K.

I. INTRODUCTION

BiCMOS circuits are receiving widespread attention because they offer the high-speed capability of bipolar circuits together with the low power dissipation and high density of CMOS circuits. The most recent advances in BiCMOS technologies have resulted in the combination of high-performance bipolar and CMOS transistors [1], [2]. Because the operation of CMOS circuits at liquid-nitrogen temperature (LN) offers many advantages over room-temperature (RT) operation [3], [4] and because high-gain LN bipolar transistors have been recently demonstrated [5], [6], BiCMOS performance at LN may improve over the RT performance.

One concern with the operation of BiCMOS circuits is the reverse biasing of the emitter-base junction of the bipolar transistors that interface with the CMOS gates [7]. The reverse-bias stress causes hot-carrier damage around the emitter edge which increases the base-emitter recombination current and thus degrades the current gain [7]–[9]. With the possibility of operating BiCMOS circuits at low temperatures, it is important to investigate the degradation of bipolar devices at low temperature. This brief examines and models the degradation of self-aligned polysilicon-emitter bipolar transistors at 300 and 110 K. The implications of the degradation upon BiCMOS operation at 300 and 110 K are considered by simulating the increase in propagation delay of a BiCMOS inverter with increased time of operation.

II. REVERSE-BIASED EMITTER-BASE CHARACTERISTICS

n-p-n transistors were fabricated using a single-level polysilicon, self-aligned process [9]. A device cross section is shown in the inset of Fig. 1. The dose used for the extrinsic base is 2×10^{14} cm^{-2} , which is typical of the link-base dosage for high-performance digital devices [10]. The devices under consideration in this work have an emitter area of $1.2 \mu\text{m} \times 3.2 \mu\text{m}$.

Fig. 1 shows the reverse I - V characteristics at 300 and 110 K. The large current at the lower voltages can be associated with a tunneling current due to the large electric field along the periphery [8], [9]. The emitter-base junction breaks down at approximately 5.4 V with the sudden increase in current being due to a large increase in avalanche multiplication. By using the expression for the band-to-band tunneling current [11] in conjunction with the expression for avalanche multiplication [11], [12], the measured reverse

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The authors are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720.
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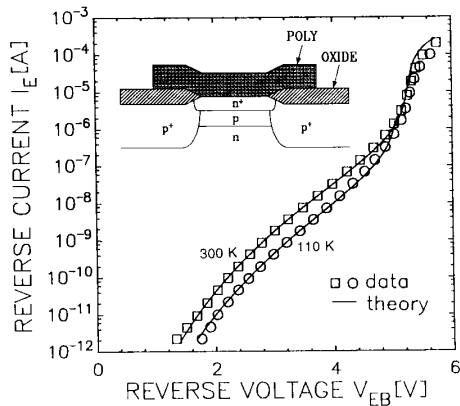


Fig. 1. Reverse characteristics for the emitter-base junction at 300 and 110 K. The symbols represent the measured data while the solid lines result from combining analytical expressions for band-to-band tunneling and avalanche multiplication.

I - V characteristic can be modeled accurately as shown in Fig. 1. For the same reverse voltage, prior to significant avalanche multiplication, the current at 110 K is about three to four times lower than the 300 K value. This decrease results from the increase in bandgap energy at 110 K, which causes a decrease in the tunneling probability.

III. BIPOLAR TRANSISTOR DEGRADATION

An effective monitor for the degradation is the change in the forward base current ΔI_B measured at a given collector current density J_C [8], [9]. The constant-current stress degradation of I_B for 300 and 110 K is shown in Fig. 2. It should be noted that the device measurements after stress are performed at the same temperature as the stress. The rate of degradation, measured at $J_C = 0.1 \mu\text{A}/\mu\text{m}^2$, is about four times larger at 110 than at 300 K for the same reverse-stress voltage and about ten times larger for the same reverse-stress current. The increase in ΔI_B and the rate of degradation at 110 K is consistent with the increased severity of hot-carrier damage in MOSFET's at low temperatures [3], [13].

The degradation can be modeled as [9]

$$\Delta I_B = DJ_C^a I_R^b t^c \quad (1)$$

where J_C is the collector current density in amperes per square micrometers, I_R is the reverse-stress current, t is the stress time, and $a = 0.578$, $b = 0.9$, $c = 0.5$, and $D = 0.875$ for 300 K and $a = 0.361$, $b = 0.92$, $c = 0.58$, and $D = 0.249$ for 110 K. The physical interpretations of a , b , and c were discussed in [9]. With (1), the degradation can be characterized over a range of I_R and J_C . The good agreement between the measured and calculated values of current gain variation with stress time is illustrated in Fig. 3 for the 300 and 110 K stresses.

IV. BiCMOS INVERTER DEGRADATION

In order to determine the impact of bipolar transistor degradation upon BiCMOS circuit performance, a typical BiCMOS inverter, as shown in the inset of Fig. 4, was simulated. The values for I_S , I_{KF} , and β_F at 300 and 110 K were extracted from the devices prior to stressing. The CMOS devices had $L_{\text{eff}} = 0.7 \mu\text{m}$ and $t_{\text{ox}} = 157 \text{ \AA}$. For the n-channel devices, $W/L = 3 \mu\text{m}/0.7 \mu\text{m}$, while for the p-channel devices, $W/L = 6.6 \mu\text{m}/0.7 \mu\text{m}$. For the 110 K simulations, the parasitic resistances and capacitances of the bipolar and CMOS devices were unchanged from their 300 K values, while the mobility of the CMOS devices was assumed to increase by 50% for the n-channel device and 25% for the p-channel device [3].

The base-emitter junction of Q1 can become reverse biased when the output undergoes a high-to-low transition. The emitter-base

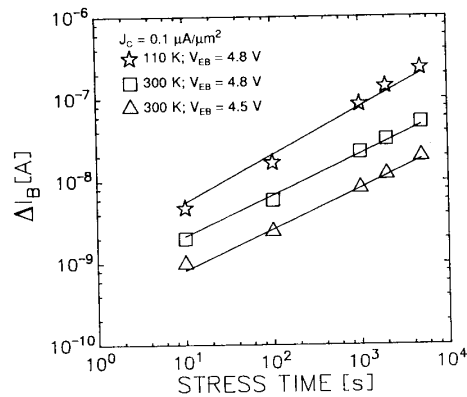


Fig. 2. Degradation of I_B , ΔI_B , for different stress conditions. The reverse-stress current was the same for the 110 K, $V_{EB} = 4.8 \text{ V}$ and the 300-K, $V_{EB} = 4.5 \text{ V}$ stresses. ΔI_B at 110 K is about four times greater than the 300 K value for the same reverse voltage stress and about ten times greater for the same reverse-stress current.

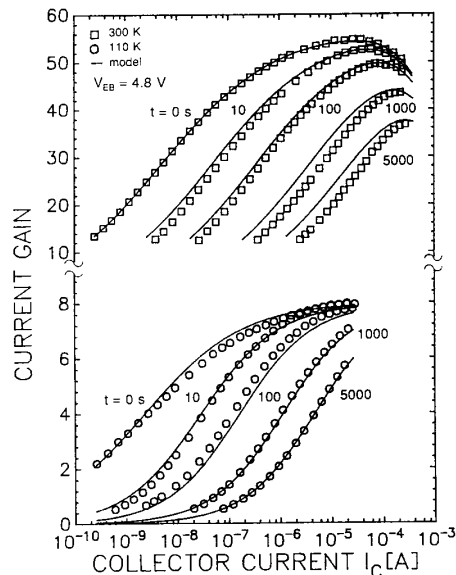


Fig. 3. The β - I_C characteristics show the degradation of β at 300 and 110 K with constant current stress. The upper curve of each set corresponds to the device before stress with each successive curve beneath it corresponding to increasing intervals of stress time. The solid lines result from (1) with $a = 0.578$, $b = 0.9$, $c = 0.5$, and $D = 0.875$ for the 300 K data and with $a = 0.361$, $b = 0.92$, $c = 0.58$, and $D = 0.249$ for the 110 K data.

reverse current of Q1 was calculated for a cycle of operation at 100 MHz by monitoring the emitter-base voltage of Q1 of a cycle and using a typical reverse I - V characteristic. Fig. 4 shows the simulated emitter-base reverse voltage and current of Q1 at 300 and 110 K for a worst case V_{CC} of 5.5 V. The reverse-stress current at 110 K is seen to be almost an order of magnitude smaller than the 300 K current. This decrease results primarily from the decrease in reverse current at 110 from 300 K for a given reverse voltage. Also, the output voltage swing at 110 K is reduced because the built-in voltage is larger; hence, the maximum reverse voltage across the base-emitter junction of Q1 is decreased.

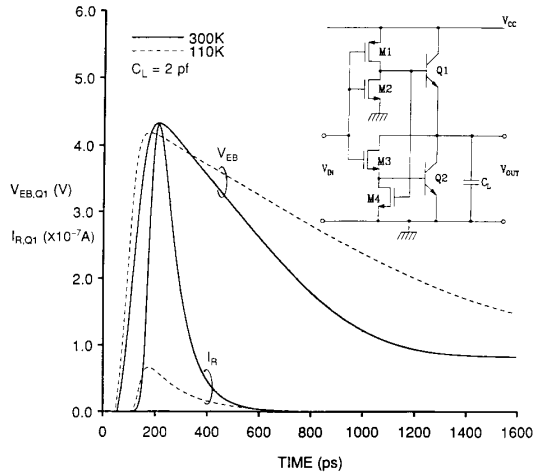


Fig. 4. The simulated transient reverse voltage and current of the emitter-base junction of Q1 at 300 and 110 K with $C_L = 2$ pF and $V_{CC} = 5.5$ V. The inset shows the BiCMOS inverter circuit used in the simulations. For the bipolar transistors, the simulations used $\beta_F = 60$ and $I_{KF} = 2$ mA at 300 K and $\beta_F = 8$ and $I_{KF} = 2$ mA at 110 K. For the MOS devices, $W_n/L_n = 3/0.7$ and $W_p/L_p = 6.6/0.7$.

The degradation from a time-varying I_R is determined using a quasi-static form of (1). The time derivative of (1) yields

$$\frac{d\Delta I_B}{dt} = cDJ_C^a I_R^b t^{c-1} = c(DJ_C^a I_R^b)^{1/c} \Delta I_B^{(c-1)/c}. \quad (2)$$

After the variables ΔI_B and t are separated onto different sides, (2) is integrated to give

$$\int \frac{d\Delta I_B}{c\Delta I_B^{(c-1)/c}} = \Delta I_B^{1/c} = D^{1/c} J_C^a \int I_R^{b/c}(t) dt. \quad (3)$$

Using $J_C = (I_S/A_E) e^{V_{BE}/V_i}$, ΔI_B is expressed in a form that can be implemented into the SPICE Gummel-Poon (GP) model

$$\Delta I_B = D(I_S/A_E)^a e^{aV_{BE}/V_i} \cdot \left[(\# \text{ of cycles}) \int_{1 \text{ cycle}} I_R^{b/c}(t) dt \right]^c. \quad (4)$$

Equation (4) assumes that the reverse current, as shown in Fig. 4, is the same for each cycle. By incorporating (4) into the nonideal base current term of the GP model, we simulated the increase in the low-to-high propagation delay (t_{PLH}) resulting from the ΔI_B degradation. The results of Fig. 5 show that after 10 years of operation with $C_L = 2$ pF, t_{PLH} degrades by about 7% from 440 ps (while the peak value of β degrades by 70% from 60) at 300 K and by about 3% from 680 ps (while the peak value of β degrades by 13% from 8) at 110 K. The improvement in the t_{PLH} percentage degradation at 110 K over 300 K is not unexpected since the sensitivity of t_{PLH} on ΔI_B is reduced due to the much smaller β_F at 110 K. Furthermore, t_{PLH} degrades less for $C_L = 1$ pF than 2 pF because smaller values of C_L reduce the degradation signal that occurs each cycle. For a given C_L , the degradation signal can be reduced by increasing the area of Q2 and the W of M3, thereby pulling down the emitter of Q1 faster, and by decreasing the W of M2, thereby increasing the pull-down time of the base of Q1.

V. SUMMARY

Although the reverse current is smaller at 110 than at 300 K for the same reverse voltage, the rate of base current degradation is several times larger. The impact of the base current degradation upon BiCMOS inverter circuit performance was simulated using a

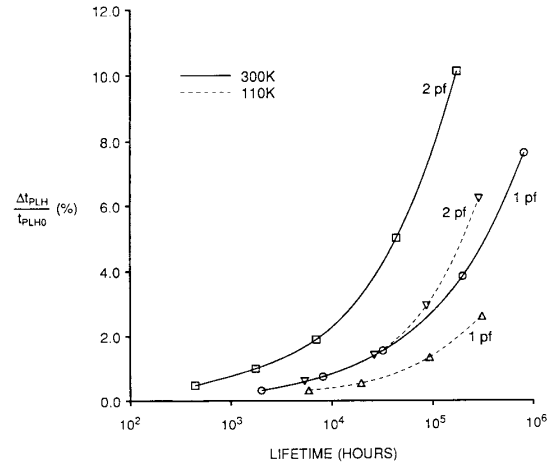


Fig. 5. The simulated degradation of t_{PLH} with increasing time of operation for a BiCMOS inverter at 100 MHz. The simulated values for t_{PLH} prior to degradation are: at 300 K, 290 ps for $C_L = 1$ pF and 440 ps for $C_L = 2$ pF; at 110 K, 404 ps for $C_L = 1$ pF and 680 ps for $C_L = 2$ pF.

quasi-static model for the degradation of the base current due to a periodic time-varying stress. The simulation of an advanced BiCMOS process, which has self-aligned polysilicon-emitter bipolar transistors, indicates a degradation in the low-to-high propagation delay of 7% at 300 K and 3% at 110 K after 10 years of operation with $C_L = 2$ pF and $V_{CC} = 5.5$ V.

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