

HOT-CARRIER RELIABILITY OF BIPOLAR TRANSISTORS

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ABSTRACT

Bipolar degradation is due to an excess forward base current, $\Delta I_B = DJ_C^a I_R^{0.9} t^{0.5}$, where $a = 1/n_E$. This relationship is perfectly consistent with CMOS hot-electron degradation models except for a non-local high-field-effect correction. This model is incorporated into a circuit reliability simulator and used to simulate the performance degradation of a BiCMOS inverter and a differential pair.

I. INTRODUCTION

One concern for the reliability of bipolar transistors is the reverse bias of the emitter-base junction which can result in the degradation of the current gain [1-6]. This undesirable condition occurs frequently in circuits when bipolar and CMOS transistors interface, e.g., BiCMOS gates, and when analog inputs feed into bipolar devices, e.g., the input comparator of flash analog-to-digital converters (ADCs) or the input of operational amplifiers (op amps). One component in improving the performance of bipolar transistors is the reduction of the extrinsic base resistance, which is often achieved by the increased doping of the extrinsic base region and through the self-alignment of the heavily-doped emitter and extrinsic base regions. These modifications result in a very large electric field and a significant reverse current at the emitter-base junction. This is an undesirable combination under reverse bias because the large electric field can create hot carriers that degrade the oxide around the emitter edge, causing an increase in the forward base recombination current. The result is a decrease in the current gain which, in turn, can limit the performance of the bipolar circuit. Fig. 1 shows the degradation of the β - I_C characteristic due to constant current stress. In this paper, we present a study of bipolar degradation over a range of stress and measurement conditions. The implications of the degradation upon circuit operation are considered by simulating the increase in propagation delay of a BiCMOS inverter and the shift in offset voltage of an emitter-coupled pair.

The npn transistors used in this study were fabricated using a self-aligned, polysilicon-emitter process [4]. The device cross-section is shown in the inset of Fig. 2. The self-alignment of the emitter and extrinsic base is achieved by using a thin oxide-nitride stack to define the intrinsic area while blocking the extrinsic-base implant. The dose used for the extrinsic base is $2 \times 10^{14} \text{ cm}^{-2}$, which is typical of the link-base dosage for high-performance digital devices [7]. Fig. 2 shows the reverse I-V characteristics at 300 K and 110 K. The large current at the lower voltages can be associated with a tunneling current due to the large electric field along the periphery [3-5]. The emitter-base junction breaks down at approximately 5.4 V with the sudden increase in current being due to a large increase in avalanche

multiplication. For the same reverse voltage, prior to significant avalanche multiplication, the current at 110 K is about three-to-four times lower than the 300 K value. This decrease results from the increase in bandgap energy at 110 K, which causes a decrease in the tunneling probability.

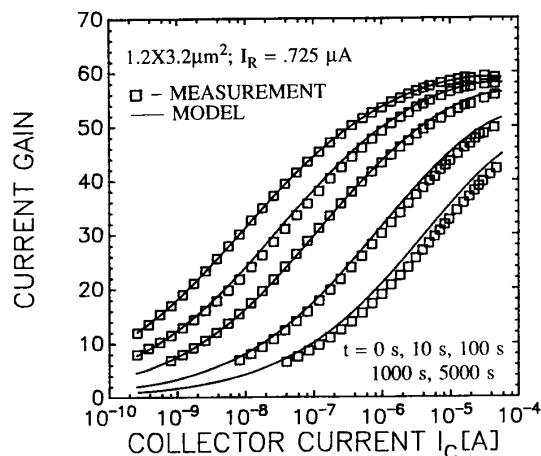


Fig. 1. Degradation of β - I_C characteristic with dc stress. The solid lines are calculated using the ΔI_B model.

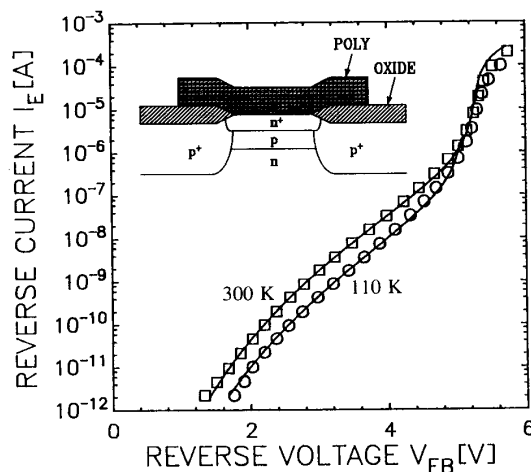


Fig. 2. Reverse emitter-base characteristics at 300K and 110K.

II. CONSTANT-STRESS DEGRADATION

Because the damage from the reverse bias creates an excess base current, the change in forward base current, ΔI_B , is an effective monitor for the degradation. From the dynamics of bipolar device degradation [4]

$$\Delta I_B \propto f(t I_R e^{-\phi_T/kT_E}) \quad (1)$$

where $f(x) \approx x^{0.5}$, ϕ_T is the critical energy for device damage, 3.7 eV [8], t is the stress time, I_R is the reverse-stress current, and T_E is the maximum electron temperature. Fig. 3 shows this power-law dependence on accumulated stress time for different values of dc-stress bias.

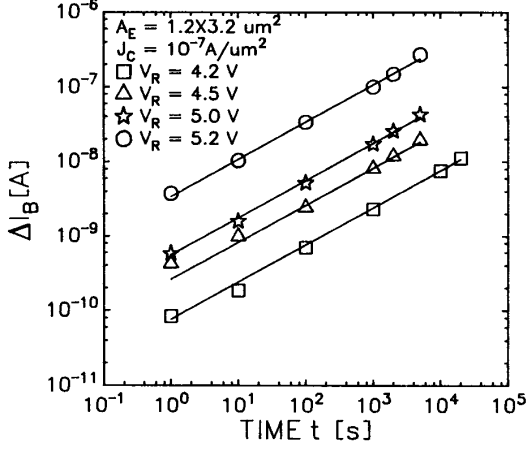


Fig. 3. Degradation of I_B , ΔI_B , for different dc-stress biases.

In the heavily-doped emitter-extrinsic-base junction, the band-to-band tunneling current is given as [9]

$$I_R \propto E_M V_R \exp(-B/E_M) \quad (2)$$

where E_M is the peak electric field and V_R is the applied voltage. Measured data yields an experimental value of $B = 18$ MV/cm [10]. By neglecting the pre-exponential dependence of I_R on E_M and V_R , $I_R \propto \exp(-B/E_M)$, which conveniently allows (1) to be expressed as

$$\Delta I_B \propto \left[t I_R^d e^{\phi_T E_M/kBT_E} \right]^{0.5} = (t I_R^d)^{0.5} \quad (3)$$

where $d = 1 + \phi_T E_M/kBT_E$. A general expression for T_E due to a one-dimensional electric field, $E(x)$, has been derived from the energy conservation equation [11,12] as

$$\frac{dT_E(x)}{dx} + \frac{2T_E(x)}{5\lambda} = \frac{2qE(x)}{5k} \quad (4)$$

having defined λ as a hot-electron mean free path. Good agreement between experimental MOSFET I_C and this model have been obtained using $\lambda = 6.4$ nm [12]. When $E(x)$ remains constant over several λ , $T_E(x) = (q/k)\lambda E(x)$; however, when a large gradient in $E(x)$ exists, the peak T_E can be significantly less than $(q/k)\lambda E_M$. According to the local T_E model, i.e. $T_E = (q/k)\lambda E_M$, $d = 1 + \phi_T/q\lambda B = 1.3$. However, as observed from the ΔI_B data of Fig. 4, $d = 1.8$. The data in Fig. 4 represent a two decade range of I_R , and similar behavior was observed for other emitter sizes and different technologies.

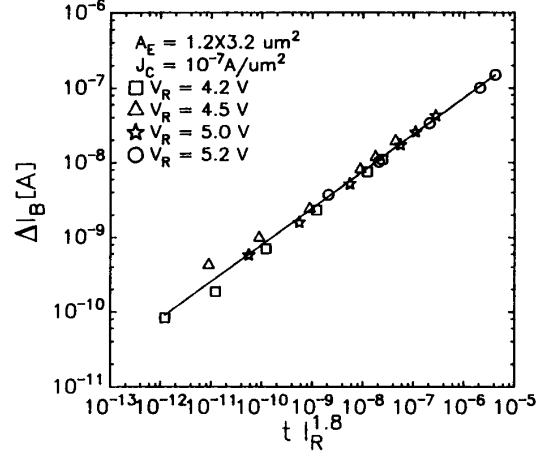


Fig. 4. ΔI_B data of Fig. 3 replotted to indicate that $\Delta I_B \propto (I_R^{1.8} t)^{0.5}$.

The observed d can be explained by using a non-local electron temperature model. As illustrated in Fig. 5, the tunneling portion of the reverse I-V characteristic can be fit using (2) for a linearly graded junction with a doping gradient of 6×10^{24} cm⁻⁴. The solid line in Fig. 6 shows the electric field of the same junction with $V_R = 4$ V. The highest probability for tunneling occurs near the maximum electric field. By solving (4) for electrons emerging from tunneling, $T_E(x)$ can be derived in a simple, closed-form expression and is shown by the dashed line in Fig. 6. The maximum value of kT_E/qE_M is found to be 0.39λ , which yields $d = 1 + \phi_T/0.39q\lambda B = 1.8$ in excellent agreement with the experimental results. This is the most dramatic example of the non-local effect ever observed because the high-field-region width involved is many times smaller than in MOSFETs. An excellent fit to the reverse current characteristic, as shown in Fig. 5, results by using E_M to calculate the band-to-band tunneling

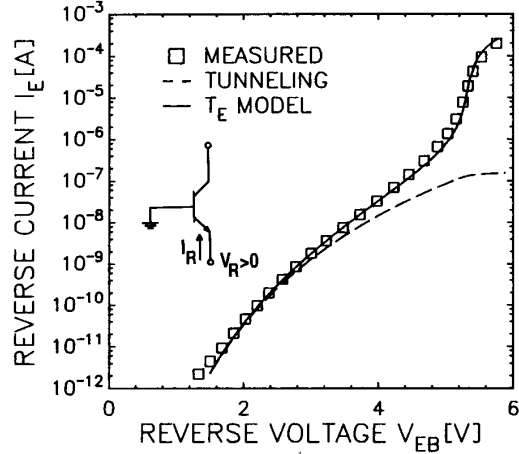


Fig. 5. Reverse emitter-base characteristics. The excellent fit to the experimental data results by using band-to-band tunneling along with avalanche multiplication based on non-local effects.

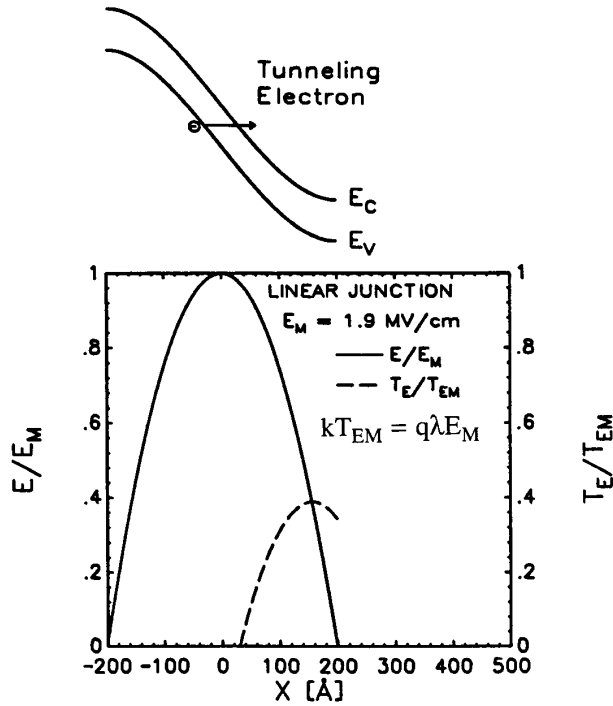


Fig. 6. Representation of the tunneling electrons, electric field, and electron temperature along the extrinsic-base-emitter junction by using a linear junction with $a = 6 \times 10^{24} \text{ cm}^{-4}$ and $V_R = 4 \text{ V}$. T_{EM} is the maximum T_E without non-local effects, $T_{EM} = qE_M\lambda/k$.

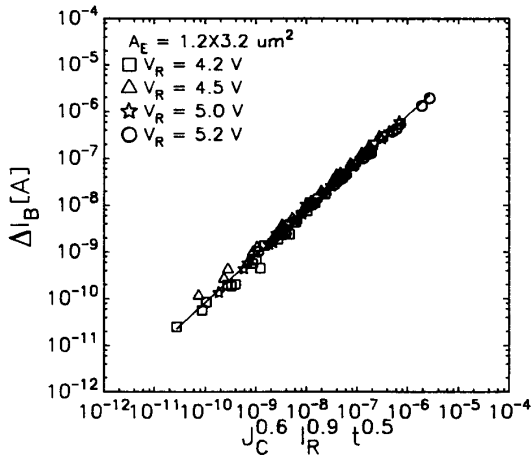


Fig. 7. ΔI_B data over a range of J_C , I_R , and t plotted to indicate that $\Delta I_B = DJ_C^{0.6} I_R^{0.9} t^{0.5}$. $D = 1.2$ with J_C in $\text{A}/\mu\text{m}^2$.

current, given by (2), and then using the peak value of T_E from (4) to calculate the avalanche multiplication factor.

By measuring ΔI_B at different values of collector current density, J_C , ΔI_B is found to follow a power-law dependence on J_C as $\Delta I_B \propto J_C^a$, where $a = 0.6$. J_C^a provides the exponential dependence of the non-ideal base current on V_{BE} , $J_C^a \propto e^{V_{BE}/n_E V_T}$, where the non-ideality factor, $n_E = 1/a$, is 1.7 in these devices. With the variables of t , I_R , and J_C , ΔI_B can be modeled as $\Delta I_B = DJ_C^{0.6} I_R^{0.9} t^{0.5}$, as illustrated in Fig. 7. The solid lines in Fig. 1 show that the inclusion of the ΔI_B model in the current gain calculation provides good agreement with the measured current gain degradation.

III. EFFECT OF TEMPERATURE AND INTERFACIAL LAYER

The degradation of I_B for constant-current stress at 300 K and 110 K is shown in Fig. 8. (The device measurements after stress are performed at the same temperature as the stress.) The rate of degradation, measured at $J_C = 0.1 \mu\text{A}/\mu\text{m}^2$, is about four times larger at 110 K than at 300 K for the same reverse-stress voltage and about ten times larger for the same reverse-stress current. The increase in ΔI_B and the rate of degradation at 110 K is consistent with the increased severity of hot-carrier damage in MOSFETs at low temperatures [13,14]. Our results indicate that the functional dependence of ΔI_B is valid down to 110 K. Fig. 9 shows the agreement between the modeled and experimental β degradation at 110 K.

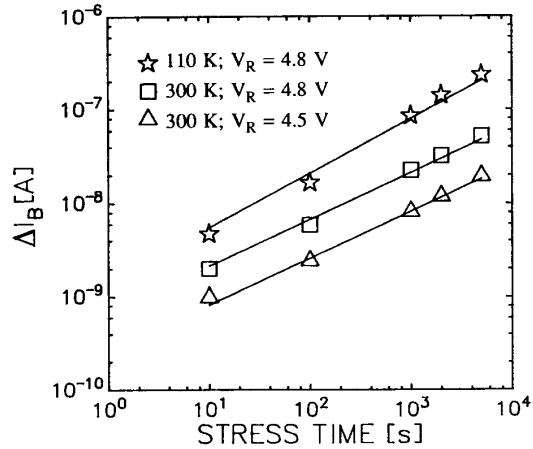


Fig. 8. ΔI_B measured at $J_C = 0.1 \mu\text{A}/\mu\text{m}^2$ for different stress conditions. The reverse-stress current was the same for the 110K, $V_{EB} = 4.8 \text{ V}$ and the 300K, $V_{EB} = 4.5 \text{ V}$ stresses.

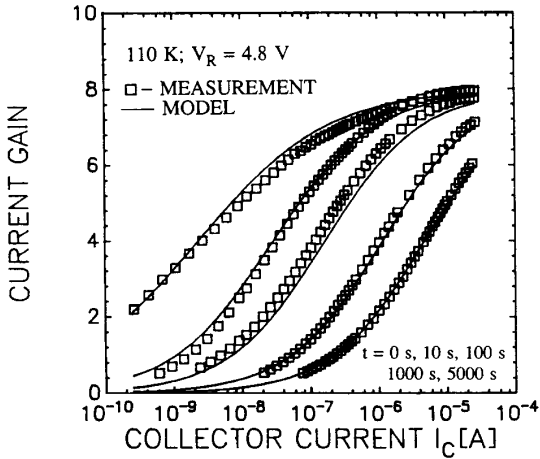


Fig. 9. Degradation of the β - I_C characteristic at 110 K. The functional form of the ΔI_B model remains valid with $D = 0.25$, $a = 0.36$, $b = 0.92$, and $c = 0.58$ used to provide the fit shown.

The base current in polysilicon-emitter devices depends substantially upon the interface between the polysilicon and silicon substrate. To explore the reliability of devices with different interfacial layers, we have fabricated wafers with intentional interfacial layers. The wafers received the same processing as those previously described except at the step prior to polysilicon deposition. At this time the wafers first had a thin ($\approx 15 \text{ \AA}$) rapid thermal oxide (RTO) grown on the silicon surface. Some wafers then received a short nitridation in an ammonia ambient (RTO/RTN). After this step, polysilicon was deposited. As seen in Fig. 10, the devices with an intentional interface exhibited a much greater peak β . This is expected because the interfacial

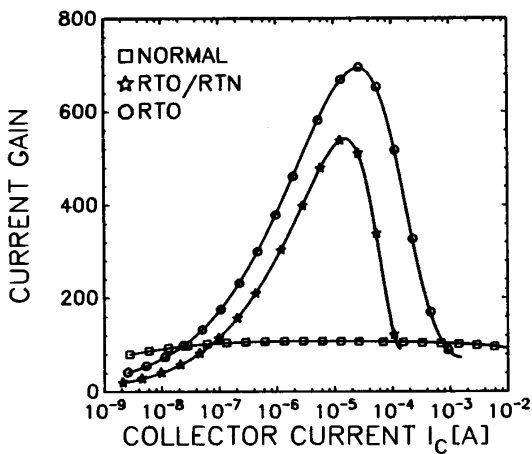


Fig. 10. β - I_C characteristics for devices with different interfaces between the poly-emitter and monocrystalline-silicon. ($A_E = 20 \times 20 \mu\text{m}^2$.)

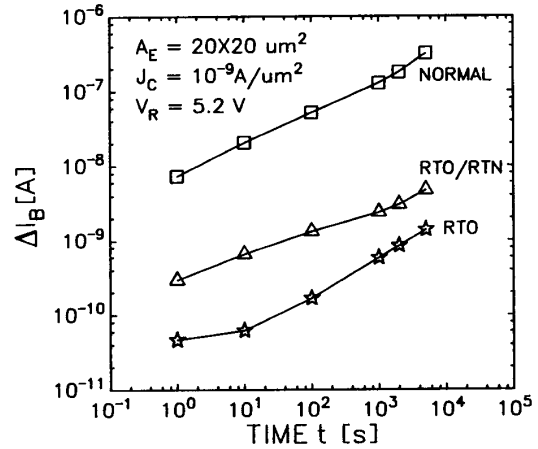


Fig. 11. ΔI_B for the devices with different interfaces. The RTO and RTO/RTN devices show much less degradation for the same stress voltage than the devices without an intentional interface.

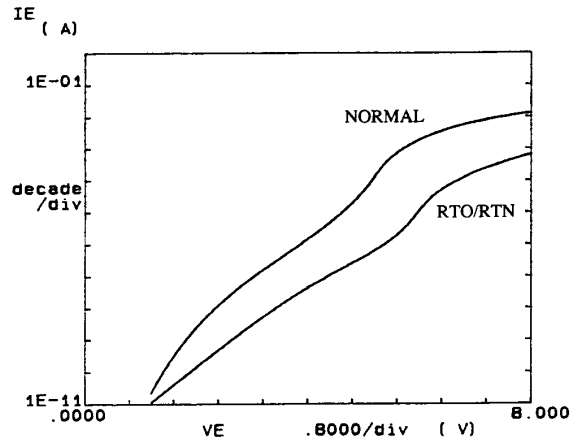


Fig. 12. Reverse I-V characteristics for the normal and RTO/RTN devices. (The RTO's reverse characteristic is very similar to that of the RTO/RTN device.)

layer impedes the flow of the holes from the base to the emitter. Fig. 11 shows the ΔI_B characteristics for the different wafers for a reverse-bias of 5.2 V. The RTO interface results in ΔI_B degradation two orders of magnitude less than a clean interface, while the RTO/RTN interface is over an order of magnitude less. This improvement in ΔI_B can be explained by considering the reverse I-V characteristic shown in Fig. 12. At a given reverse voltage, the RTO/RTN (and RTO) devices have a much smaller reverse current than the normal devices, and therefore less damage is produced.

IV. CIRCUIT RELIABILITY SIMULATION

In order to determine the impact of the hot-carrier degradation upon circuit performance, an expression for the degradation due to time-varying stress signals has been developed. From the dc-stress equation, $\Delta I_B = D J_C^a I_R^b t^c$, a quasi-static expression for ΔI_B due to a time-varying I_R is [15]

$$\Delta I_B = D (I_S/A_E)^a e^{aV_{BE}/V_T} \left[(\# \text{ of cycles}) \cdot \int_{1 \text{ cycle}} I_R^{b/c}(t) dt \right]^c \quad (5)$$

by using $J_C = (I_S/A_E)e^{V_{BE}/V_T}$ and by assuming that the reverse current is the same for each cycle. (5) is compatible with the non-ideal base current term of the SPICE Gummel-Poon model and can therefore be used to simulate the effect of the degradation on circuit performance.

In order to determine the impact of the bipolar transistor degradation upon BiCMOS circuit performance, a typical BiCMOS inverter, as shown in the inset of Fig. 13, was simulated [15]. The base-emitter junction of Q1 can become reverse biased when the output undergoes a high-to-low transition. The emitter-base reverse current of Q1 was calculated for a cycle of operation at 100 MHz by monitoring the emitter-base voltage of Q1 of a cycle and using a typical reverse I-V characteristic. Fig. 13 shows the simulated emitter-base reverse voltage and current of Q1 at 300 K and 110 K for a worst-case V_{CC} of 5.5 V. The reverse-stress current at 110 K is seen to be almost an order of magnitude smaller than the 300 K current. This decrease results primarily from the decrease in reverse current at 110 K from 300 K for a given reverse voltage. Also, the output voltage swing at 110 K is reduced because the built-in voltage is larger; hence, the maximum reverse voltage across the base-emitter junction of Q1 is decreased.

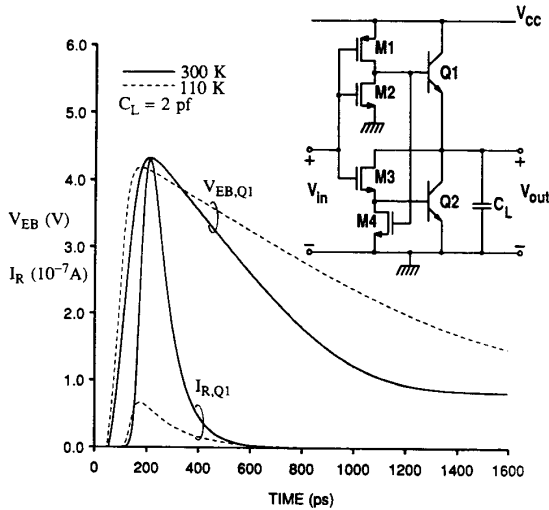


Fig. 13. Simulated transient reverse voltage and current of the emitter-base junction of Q1 at 300K and 110K with $C_L = 2$ pf and $V_{CC} = 5.5$ V.

By incorporating (5) into the non-ideal base current term of the GP model, we simulated the increase in the low-to-high propagation delay (t_{PLH}) resulting from the ΔI_B degradation. The results of Fig. 14 show that after 10 years of operation with $C_L = 2$ pf, t_{PLH} degrades by about 7% from 440 ps (while the peak value of β degrades by 70% from 60) at 300 K and by about 3% from 680 ps (while the peak value of β degrades by 13% from 8) at 110 K. The improvement in the t_{PLH} percentage degradation at 110 K over 300 K is not unexpected since the sensitivity of t_{PLH} on ΔI_B is reduced due to the much smaller β_F at 110 K. Furthermore, t_{PLH} degrades less for $C_L = 1$ pf than 2 pf because smaller values of C_L reduce the degradation signal that occurs each cycle.

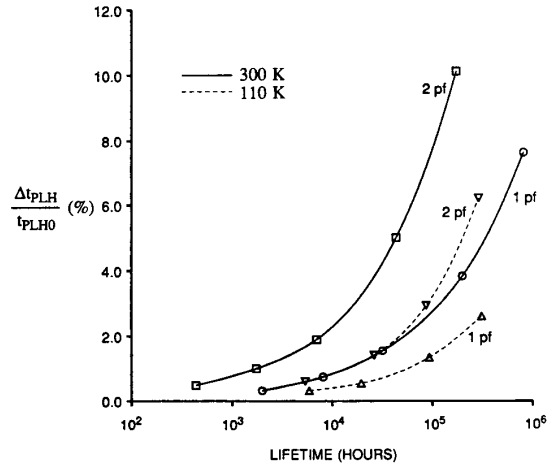


Fig. 14. Simulated degradation of t_{PLH} with increasing time of operation for a BiCMOS inverter at 100 MHz.

Another circuit subject to reverse stress signals is the differential pair of the input comparator in flash ADCs. A typical emitter-coupled pair circuit is shown in Fig. 15a. For flash ADCs to operate properly, it is imperative that the linear region of the differential pair exhibit very little offset. An offset voltage can occur due to reverse-bias stress if the voltage drop across the base resistance (internal and external) from ΔI_B becomes comparable to V_T . This is illustrated in Fig. 15b for a stress of 4.6 V applied to Q1 and with $R_B \approx 200 \Omega$. The amount of offset can be reduced by either reducing the stress signal or by reducing J_C , which corresponded to $V_{BE} = 0.8$ V in the simulation. The reverse stress also creates an additional offset in the input current which is very undesirable in circuits, such as op amps, where low input offset currents are desired.

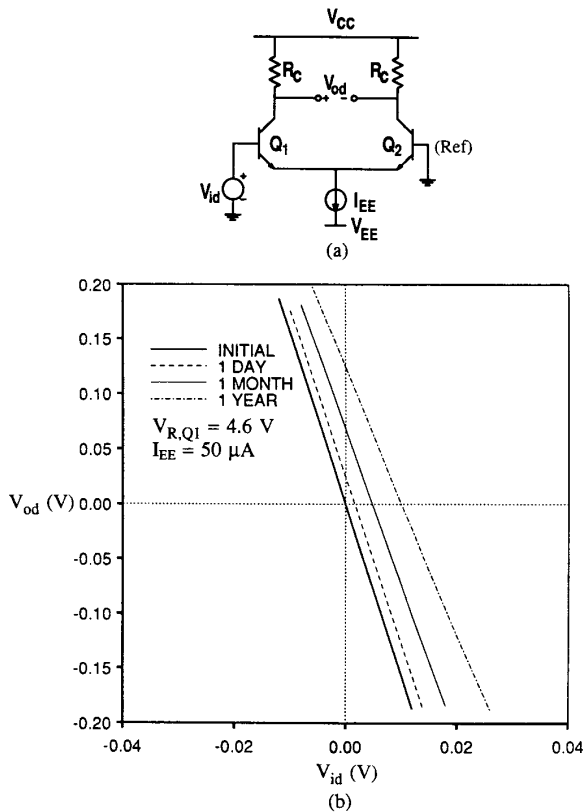


Fig. 15. (a) Emitter-coupled pair circuit. (b) Simulated degradation of the output characteristics of the emitter-coupled pair.

V. SUMMARY

In this study, we show that the excess base current, ΔI_B , varies in a power-law manner with J_C , I_R , and t . The I_R dependence results from a significant non-local effect in electron temperature that occurs at the periphery of the emitter due to the narrow depletion width. A quasi-static model of the degradation, suitable for SPICE circuit simulation, is presented and used to simulate the degradation of a BiCMOS inverter and differential pair circuit. The simulation of an advanced BiCMOS process indicates a degradation in the low-to-high propagation delay of 7% at 300 K and 3% at 110 K after 10 years of operation with $C_L = 2$ pf and $V_{CC} = 5.5$ V. For emitter-coupled pair circuits, the base current degradation can create a voltage drop across the base resistance resulting in an additional offset voltage component.

With the modeling methodology presented here, one can predict the effect of varying the emitter-extrinsic-base junction doping profile on circuit reliability. First, one would simulate E_M versus V_{BE} . From this result, $T_E(V_{BE})$ and $I_R(V_{BE})$ are calculated and the circuit degradation simulated.

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REFERENCES

- [1] S.P. Joshi, R. Lahri, and C. Lage, "Poly emitter bipolar hot carrier effects in an advanced BiCMOS technology," in *IEDM Tech. Dig.*, 1987, p. 182.
- [2] D.D. Tang and E. Hackbarth, "Junction degradation in bipolar transistors and the reliability imposed constraints to scaling and design," *IEEE Trans. Electron Devices*, ED-35, no. 12, p. 2101, 1988.
- [3] E. Hackbarth and D.D. Tang, "Inherent and stress-induced leakage in heavily doped silicon junctions," *IEEE Trans. Electron Devices*, ED-35, no. 12, p. 2118, 1988.
- [4] J.D. Burnett and C. Hu, "Modeling hot-carrier effects in polysilicon emitter bipolar transistors," *IEEE Trans. Electron Devices*, ED-35, no.12, p. 2238, 1988.
- [5] S.P. Joshi, "Suppression of poly emitter bipolar hot carrier effects in an advanced BiCMOS technology," *Proceedings IEEE 1989 Bipolar Circuits and Technology Meeting*, 1989, p. 144.
- [6] H.S. Momose, Y. Niitsu, H. Iwai, and K. Maeguchi, "Temperature dependence of emitter-base reverse stress degradation and its mechanism analyzed by MOS structures," *Proceedings IEEE 1989 Bipolar Circuits and Technology Meeting*, 1989, p. 140.
- [7] T.-C. Chen, C.T. Chuang, G.P. Li, S. Basvaiah, D.D. Tang, M.B. Ketchen, and T.H. Ning, "An advanced bipolar transistor with self-aligned ion-implanted base and W/Poly emitter," *IEEE Trans. Electron Devices*, ED-35, no. 8, p. 1322, 1988.
- [8] C. Hu, S. Tam, F.-C. Hsu, P.K. Ko, T.Y. Chan, and K. Terri, "Hot-electron-induced MOSFET degradation--model, monitor, and improvement," *IEEE Trans. Electron Devices*, ED-32, no. 2, p. 375, 1985.
- [9] J.L. Moll, *Physics of Semiconductors*. New York: McGraw-Hill, 1964.
- [10] J. Chen, T.Y. Chan, I.C. Chen, P.K. Ko and C. Hu, "Sub-breakdown drain leakage current in MOSFET," *IEEE Electron Device Lett.*, EDL-8, no. 11, p. 515, 1987.
- [11] T. Toyabe and H. Kodera, "A theory for inter-valley transfer effect in two-valley semiconductors," *Jpn. J. Appl. Phys.*, vol. 13, p. 1404, 1974.
- [12] E. Takeda, H. Kume, T. Toyabe, and S. Asai, "Submicrometer MOSFET structure for minimizing hot-carrier generation," *IEEE Trans. Electron Devices*, ED-29, no. 4, p. 611, 1982.
- [13] M. Aoki, S. Hanamura, T. Masuhara, and K. Yano, "Performance and hot-carrier effects of small CRYO-CMOS devices," *IEEE Trans. Electron Devices*, ED-34, no. 1, p. 8, 1987.
- [14] T.-C. Ong, P.K. Ko, and C. Hu, "50-Å gate-oxide MOSFET's at 77 K," *IEEE Trans. Electron Devices*, ED-34, no. 10, p. 2129, 1987.
- [15] J.D. Burnett and C. Hu, "Hot-carrier degradation in bipolar transistors at 300K and 110K--effect on BiCMOS inverter performance," to appear in *IEEE Trans. Electron Devices*.