IC RELIABILITY SIMULATION

(Invited Paper)

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Abstract

The motivation, challenges and status of IC reliability simulation are discussed. Reliability simulator BERT is used to illustrate the physical models and approaches used to simulate the hot electron effect, oxide time-dependent breakdown, electromigration, and bipolar transistor gain degradation.

Introduction

In designing a complex circuit, designers make a large number of circuit simulations, design changes and optimizations and can predict the circuit's performance reasonably accurately before committing it to silicon. It would be unthinkable to bypass the circuit simulation and analysis and rely entirely on the testing of finished IC's to discover errors or to find out if the performance of the circuit meet specifications. Yet, this is basically the way IC reliability is treated today.

A logical Alternative is to predict circuit reliability at the circuit design stage. To achieve this goal, we must, for each failure mechanism, identify a set of parameters relevant to circuit reliability (these would be the device model parameters in the analogy of circuit performance simulations) and develop simple methods of extracting these parameters for a given process or technology usually involving accelerated DC stress tests on test structures. We must also develop computer programs to predict circuit degradation or failure from these parameters for any given circuit.

At the present time, reliability assurance relies mainly on failure detection, which occurs only at the end of a lengthy product development and qualification process. It would be highly desirable to predict the circuit reliability at the circuit design stage as we predict circuit functionality and performance today. As shown in Fig. 1, this requires reliability simulation tools whose souls are the failure mechanism models, which also defines the necessary testing (for obtaining the model parameters).

Reliability Simulators

IC scaling rapidly increases the levels of current density, electric field, and inter-device interactions. As a consequence, reliability issues such as electromigration, oxide wearout, hot-carrier effects, electrostatic discharge, latchup, and radiation effects should ideally be explicitly addressed during circuit design.[1]

A circuit reliability simulator will probably contain many models to simulate the major reliability failure mechanisms. This is analogous to process simulators, which must contain separate models for diffusion, implantation, oxidation, etc. Several reliability simulators have been reported in the literature and they all include a model for the hot electron effect.[2] Some contain additional models for other failure mechanisms.

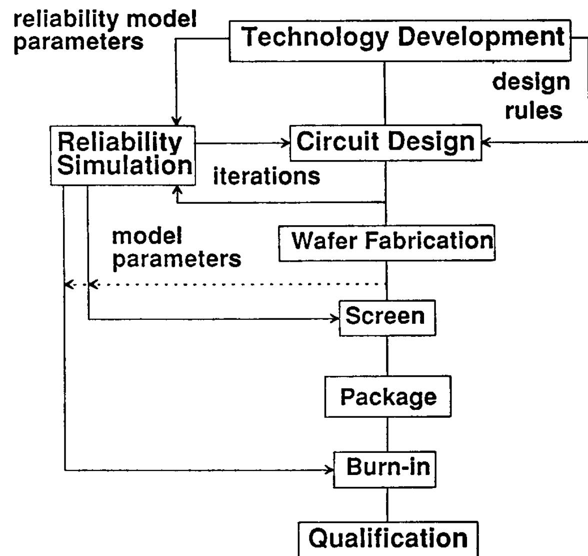

Fig. 1 A methodology of reliability assurance making greater use of information feed-forward and reliability simulation can save time and cost.

HOTRON[3] is a proprietary simulator of hot-electron effect in circuits developed at Texas Instruments, which is known to be active in developing simulators for electromigration, single-even-upset, mechanical stress, and perhaps other reliability phenomena. RELY[4] is being developed at University of Southern California. Its goal is to simulate hot electron effect, oxide reliability and electromigration, although only the results of the hot-electron effect simulations have been reported. BERT (see next section) is being developed at University of California, Berkeley. It contains the models for hot-electron effect, oxide reliability, electromigration, and bipolar transistor beta degradation. A hot-electron effect simulator is also being developed at University of Illinois[5] with special emphasis on analytical models of device degradation. A simulator of single-event and other radiation phenomena in GaAs MESFET circuits has been reported.[6]

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BERT (Berkeley Reliability Tool)

This simulator contains four modules for four reliability phenomena. They are CAS -- Circuit Aging Simulation (for hot electron effect reliability); CORS -- Circuit Oxide Reliability Simulator; EM -- Electromigration; and Bipolar Transistor Degradation. The four modules can be used together or separately to simulate IC reliability. It is anticipated that additional models will be introduced in the future.

BERT was released in March 1990. To obtain a copy of BERT, please contact Industrial Liaison Program Software Distribution Office, EECS Department, Berkeley, CA 94720, Telephone (415) 643-6687.

BERT is linked to SPICE externally in a pre- and post-processor fashion to form an independent simulator. BERT can be used with either SPICE 2 or 3 and with any of the Level 1,2,3 or BSIM MOSFET models and the bipolar transistor models.

For hot-carrier effect simulations, the fresh circuit is first simulated to determine the terminal voltage waveforms at all transistors over one cycle at any user specified power supply voltage.

The post-processor, calculates the transient substrate current and calculates the "age" of each device after any user-specified stress time. According to the "age," the simulator generates the corresponding new device parameters for each device by interpolating user-supplied process files of DC stressed transistors. Finally, the aged circuit is simulated by SPICE again.

In BERT, the "age" is taken to be $\int_0^\tau \frac{I_{ds}^{m-1}}{W I_{sub}^{m}} dt$, because the degree of device degradation hs been found to be a function of this parameter for wide ranges of channel length and stress conditions experimentally and the relationship has a plausible theoretical basis.[2] A minimum of four device parameter (process) files extracted for different stress ages must be given to the simulator. From the given process files, parameters are interpolated for all ages.

Figures 2 and 3 show the general agreement between BERT (CAS) simulations and measured ring-oscillator frequency

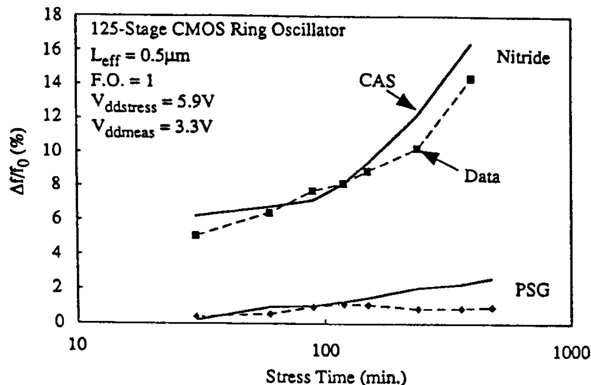

Fig. 2 Measured and BERT-CAS-simulated percentage change in frequency ($\Delta f/f_0$) versus stress time for the hot-carrier-enhanced nitride- and PSG-passivated 125-stage ring oscillator measured at $V_{dd} = 3.3V$.

decrease resulting from the hot electron effect.[7] In order to achieve significant degradation in a reasonably short test time, the test circuits were fabricated without the LDD (lightly doped drain) structure at the Motorola Advanced Products Research and Development Laboratory. Figure 2 shows the detrimental effects of a hydrogen rich Si_3N_4 passivation.

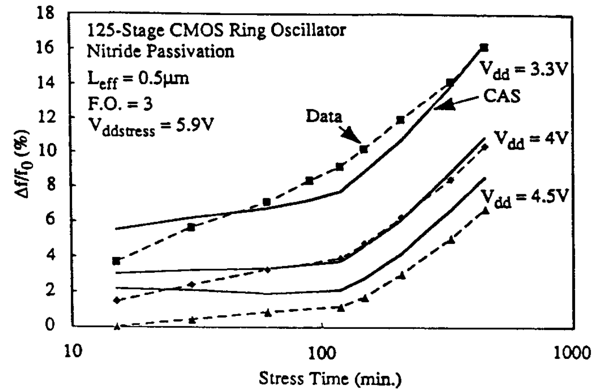

Fig. 3 Measured and BERT-CAS-simulated percentage change in frequency ($\Delta f/f_0$) versus stress time at different frequency-measuring V_{dd} values for the hot-carrier enhanced nitride-passivated oscillator. Fan-out is equal to three.

Another BERT module which generates statistics about circuit failures due to MOS oxide breakdown has been developed. The program, CORS (Circuit Oxide Reliability Simulator), predicts the probability of circuit failure as a function of operating time, temperature, power supply voltage and input waveforms.[8] CORS calculates the probability of failure by using the node voltages provided by SPICE and oxide defect statistics which are provided by the user. The effect of burn-in on oxide reliability can also be simulated.

Data indicate that the overall reliability of oxides produced by a given "technology," which includes the quality of the silicon material, the cleanliness of the fabrication environment and the gettering and oxidation conditions, etc., can be characterized by a $D(\Delta X_{ox})$ function. Every weak spot, i.e., defect point, behaves as an oxide with a thickness that is thinner than the nominal thickness by ΔX_{ox}. D is the density (in cm^2) of all defects with ΔX_{ox} larger than a given value. $D(\Delta X_{ox})$ can be determined from simple and fast voltage ramp breakdown tests.[9]

$$t_{BD} = C\, e^{G(X_{ox}-\Delta X_{ox})/V_{ox}} \quad (1)$$

$$\text{Cumulative failure} = 1 - e^{-AD(\Delta X_{ox})} \quad (2)$$

t_{BD} is the oxide breakdown lifetime, $C \approx 10^{-11}\,s$, $G \approx 350\,MV/cm$, V_{ox} is the applied oxide voltage. Equation (2) assumes Poisson defect distribution.[9]

Time dependent breakdown characteristics have been predicted rather accurately with the above model as illustrated in Ref. 9. These equations and $D(\Delta X_{ox})$ measured at wafer level

are expected to predict low voltage (to at least 5V), long term reliability as well as the optimal screen or burn-in condition. Of course, the tools can easily accept alternative t_{BD} models such as that described in [10] rather than Eq. (1). We have implemented the so-called E-model.

The CORS user creates an input deck similar to an ordinary SPICE input deck with a few additional commands which are required to provide the ramp voltage breakdown statistics or the time to breakdown statistics of test capacitors. The simulator uses this supplied data to derive the oxide defect distribution for the particular technology.

CORS determines $V_{ox}(t)$ for each oxide element in the circuit from the SPICE node voltages and a consideration of the work function difference between the electrodes. Circuit failure statistics are calculated using the rule that if any MOSFET or capacitor experiences breakdown, then the entire circuit fails. Figure 4 shows an example of the CORS simulation results.

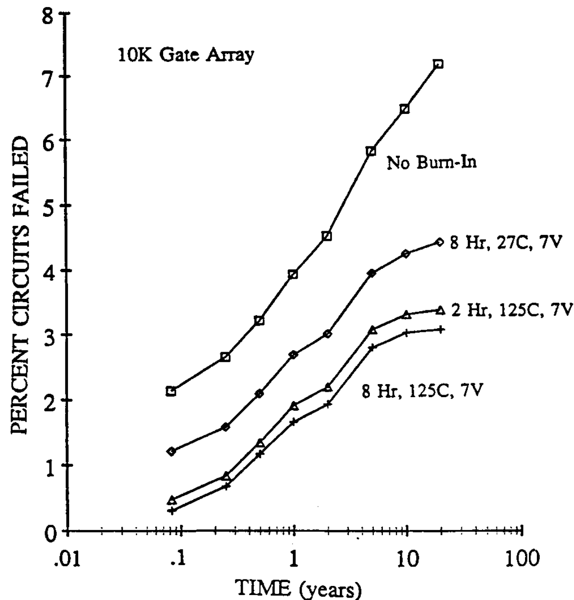

Fig. 4 BERT-CORS simulates the cumulative failure or failure rate of a circuit due to oxide breakdown, as a function of time, voltage, temperature, and burn-in conditions. The simulation uses "defect density," $D(\Delta X_{ox})$ extracted from oxides grown in the University laboratory.

Electromigration lifetime predictions from the vacancy recombination model[11] are implemented to calculate the current dependence of the electromigration time-to-failure. The time-to-failure under arbitrary current conditions is given by:

$$TTF_{ACDC} = \frac{A_{DC}(T)}{|J|^{m-1}\bar{J}}\left[1 + \frac{A_{DC}}{A_{AC}}\,\frac{(\overline{|J|} - \bar{J})}{\bar{J}}\right] \qquad (3)$$

We have shown that the model is valid for interconnect as well as intermetallic contact and believe that the model can be generalized to all electromigration failures. The necessary parameters m, $A_{DC}(T)$, $A_{AC}(T)$ and E_a (the activation energy in $A_{DC}(T)$ and $A_{AC}(T)$) are experimentally determined constants. The user is required to provide one set of all four parameters for each type of interconnect (up to three levels of interconnect are supported), contact and via.

Given a SPICE circuit description and without any layout information, BERT-EM can generate a set of layout advisory. The layout advisory recommends the width-length of interconnects and the number of contacts/vias in each branch of the circuit. If the layout of the circuit is given in the form of a CIF file, BERT-EM can simulate the electromigration failure rate of the circuit as a function of time, voltage, temperature, etc. Figure 5 shows an example of the BERT-EM simulation results.

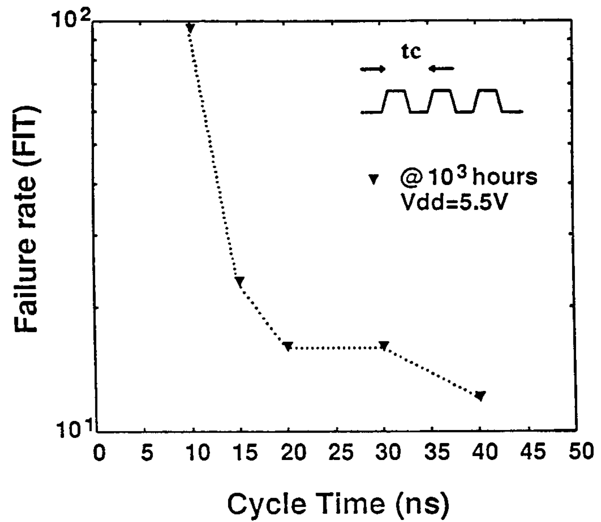

Fig. 5 The failure rate for the 21-stage BICMOS inverter chain simulated with BERT-EM increases as the cycle time of the input waveform is reduced. As the MOS transistors switches on and off more often, the average current density in the interconnect and contact becomes larger and degrades electromigration reliability.

Under emitter-base reverse bias, a small reverse current, I_R, flows through the junction due to band-to-band tunneling and impact ionization. These carriers apparently generate interface traps near the junction and introduce a component of non-ideal base forward current, ΔI_B, which causes the current gain to decrease. It can be shown that

$$\Delta I_B = D\, J_C^a \left[\int I_R^b\, dt\right]^c \qquad (4)$$

Figure 6 shows an example of the degradation of the offset voltage of an emitter coupled pair circuit and the model prediction.[12] This mechanism is not important in ECL digital circuits, where the base-emitter junctions do not experience reverse bias stress. It is a potential reliability factor in BICMOS circuits. We have simulated the increase in the low-to-high propagation delay

of a BICMOS inverter in a manner similar to CAS and found 10% speed degradation in 10 years in one case.

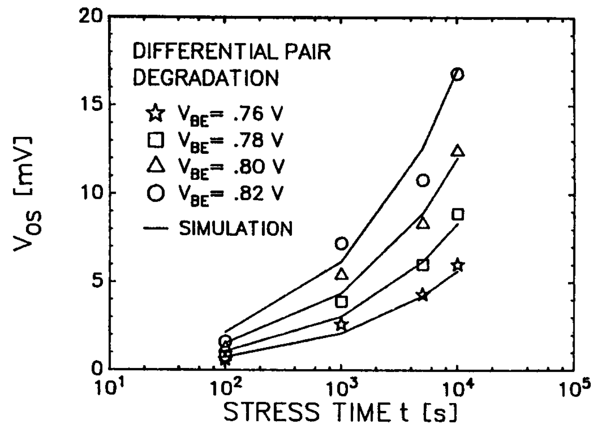

Fig. 6 Measured and simulated values of the offset voltage with stress time show good agreement. $I_R = 2\,\mu A$ and $V_R = 5.4$ V.

Summary

There are many parallel efforts in developing IC reliability simulators. A reasonable goal is to simulate circuit reliability and failure rate with CPU times comparable to typical SPICE simulations so that "design for reliability" adds only a small effort to the routine process of "design for performance." The reliability models therefore must be simple, yet accurate and general enough to pinpoint major reliability weak spots in a circuit and to always correctly predict at least the relative reliability changes in "what if" design procedures. Relevant reliability parameters of a given technology are obtained from dc accelerated tests on test structures. Failure mechanism models in a simulator can then predict the reliability of complex circuits. Simulator models for hot carrier effects, oxide breakdown, electromigration, bipolar transistor degradation, have been developed. Additional failure models will no doubt be introduced in the future.

Model and tool verification is an important part of the simulator development. Due to the long testing time and the statistical nature of reliability testing, verifying a reliability simulator with experimental data will not be easy even for a user with well established reliability study expertise. Therefore, the users will likely ask the tool developer for evidences of tool and model validity. Model development and verification is still the bottleneck in simulator development.

Users should expect a reliability simulator to require more user input than a circuit simulator, mainly in statistical data collection or parameter extraction on degraded devices. Considerable tweaking of the parameters may be necessary initially before quantitative agreement with failure data is obtained. This is somewhat similar to the early experience with IC process simulators and should not distract from the long-term potential of reliability simulations.

Acknowledgment

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