

THIN OXIDE DAMAGE BY PLASMA ETCHING AND ASHING PROCESSES

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Abstract

The plasma Al etching and resist ashing processes cause Fowler-Nordheim current to flow through the oxide. The stress current is collected only through the aluminum surfaces not covered by the photoresist during plasma processes. The plasma stress current is proportional to Al pad peripheral length during Al etching and Al pad area during photoresist stripping. Using the measured stress current, the breakdown voltage distribution of oxides after plasma processes can be predicted accurately. A model of oxide damage due to plasma etching is proposed.

Introduction

Plasma processes are widely used in manufacturing of highly integrated semiconductor devices. In the plasma process, devices fabricated on Si wafers are usually exposed to plasma directly and charges are collected by aluminum or polysilicon pads, which serve as "antennas". As a result, degradation of gate oxides in MOS devices due to plasma processes is one of the serious problems in VLSI manufacturing [1]-[4]. Since this problem will become severe with device scaling down, a complete understanding of the damage mechanism is needed.

The degradation of gate oxides is attributed to electrostatic stress during plasma process. The stress can cause surface states at SiO₂-Si interface as well as trapped charges in the oxide, therefore decreasing the breakdown voltage and deforming the CV curve of the gate oxide. It has been shown recently [5] that the stressing can be modeled as a constant current stress and that CV distortion is a much simpler and sensitive method of monitoring the stress than the reduction in oxide breakdown voltage.

Experiment

The test structures used are polysilicon-gate MOS capacitors fabricated on n-type (100) silicon substrate with 11.6 nm gate oxide thermally grown in dry oxygen at 900 °C. After n⁺ poly gate definition, 500 nm aluminum was deposited. Aluminum etching was done

in Lam Research Autoetch 690B system with a 50 % overetch after the detection of endpoints and the subsequent photoresist ashing was done in a Technics Micro stripper Series 2000 system. In addition, control wafers receiving only wet-etching and resist stripping were also fabricated. Three types of test structures are studied. One consists of 1,600 μm² capacitors with identical layout except for the size of square aluminum pads ranges from 16,000 to 160,000 μm². Another group of capacitors have elongated aluminum "antennas" with the same area of 40,000 μm² but varying peripheral lengths. The third group are large (1 mm²) capacitors with different Al pad sizes used in breakdown voltage test.

If the plasma-induced damage is due to electrostatic charging during the process, the damage to gate oxide should be identical to that produced by applying a constant current to the gate electrode for a duration equal to the process time. The current that must be applied would correspond to that collected by the antennas during the plasma process. To test this hypothesis, capacitors on wet-etched control wafers were stressed by passing different levels of constant current through the oxide for 60 s, i.e. the same time as the plasma etching time, to generate a series of reference curves, as shown in Fig. 1. Also shown in the

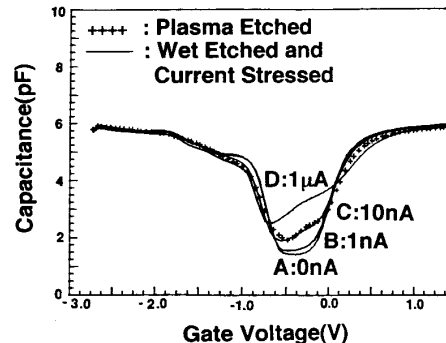


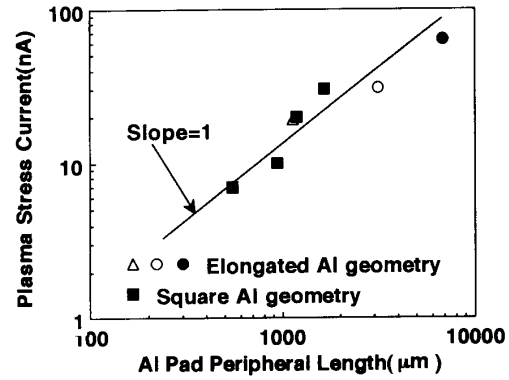
Fig. 1. CV after constant stress at varying current level. The CV after plasma etching matches very well with CV after 10 nA stress. Plasma-induced damage can be closely reproduced with a constant-current stress[5].

figure is the CV curve of a capacitor etched in plasma. This curve matches the reference curve of 10 nA constant-current stressing curve (curve C in Fig. 1) very well, indicating that the Al pad collected 10 nA of plasma stressing current during the etching process. By using the same method, the plasma stress current for each test capacitor can be extracted with a high resolution [5].

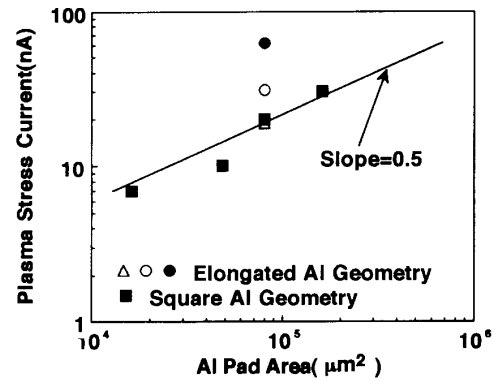
Significance of exposed Al surface

Fig. 2a shows the deduced plasma stressing current during Al etching as a function of Al pad peripheral lengths for devices located about 2 cm from the wafer center. The slope is about 1, independent of the shape of Al pads. Clearly, the stressing current does not increase in proportion to the Al pad area (Fig. 2b). Even though the elongated Al geometries have the same area, the stress currents collected by these pads are different since they have different Al peripheral lengths. Therefore, the plasma stress current is proportional to the peripheral length of Al pads (Fig. 2a). The implication is that only the Al surface exposed to the plasma, i.e., the edges of the Al geometries, can collect current and contribute to the antenna effect. To confirm this conclusion, plasma etching was done with photoresist covering the entire surface of a wafer with Al pads previously patterned by wet-etching. Fig. 3 compares the plasma stress current in these devices with the current in normal aluminum etching, during which Al was covered by patterned photoresist. The stress current detected with the Al patterns covered by a blanket photoresist layer is negligible and is independent of the location of the device, while there is a radial distribution of the plasma stress current across the wafer during normal Al etching. This confirms that the charges are collected by the pad only through the edge during etching. There was no detectable stress current in devices covered by blanket photoresist because there was no exposed Al surfaces. The radial distribution of the stress current results from the radial distribution of the plasma intensity and etch rate in this etcher. Since oxide stressing effectively occurs after the Al has been etched into individual patterns (until then, the Al is likely shorted to the substrate through one defect), the devices near the wafer edge not only experience lower stress current because of the lower plasma density but also spent little time in the etcher after the Al patterns are separated due to the lower etch rate at the wafer edge.

During photoresist ashing, most of the damage is expected to be done after the photoresist is stripped and when the entire Al pads are exposed. Fig. 4 shows the stressing current during plasma photoresist stripping as a function of aluminum pad areas. The slope of all the lines is about 1. Clearly, the plasma stressing current is roughly proportional to the area of the Al pads. We interpret this as a confirmation of the prediction that most of the damage is done after the photoresist is stripped such that the entire Al pads are exposed. To support this interpretation, capacitors with bare Al pads



(a)



(b)

Fig. 2. (a) The plasma stress current as a function of Al peripheral lengths. The plasma stress current during the etching is approximately proportional to the Al edge length, independent of the Al pads shape. (b) The same data plotted as a function of Al pad areas.

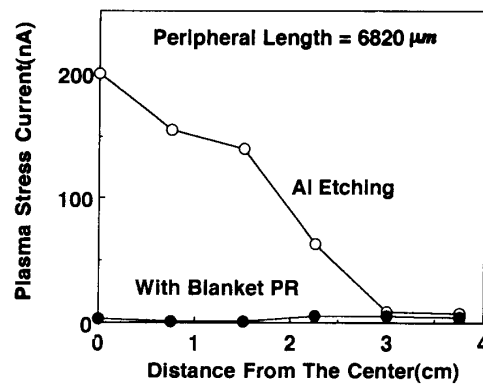


Fig. 3. Plasma stress current for different locations during aluminum etching. The photoresist can block the charges from plasma.

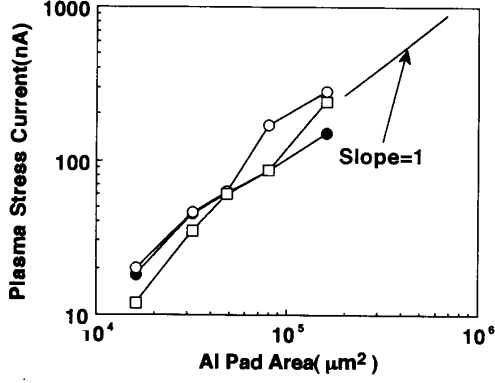


Fig. 4. Since the entire surface of the Al pad can collect charges from plasma, the plasma stress current during plasma photoresist stripping is proportional to electrode area. The four curves are for different locations on the wafer.

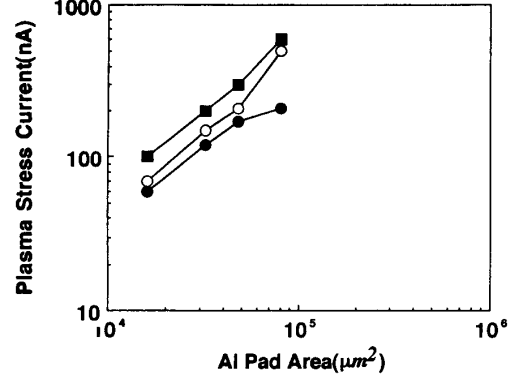


Fig. 5. The plasma stress current under plasma photoresist stripping condition without any resist present is also proportional to the Al pad area. The current is about 4 times larger than in the previous figure. Three sets of data taken from different positions are shown.

previously patterned by wet etching were put through the photoresist stripping process even though the photoresist had already been removed by a wet process. The stressing current was also found to be proportional to the area (Fig. 5). Moreover, the larger magnitude of stress current in Fig. 5 than Fig. 4 reflects the fact that for the latter case the device collected the charges during all the process time of 60 minute whereas, in former case the stress current is collected only after the photoresist is stripped and the Al is exposed.

Oxide breakdown voltage prediction

The logarithm of the time-to-breakdown t_{BD} follows a reciprocal field dependence [6]

$$t_{BD} = \tau_0 \exp\left(\frac{GX_{eff}}{V_{OX}}\right) \quad (1)$$

where V_{OX} is the voltage across the oxide, X_{eff} is the effective oxide thickness at the weakest spot in the oxide, and $G = 350$ MV/cm and $\tau_0 = 1 \times 10^{-11}$ s [7]. In general, the rate at which the oxide is damaged is a function of the stress voltage, temperature, and oxide defect severity (X_{eff}). Assuming that the rate at which "damage" accumulates may depend on those factors plus the cumulative damage that exist at that instant, the rate of increase of damage, Δ , is assumed to be [8]

$$\frac{d\Delta}{dt} = f(\Delta)g(V, T, X_{eff}) \quad (2)$$

where the functional form of f and g are unknown for now and the voltage and temperature are time-dependent ($V=V(t)$, $T=T(t)$). Eq. (2) is integrated to obtain

$$\int_0^{\Delta_{BD}} \frac{d\Delta}{f(\Delta)} = \int_0^{t_{BD}} g(V, T, X_{eff}) dt = C \quad (3)$$

where Δ_{BD} is the damage threshold level for destructive breakdown and the integrals are equal to a constant. For a constant voltage and temperature stress, the second integral in (3) can be evaluated

$$C = g(V, T, X_{eff}) t_{BD} \quad (4)$$

By comparing (4) and (1), the functional form of g is obtained

$$g(V_{OX}, T, X_{eff}) = \frac{C}{\tau_0(T)} \exp\left(-\frac{G(T)X_{eff}}{V_{OX}}\right) \quad (5)$$

Substituting for g in (3), the breakdown condition for time-dependent voltage $V=V(t)$ and temperature $T=T(t)$ is determined.

$$1 = \int_0^{t_{BD}} \exp\left(\frac{-G(T)X_{eff}}{V}\right) \frac{dt}{\tau_0(T)} \quad (6)$$

Applying (6) in case of the ramp voltage test where

$$V(t)=Rt, T(t)=T_t \quad (7)$$

and R is the ramp rate (in volts per second), the breakdown condition becomes

$$1 = \int_0^{t_{BD}} \exp\left(\frac{-G(T_t)X_{eff}}{Rt}\right) \frac{dt}{\tau_0(T_t)} \quad (8)$$

which is evaluated to obtain

$$1 \approx \frac{V_{BD}^2}{RG(T_t)\tau_0(T_t)X_{eff}} \exp\left(-\frac{G(T_t)X_{eff}}{V_{BD}}\right) \quad (9)$$

In general, (9) has to be solved numerically to determine the X_{eff} corresponding to a measured V_{BD} . However, since the X_{eff} dependence of the exponential term in (9) dominates over the X_{eff} dependence of the pre-exponential coefficient, it is possible to obtain an accurate closed-form solution for X_{eff} by setting X_{eff} in the pre-exponential term to 8 nm

$$X_{eff} \approx \frac{V_{BD}}{G(T_t)} \ln \left(\frac{V_{BD}^2}{RG(T_t)\tau_0(T_t)8nm} \right) \quad (10)$$

Fig. 6 shows the ramp breakdown voltage distribution of large (1 mm²) control capacitors. In Fig. 6, therefore, each V_{BD} of control oxides corresponds to one X_{eff} , and Fig. 6 simply reflects the density of defect spots having varying X_{eff} 's.

If a constant voltage stress is applied to the oxide before the ramp test is done (such as in oxide burn-in or plasma-induced stress), the breakdown condition (6) is simply a summation of the damage incurred during stress Δ_{stress} and that incurred during the ramp test Δ_{test}

$$1 = \Delta_{stress} + \Delta_{test} \quad (11a)$$

$$1 \approx \frac{t_s}{\tau_0(T_s)} \exp\left(-\frac{G(T_s)X_{eff}}{V_s}\right) + \frac{V_{BD}^2}{RG(T_t)\tau_0(T_t)X_{eff}} \exp\left(-\frac{G(T_t)X_{eff}}{V_{BD}}\right) \quad (11b)$$

where the oxide is subjected to a stress at V_s volts and T_s kelvin for t_s seconds and has a subsequent ramp test at T_t . Since the plasma process can be modeled as a constant current (or voltage) stress, (11) is used for prediction of the ramp breakdown voltage after plasma process. Fig. 6 compares the ramp breakdown voltage distribution of capacitors having 9 mm² metal pads after plasma etching with the breakdown voltage distribution of control oxides. Again, remember each V_{BD} corresponds to a certain X_{eff} (Eq. 10). From the measured 2 pA/ μ m value of electrical stress current during plasma etching and the oxide IV characteristics, the voltage appearing on the gate of 1 mm² oxide during the process can be determined to be $V_s = 9.0$ V. Using this stress voltage in eq. (11), the ramp breakdown voltage distribution of capacitors after etching is predicted for each X_{eff} of control (wet oxide etch) oxides, and plotted in Fig. 6. The predicted curve matches the measured distribution very well.

Similarly, the breakdown voltage distribution after photoresist stripping was accurately predicted for two different antenna ratios (Fig. 7) using (11). The two oxide stress current densities are $J_{ox} = 34.2$ mA/cm² and $J_{ox} = 3.8$ mA/cm², i.e., $V_s = 11.9$ V and $V_s = 10.9$ V, for oxides with antenna ratios of 9 and 1 respectively.

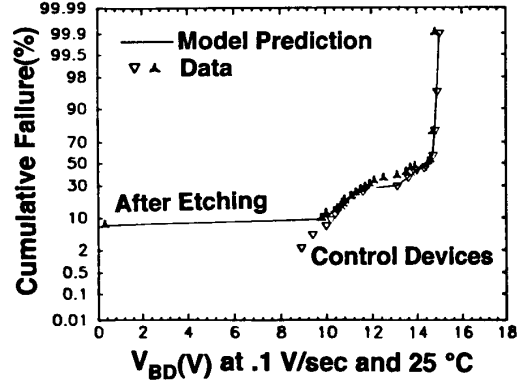


Fig. 6. Cumulative failure vs. breakdown voltage for 1 mm² capacitors after Al etching. The model matches the data very well.

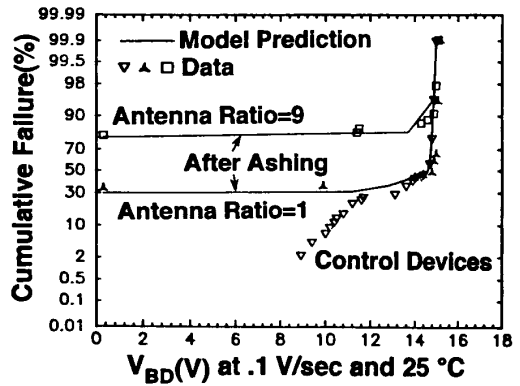


Fig. 7. The breakdown voltage distribution after photoresist ashing can be predicted accurately.

Improvement to DC stress model

During rf plasma processes, the surface of the wafer collects conduction current from the plasma which is composed of steady ion current and pulsed electron current [9] (Fig. 8). Therefore, the plasma process can better be modeled as a bi-directional current stress. For simplicity, however, we have arbitrarily modeled the stress current as a DC current. We feel that this simplification can be refined at a later time. The magnitude of the ion current during plasma etching is given by

$$J_i = \epsilon_0 \left(\frac{2e}{M} \right)^{\frac{1}{2}} \frac{V_0^{\frac{3}{2}}}{s^2} \quad (12)$$

where ϵ_0 is permittivity, e is electronic charge, M is ion mass, V_0 is the DC voltage across two plates and s is the sheath thickness. The DC voltage V_0 was measured to be 400 volts at 500 watts and 120 volts at 250 watts. The

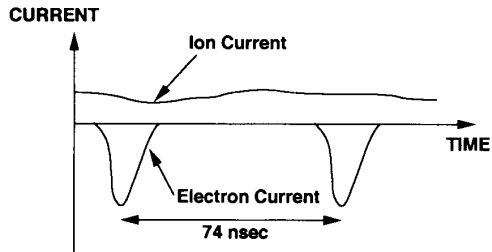


Fig. 8. Conduction current during rf plasma discharge. The areas under the ion current and the electron current are the same [9].

sheath thickness s is about 0.5 cm and is almost independent of the power level. Fig. 9 compares the calculated ion current with the stress current deduced from the CV measurement for different power levels. The experimental value and the calculated ion current value is of the same order of magnitude and the difference is attributed to the electron current component and possibly the enhanced rate of interface trap generation under AC stress [10].

Conclusion

The stress current is collected only through the aluminum surfaces not covered by the photoresist during plasma processes. Using the measured stress current, the breakdown characteristics after plasma processes can be predicted accurately. A model of oxide damage due to plasma etching is proposed.

Acknowledgement

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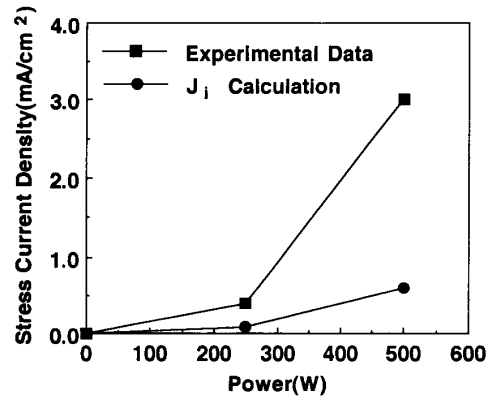


Fig. 9. Plasma stress current per unit area of exposed Al surface and predicted ion current density at different powers.

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