AN ACCURATE MODEL OF THIN FILM SOI MOSFET BREAKDOWN VOLTAGE

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Abstract

A quantitative model which relates the SOI MOSFET breakdown voltage to key parameters such as channel length, SOI film thickness and gate voltage is presented. The SOI breakdown is caused by electron impact ionization current produced near the drain which is subsequently amplified by parasitic lateral bipolar transistor. This model is based on analytic modeling, quasi-2D simulation and experimental study of the maximum drain electric field in SOI, and a novel method for measuring the lateral BJT current gain β using GIDL current. It can accurately model the breakdown voltage within 0.2V for different channel lengths, gate voltages and SOI film thicknesses.

I. Introduction

Low breakdown voltage is a major problem for short channel SOI MOSFET's, and many have studied this problem[1-5]. Due to its floating body, an SOI MOSFET's exhibits different breakdown behavior compared with bulk device. An accurate model is needed to relate the breakdown voltages to important device parameters as film thickness and provide design guidelines. In this paper, we studied the mechanism of SOI MOSFET breakdown and modeled breakdown voltage as function of SOI MOSFET parameters. The key is to find the correct maximum drain electric field E_M and lateral BJT gain β. The model can predict the breakdown voltage dependence with channel lengths, gate voltages, gate oxide thickness, and SOI film thicknesses.

II. SOI MOSFET Breakdown Model

The SOI devices used in this study were fabricated on SIMOX (Separation by IMplanted OXygen) wafers using a modified sub-micron CMOS technology. The SIMOX wafers were implanted with a high dose of oxygen ions (10^{18} cm^{-2}) at 200 KeV and subsequently annealed at 1230°C. Thin SOI films were obtained by thermal oxidation and subsequent etching of the oxide layer. The SOI film thickness measured by CV technique ranges from 68nm to 100nm [6], and the floating body is P-type with acceptor density of $1\times10^{17}cm^{-3}$.

A schematic diagram illustrating current flow in an SOI n-channel MOSFET is shown in Fig.1. At high drain voltages, electron and hole pairs are created by impact ionization when the device is on, or by gate-induced-drain-leakage (GIDL) [7] current when the device is off and a high electrical field exists between drain and gate. Hole current flows to the floating body and forward biases the source-body junction which is the emitter-base junction of the lateral npn BJT. Drain current is amplified by lateral BJT and by impact ionization due to maximum drain electrical field E_M. In SOI MOSFET's, the total drain current can be modeled as:

$$I_D = \frac{M(\beta+1)}{1-(M-1)\beta} I_{GIDL} + \frac{M}{1-(M-1)\beta} I_{CH} \qquad (1)$$

here $M-1=1.2(V_D-V_{DSAT})\exp[-B_i l/(V_D-V_{DSAT})]$, V_{DSAT} is the saturation voltage, β is the lateral BJT gain. From analytic modeling and quasi-2D simulation, the channel field display a near-exponential rise towards the drain as in Fig.2, and the pseudo-two-dimensional model [8] still apply. Through simulation and experiments [9], it is found that $l=0.22(1.6T_{Si})^{1/2}T_{OX}^{1/3}$ for thin film SOI devices. This leads to a higher E_M for thin film SOI than bulk device since $E_M=(V_D-V_{DSAT})/l$, and $1.6T_{Si}<X_j$ typically.

Figures 3 and 4 show the breakdown characteristics of long and short channel SOI MOSFET's. For $V_G>V_T$, the drain current is dominanted by I_{CH} in eqn.(1), and the breakdown voltage increases as gate voltage increases. There is snap-back in the drain current for long channel device at low V_G. When $(M-1)\beta$ reaches 1, current increases which turns on the source substrate junction and β rises, hence smaller M, i.e., lower V_D, is needed to sustain $(M-1)\beta=1$ so snap-back happens. For short channel device, because V_{BE} "on" is satisfied before $(M-1)\beta=1$, there is no snap-back.

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At negative gate voltages, GIDL current is amplified and breakdown occurs as shown in Fig.5. Breakdown is initiated at the same current level for different V_G's because at that current level the source-substrate (emitter-base) junction turns on. Thus, three factors determine the drain breakdown voltage as illustrated by the measured breakdown voltages vs. V_G shown in Fig.6. At high V_G, breakdown is limited by $(M-1)\beta=1$. As V_G approaches V_T, the junction is difficult to turn on and breakdown is limited by $V_{BE}=0.7V$. As V_G becomes more negative, the GIDL current increases and lowers the breakdown voltage. The observed breakdown voltage is limited by the dominant of these factors.

III. Using GIDL Current TO Measure β

In order to model the breakdown accurately, the parasitic BJT current gain, β, must be determined. We developed a novel technique to measure β. This technique is illustrated in Fig.7 in which the GIDL currents of SOI devices were shown for different channel lengths at low drain voltages and negative gate voltages. GIDL current is known to be independent of channel length [7]. However in an SOI MOSFET, I_{GIDL} serves as base current of the lateral BJT and is amplified. The measured drain current is therefore $(\beta+1)I_{GIDL}$. Notice that this is the special case for eqn.(1) when M-1=0. For the long channel device, β=0 and the measured current is simply I_{GIDL}. Hence the ratio of the GIDL currents for short channel and long channel device is β+1, where β is the lateral bipolar transistor current gain of the short channel device. It is found that the GIDL currents for L=10μm and L=50μm devices are the same as expected. As shown in Fig.7, the GIDL currents for L=10μm and L=1.1μm devices are equal for low I_D because β is very small at very low collector current levels even for the 1.1μm device. Current gain β increases with increasing collector level. Fig.8 shows the measured β for different channel lengths. It shows that current gain β is basically zero for channel lengths above 4μm, and it is not sensative to gate voltages.

IV. Results and Discussions

Using the measured β and eqn.(1) and defining breakdown as the bias point when $I_D=2I_{CH}$, V_{BD} was calculated for different channel lengths and gate voltages. Very good agreement was achieved for different channel lengths and gate voltages as shown in Fig.9. The low breakdown voltage for short channel SOI MOSFET's is due to increasing lateral BJT gain β. A general expression for breakdown voltage is:

$$V_{BD} = V_{DSAT} + \frac{B_i 0.22(1.6T_{Si})^{1/2}\ T_{ox}^{1/3}}{\ln[1.2(V_{BD}-V_{DSAT})(1+2\beta)]} \qquad (2)$$

As SOI film thickness reduces, E_M become higher and M-1 increases, which in turn will lower drain breakdown voltages. Fig.10 shows the measured and calculated breakdown voltage as a function of SOI film thickness T_{Si} for different V_G's. The breakdown voltage is a weak function of SOI T_{Si}. When T_{Si} change from 50nm to 100nm, the breakdown voltage increases by about 0.5V. This is important to know to SOI film thickness scaling. Fig.11 shows the breakdown characteristics of SOI MOSFET's with different film thicknesses. Note that the devices with thicker T_{Si} has higher breakdown voltage because of smaller E_M. Beyond the breakdown voltage, drain current increases more slowly with voltage than that of bulk MOSFET's because the current becomes space charge limited as shown in Fig.12.

V. Conclusion

A physical model which relates the breakdown voltage of SOI MOSFET to key parameters such as channel length, SOI film thickness and gate voltage is presented. Parasitic lateral BJT current gain β were measured for calculation of breakdown voltage in the model. Breakdown voltage decreases with thinner SOI film thickness T_{Si}, but is a weak function of T_{Si}. When T_{Si} increases from 50nm to 100nm, breakdown voltage increases by about 0.5V.

VI. Acknowledgement

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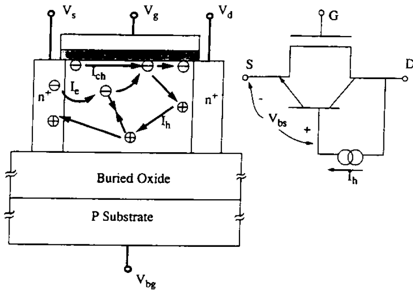

Fig.1 Schematic of n-channel SOI MOSFET current flow operated in the breakdown regime. Hole current I_h is the lateral npn bipolar transistor base current.

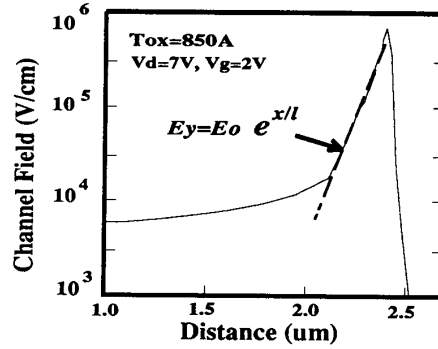

Fig.2 PISCES simulation of channel electric field versus position in the channel near the drain for SOI MOSFET. It shows near exponential rise so the analysis in [8] holds.

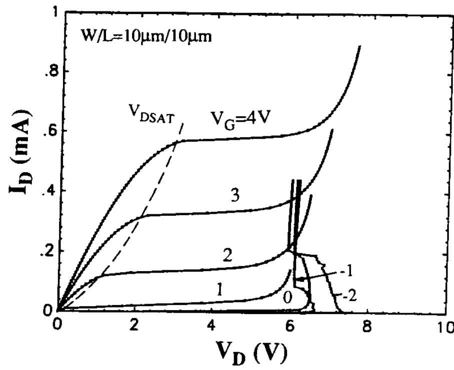

Fig.3 Measured I-V characteristics of long channel SOI MOSFET with L=10µm in the breakdown region by ramping current. When $V_G<V_T$, there is snap-back in the drain current.

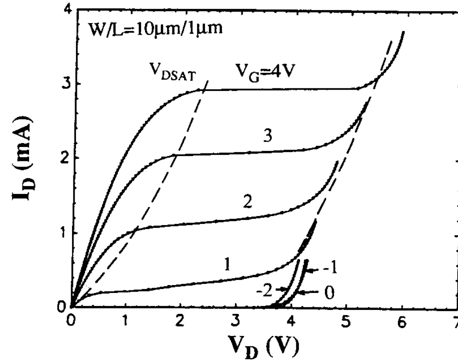

Fig.4 I-V characteristics of short channel SOI MOSFET with L=1µm in the breakdown region. There is no snap-back for the short channel device because the V_{BE}=0.7V is satisfied before (M-1)β=1. The dashed line shows the V_{DSAT} contour which is parallel to the breakdown contour.

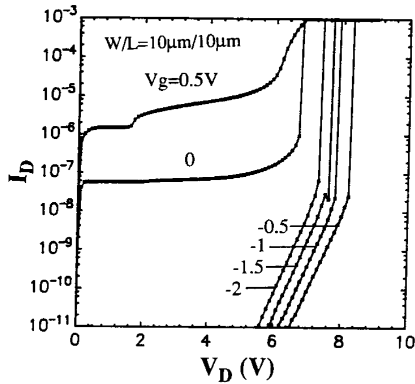

Fig.5 Breakdown characteristics at negative gate voltages. Starting from V_G=-0.5V, GIDL current causes breakdown which happens at a fixed current level where the source-substrate(emitter-base) junction turns on.

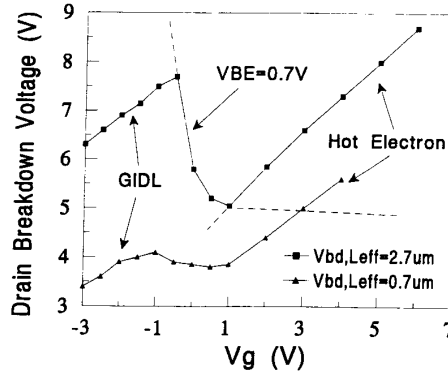

Fig.6 Breakdown voltage as a function of gate voltage. The breakdown voltage is limited by V_{BE}, M-1, and the GIDL current.

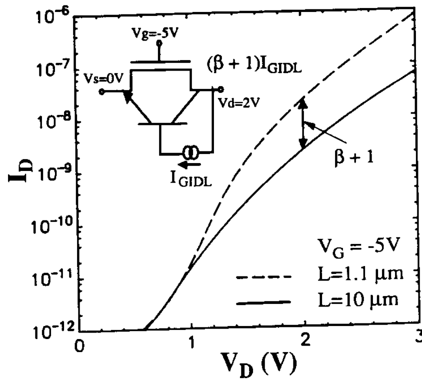

Fig.7 GIDL currents of long channel and short channel SOI MOSFET's. I_{GIDL} is the base current of the lateral bipolar transistor and gets amplified. From the ratio of those two the bipolar gain β of short channel device can be deduced.

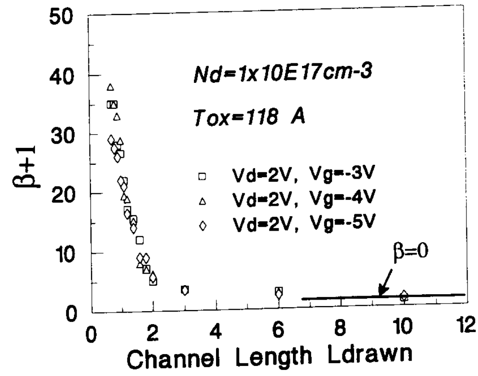

Fig.8 Lateral bipolar transistor current gain β for different channel lengths.

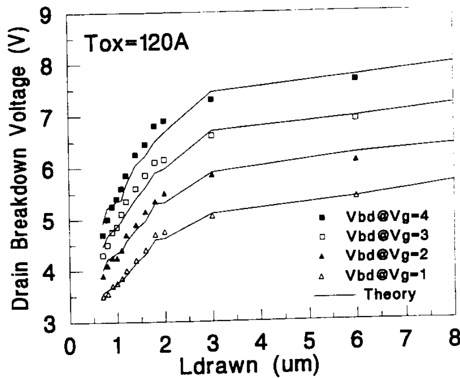

Fig.9 Measured and modeled values of breakdown voltage for different channel lengths and gate voltages.

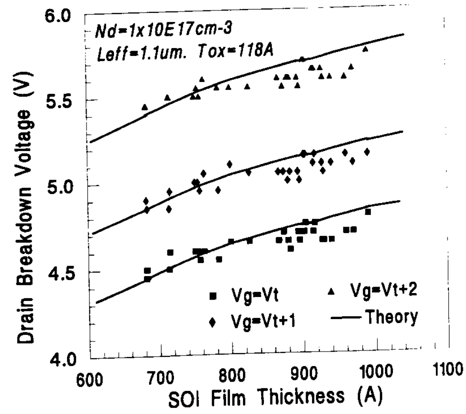

Fig.10 Measured and modeled values of breakdown voltage versus SOI film thickness T_{Si}.

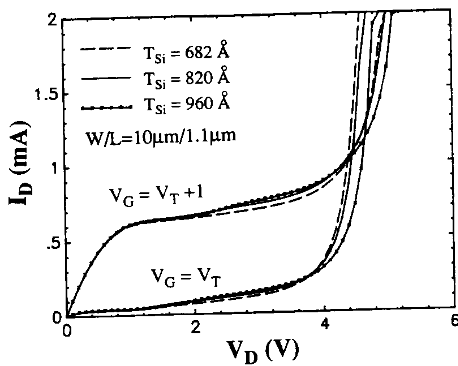

Fig.11 I-V characteristics of SOI MOSFET's with different film thicknesses. The MOSFET with thicker film has higher breakdown voltage.

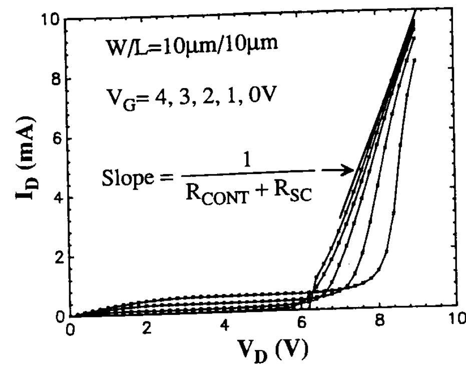

Fig.12 I-V characteristics of SOI device beyond breakdown voltage. Current increases more gently than bulk MOSFET with voltage due to space charge limitation in the SOI film.