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SIMULATION OF P- AND N-MOSFET HOT-CARRIER DEGRADATION IN CMOS CIRCUITS

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Abstract

A PMOSFET hot-carrier degradation model has been incorporated into the reliability simulator BERT-CAS, enabling prediction of dynamic circuit-level degradation in which both PMOSFET and NMOSFET degradation play a major role. Comparisons are presented which reveal the good fit obtained between measurement and simulation results.

Introduction

Within the past decade, there has been much concern over hot-carrier degradation as MOSFET device dimensions continue to shrink. There have been many device-level studies which have greatly increased the understanding of the mechanisms causing degradation, and the more recent papers have focussed on degradation caused by AC waveforms, which more closely mimic conditions seen within an operating circuit.

It remained unclear, however, how device degradation would affect the actual behavior or performance of the circuit. This lack of understanding caused device engineers to arbitrarily set device degradation guidelines which were too stringent and increasingly difficult to satisfy. Thus, reliability simulators were developed to study what affects device degradation had on circuit output^{1,2,3}. These circuit simulators use voltage information calculated by circuit simulators to calculate the individual device degradation that occurs. This degradation information is then used to calculate degraded model parameters which would be used to calculate the actual degraded behavior of the circuit. Up to now, hot-carrier simulations incorporated NMOSFET degradation only, as this was the dominant degradation. However, with increasingly shrinking device dimensions, stressed-induced drift in PMOSFET characteristics may become more significant.

In this paper, we present for the first time results of hot-carrier simulation incorporating both NMOSFET and PMOSFET degradation using the Berkeley Reliability Tools - Circuit Aging

Simulator (BERT-CAS)². Using CAS, circuit degraded behavior after a user-specified operating time can be simulated. Modeling circuit degradation involves three steps - calculating the amount of device degradation suffered under circuit operating conditions, determining the degraded model parameters from the degradation calculated, and re-simulating the circuit using the aged model parameters. These concepts will be discussed in detail in the following sections, with a comparison of simulation results with measured data from CMOS ring oscillators to conclude the paper.

Device Degradation Model

CAS is based on the concept that the amount of stress experienced by an individual device is expressed by a quantity called "Age". The amount of degradation suffered by the device, whether it be drain current degradation $\Delta I_{ds}/I_{ds0}$, threshold voltage shift ΔV_{th} , transconductance degradation $\Delta g_m/g_{m0}$, etc., can all be described by a physical model developed by Hu et al.⁴:

$$\Delta D(t) = \left[\frac{I_{ds}(t)}{WH} \left(\frac{I_{sub}(t)}{I_{ds}(t)} \right)^m t \right]^n \quad (1)$$

where $\Delta D(t)$ represents any of the degradation mechanisms, $I_{sub}(t)$ and $I_{ds}(t)$ are the time-varying substrate and drain currents that result from dynamically-changing voltage waveforms, W is the device width, t is the time, and H , m , and n are parameters extracted from device stressing measurements. Using this formulation, an expression for Age can be derived so that there is a direct relationship to ΔD of Eq. 1 but is linearly dependent on time:

$$\text{Age}(t) = \frac{I_{ds}(t)}{WH} \left(\frac{I_{sub}(t)}{I_{ds}(t)} \right)^m t \quad (2)$$

Eq. 2 is time-integrated for each device in the circuit to obtain the ages that the circuit devices would have after undergoing a user-specified circuit operating time.

The same concept is used to model the degradation for PMOSFET devices, except that it is less clear what currents to base the degradation ΔD upon. Available data⁵⁻¹¹ suggest that either I_{sub} or the gate current I_{gate} can correlate with the degradation, depending upon the technology. We therefore developed an expression for Age based on both currents using weighting coefficients that can be tailored by the user to describe the degradation for the particular technology in question:

$$Age(t) = \left\{ W_g \left[\frac{1}{H_g} \left(\frac{I_{gate}(t)}{W} \right)^{m_g} \right] + W_b \left[\frac{I_{ds}(t)}{WH_b} \left(\frac{I_{sub}(t)}{I_{ds}(t)} \right)^{m_b} \right] \right\} t \quad (3)$$

where the first term in square brackets corresponds to degradation correlating with I_{gate} , the second term pertains to degradation correlating with I_{sub} , and W_g and W_b are the weighting coefficients that determine the contributions that each term has to the degradation. m_g , H_g , m_b , and H_b are degradation parameters that can be extracted from DC device stressing measurements, W is the device width, and t is the time.

To calculate an accurate Age using Eqs. 2 and 3, a good fit must be obtained for I_{sub} and I_{gate} . The I_{sub} model used is a parametric form of the physical model developed in Refs. 12 and 13:

$$I_{sub} = \frac{A_i}{B_i} I_{ds} (V_{ds} - V_{dsat}) \exp\left(-\frac{B_i l_c}{V_{ds} - V_{dsat}}\right) \quad (4)$$

where

$$V_{dsat} = \frac{E_{crit} L (V_{gs} - V_{th})}{E_{crit} L + V_{gs} - V_{th}} \quad (5)$$

and l_c and E_{crit} are parametrized to take into account bias-dependencies. Fig. 1 shows the good I_{sub} fit achievable for the NMOSFET.

For PMOSFET devices, the same I_{sub} model as described in Eqs. 4 and 5 is used, and in addition, a lucky-electron gate current model developed in Refs. 10 and 14 is used for modeling I_{gate} in the Age expression of Eq. 3.

$$I_{gate} = G_1 \frac{I_{sub} t_{ox}}{\lambda_r} \left(\frac{\lambda E_m}{\phi_b} \right)^2 P(E_{ox}) \exp\left(-\frac{\phi_b}{E_m \lambda}\right) \quad (6)$$

where $P(E_{ox})$ is the probability that a scattered electron will surmount the oxide energy barrier and flow to the gate, ϕ_b is the oxide barrier height, $\lambda = 105\text{\AA}$ is the electron scattering mean free path, $\lambda_r = 616\text{\AA}$ is the electron re-direction scattering mean free path, and G_1 is a constant. Figs. 2 - 4 show the good I_{sub} and I_{gate} fit achievable for both buried- and surface-channel PMOSFETs using analytical lucky-electron current models.

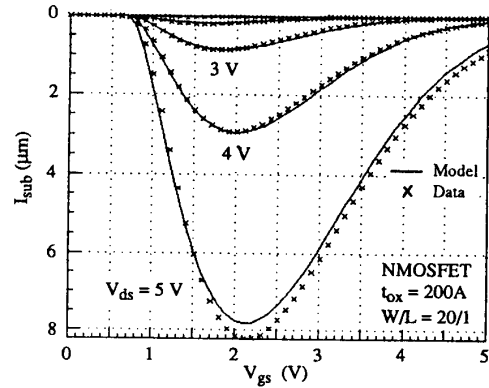


Fig. 1 Simulated NMOSFET substrate current I_{sub} versus V_{gs} at various V_{ds} showing good agreement with the measured data.

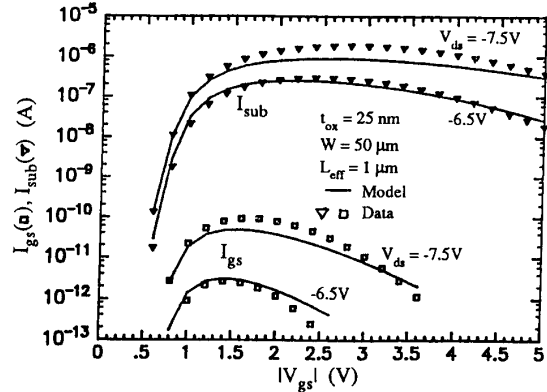


Fig. 2 Measured and simulated I_{sub} and gate current I_{gate} for a buried-channel ($n+$ poly gate) PMOSFET. I_{gate} model is the lucky-electron model^{10,14}.

Calculating Aged Model Parameters

Once the Age (the amount of degradation) for each device in the circuit is calculated, degraded model parameters corresponding to the age values must be generated. To do this for each circuit device, a set of model parameters extracted beforehand from individually stressed devices with known ages are used.

Fig. 5 illustrates the concept of aged model parameter calculation. The top row of barrels represent the model parameters extracted beforehand from individual devices at zero stress, and at successively higher levels of stress. Each model parameter set has a unique age value associated with it (calculated from Eqs. 2 and 3). Using this set of model parameters with unique age values, and using the age values calculated for each

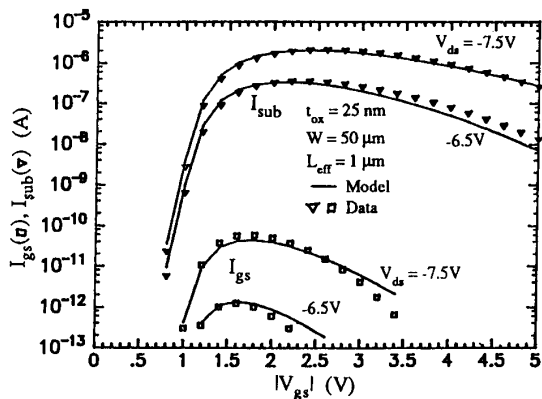


Fig. 3 Simulated and measured I_{sub} and I_{gate} for a surface-channel (p+ poly gate) PMOSFET. I_{gate} model is the same as that for the buried-channel device of Fig. 2.

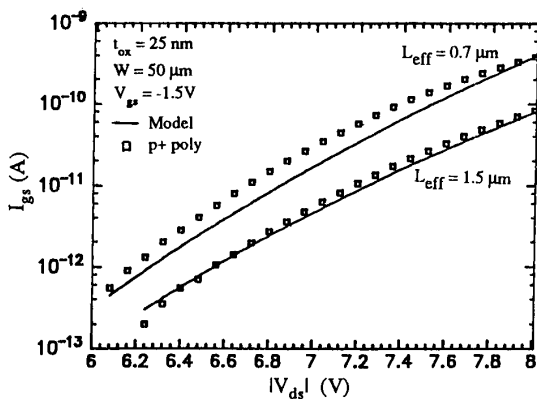


Fig. 4 I_{gate} versus V_{ds} for the surface-channel PMOSFET showing again good agreement.

device in the circuit, the aged model parameters of the circuit devices can be calculated by interpolation (shown here) or by regression using all of the pre-stressed model parameters.

To achieve accurate simulation, a good fit must be obtained for the drain currents of the fresh and stressed P- and N-MOSFET's. For inverter-based circuits, the area most affecting speed degradation is the linear to saturation transition region¹⁵. Figs. 6 and 7 show the fit achieved for both types of devices under fresh and stressed conditions using the Berkeley Short-channel I_{gfet} Model Version 2.0 (BSIM2) drain current model¹⁶.

Once the aged model parameters for all devices in the circuit are calculated, the circuit can be re-simulated to obtain the overall

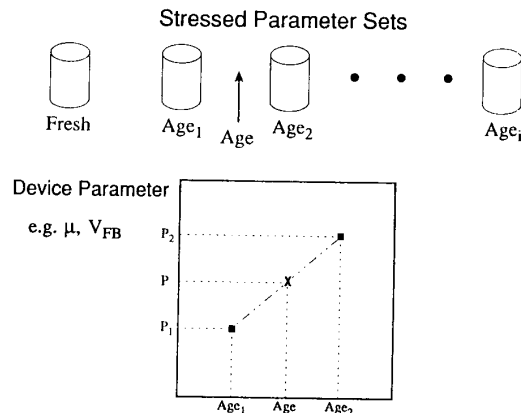


Fig. 5 Concept of calculating aged model parameters from pre-stressed extracted parameters. Top row of barrels represent the stressed model parameters extracted beforehand, each with its unique value of Age. Interpolation using the first and second stressed model parameter sets with ages Age₁ and Age₂ is shown in this example to find the degraded model parameter set of the circuit device with age Age.

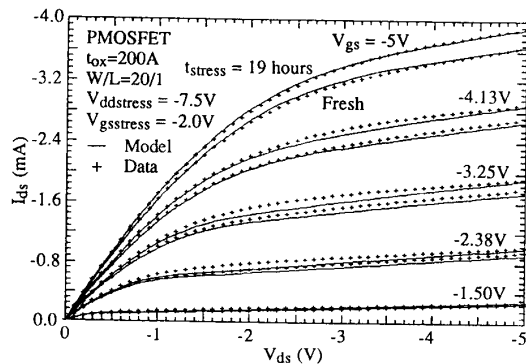


Fig. 6 Measured and BSIM2-simulated PMOSFET fresh and stressed I_{ds} versus V_{ds} curve showing good modeling prediction.

degraded behavior. The next section shows examples comparing these simulation results with actual measured data.

Experimental and Simulation Results

This section presents measured and simulated results of CMOS ring oscillators from two different technologies which exhibit different hot-carrier degradation characteristics.

The first example shows a 0.5 μ m channel length 125-stage ring oscillator specifically designed to enhance NMOSFET hot-

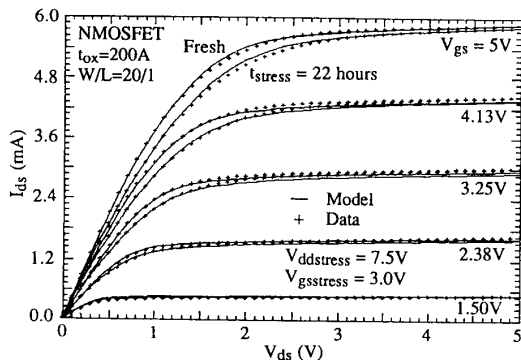


Fig. 7 Measured and BSIM2-simulated NMOSFET fresh and stressed I_{ds} versus V_{ds} curve showing good modeling prediction.

carrier degradation. Two modifications were made to enhance the degradation: 1) the PMOSFET devices were fabricated as LDD devices while NMOSFET's were processed as non-LDD devices; and 2) nitride passivation with higher than usual hydrogen content was directly deposited over the first metal layer for one of the splits (the other split used standard PSG passivation and was used for comparison). Circuit stressing was performed at $V_{dd} = 5.9V$, while frequency degradation was monitored at the lower supply voltages of $V_{dd} = 3.3, 4,$ and $4.5V$. The performance criteria used for comparison was percentage frequency degradation $\Delta f/f_0$. Two capacitive loading configurations were also measured to see how hot-carrier degradation was affected.

Fig. 8 shows percentage frequency degradation for the

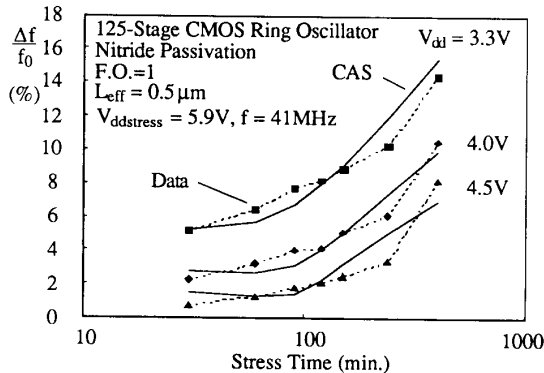


Fig. 8 Measured and CAS-simulated percentage change in frequency ($\Delta f/f_0$) versus stress time at different frequency-measuring V_{dd} values for the NMOSFET-degradation-enhanced 125-stage ring oscillator. Fan-out is equal to 1.

nitride-passivated fanout = 1 case revealing the excellent fit between measurement and CAS simulation at successive stress times and different monitoring V_{dd} values. $\Delta f/f_0$ is larger at the lower monitoring V_{dd} values because percentage drain current degradation (which affects propagation delay directly¹⁵), is larger at the lower biases. Fig. 9 shows the same ring oscillator except with higher capacitive loading (fanout = 3). Frequency degradation remains relatively unchanged from the unloaded case of Fig. 8, most likely due to the fact that although higher loading causes more degradation (longer overlap between the gate and drain pulses), the circuit oscillates at a lower frequency, decreasing the stress time of the NMOSFETs, counterbalancing the loading effect. Fig. 10 shows the successful simulation of the order-of-magnitude difference in degradation between the hot-carrier-resisting PSG and hot-carrier enhancing nitride passivations. In all cases, absolute error was less than 2% in percentage frequency degradation.

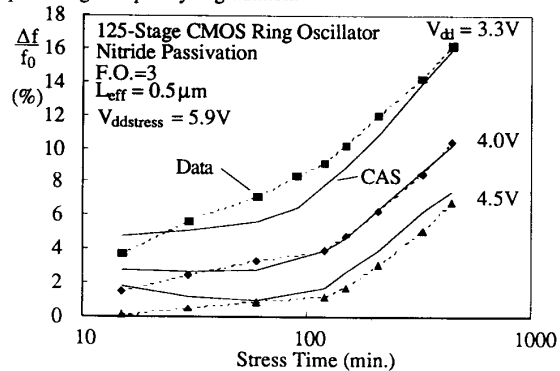


Fig. 9 Measured and CAS-simulated $\Delta f/f_0$ for the same ring oscillator as in Fig. 8 except fan-out is equal to 3.

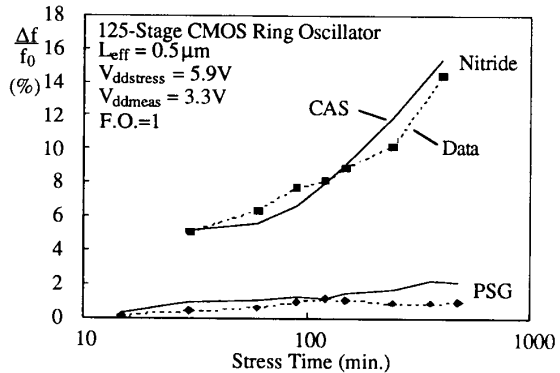


Fig. 10 Measured and CAS-simulated $\Delta f/f_0$ for the ring oscillator in Fig. 8 and an identical ring oscillator but with PSG passivation.

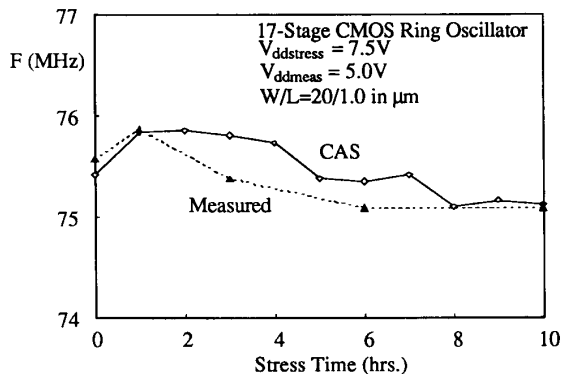


Fig. 11 Measured and CAS-simulated frequency degradation versus stress time for a 17-stage ring oscillator with both P- and N-MOSFET degradation apparent.

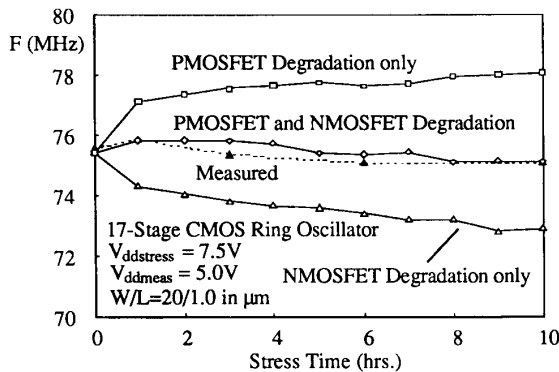


Fig. 12 CAS-simulated examples of the effect that the NMOSFET, the PMOSFET, and the combined degradation mechanisms have on the frequency degradation.

In contrast to the first example, Figs. 11 and 12 show results from a $1.0 \mu\text{m}$ 17-Stage CMOS ring oscillator with the reverse configuration of LDD NMOSFET's and non-LDD PMOSFET's. Stressing was done at $V_{dd} = 7.5\text{V}$, and frequency was measured at $V_{dd} = 5\text{V}$. The initial increase in frequency due to PMOSFET current enhancement from hot-carrier stress (see Fig. 6) can clearly be seen. NMOSFET degradation is then seen to dominate during later stages of stress, causing the non-monotonic behavior in frequency degradation. Fig. 12 shows CAS simulation examples of the frequency change when 1) only NMOSFET degradation is taken into account, 2) only PMOSFET degradation is calculated, and 3) when both degradation mechanisms are accounted for (identical to Fig. 11).

Conclusion

This paper has presented both simulation results and measurement verification of P- and NMOSFET hot-carrier degradation in CMOS ring oscillator circuits. For PMOSFET's, a degradation model valid for both surface- and buried-channel devices is used that incorporates both the substrate and gate currents through user-specified weighting coefficients. In addition to presenting and verifying the model and simulator, this study suggests that both P- and NMOSFET degradations, in inverter-based circuits at least, can be predicted from DC measurements.

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