Hot Electron Gate Current and Degradation in P-Channel SOI MOSFET's

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Hot-electron degradation is an important device reliability issue for short channel MOSFET's. The maximum drain electric field, E_m, determines device degradation. I_{SUB} is a function of E_m and in bulk n-MOSFET's, it is used as a lifetime monitor. However it is difficult to measured I_{SUB} in fully depleted SOI MOSFET's. I_G in p-channel devices is a function of E_m and may be used as lifetime monitor. In this paper, I_G in p-channel SOI MOSFET is modeled and device degradation is characterized. It is found that E_m is about the same as in bulk devices.

The SOI devices used in this study were p+ polysilicon gate P-channel MOSFET's fabricated using a modified sub-micron CMOS technology on SIMOX (Separation by IMplanted OXygen) wafers. In Fig.1, gate current of a P-channel SOI MOSFET is shown. It exhibits behavior similar to that in bulk p-MOSFET devices. Bulk P-channel device gate current has been modeled in [1,2,3].

$$I_{GATE} = 0.5\frac{I_D A_i E_m l T_{OX}}{B_i \lambda_\gamma}\left(\frac{\lambda E_m}{\Phi_b}\right)^2 P(E_{ox})\exp\left(\frac{\Phi_b}{E_m \lambda}\right)\exp\left(\frac{B_i}{E_m}\right) \tag{1}$$

$$E_m = \frac{V_D - V_{DSAT}}{l} \quad \text{and} \quad l = 0.22 X_j^{1/2} T_{OX}^{1/3} \tag{2}$$

X_j is the junction depth in bulk device, and the definitions of A_i etc. can be found in [1,2,3].

In thin film SOI MOSFET's, the physical junction depth is the same as the film thickness, T_{Si}. Some have proposed to use the above expression for l with $X_j=T_{Si}$ to estimate the maximum electric field E_m[4]. So far there is neither experimental study nor model of the maximum drain electric field E_m which determines the rate of device degradation and the breakdown voltage. This is because in fully-depleted SOI devices it is hard to measure and interpret the substrate current. Since T_{Si} is normally less than 1000Å for fully-depleted devices, one would expect SOI device has a higher E_m than bulk MOSFET's in eqn.(1) and (2).

However, we found in our study that using $X_j=1.6T_{Si}$, gate current in PMOS SOI can be well modeled as shown in solid lines of Fig.1. If $X_j=T_{Si}$ is used, the simulated gate current level will be more than two orders of magnitude higher than measured value. This suggests that using $X_j=T_{Si}$ overestimates the peak drain electric field in a SOI MOSFET. It is expected that the thinner the SOI silicon film thickness, the higher the maximum electric field will be. This is indeed observed as shown in Fig.2. The dependence of I_G on silicon film thickness T_{Si} is shown. The dashed line is calculated from the above model with X_j set to $1.6T_{Si}$. As measured data and the model show, the gate current is not very sensative to SOI silicon film thickness in the range of interest, which is less than 1000Å for fully-depleted devices.

Drain currents before and after hot-electron stressing with forward and reverse source/drain are shown in Fig.1. The device was stressed at the gate current peak. Due to stressing, electrons were injected into the oxide near the drain and some were trapped. Those negative charges induce a p^- region near the drain and cause channel shortening and device degradation. Interestingly, the back gate device drain current was also degraded after stressing as shown in Fig.4. One possible explanation is that in SOI devices, even though the negative charge was injected into the front gate oxide, the channel shortening effect is seen for the back gate transistor as well. Fig.5 shows the time dependence of $\Delta I_D/I_D$ for different V_G. After steep degradation during the first minute, the degradation follows a t^n dependence. Fig.6 shows that the peak degradation of both I_D and G_m occurs close to the I_g peak. This indicates that electron injection is the dominant mechanism for PMOS degradation in SOI and similar to bulk PMOS[5].

Acknowledgement

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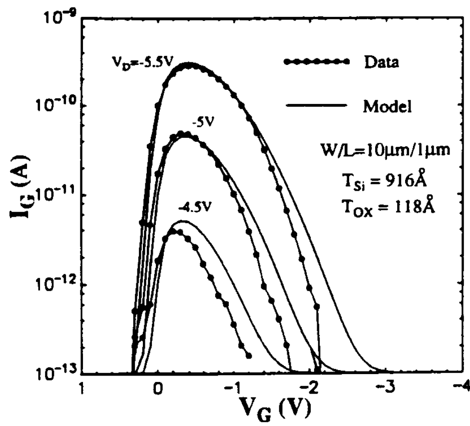

Fig.1 Gate current of P-channel SOI MOSFET. The gate current peaks at low V_G close to V_T. Solid lines are calculated from model.

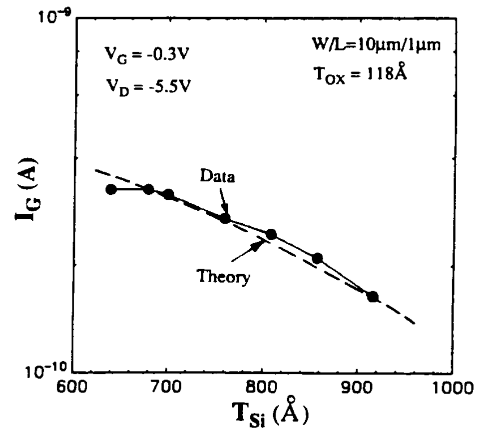

Fig.2 SOI silicon film thickness dependence of gate current in P-channel MOSFET. The dashed line is calculated form model.

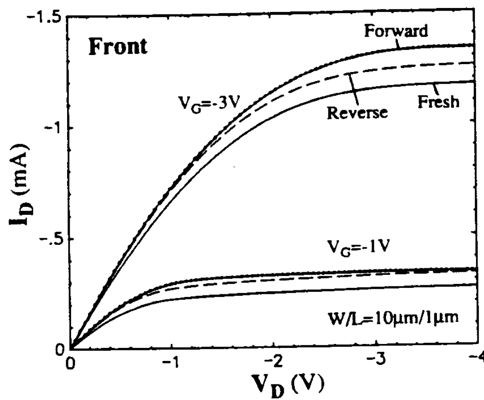

Fig.3 Drain current I_D before and after hot-electron stressing for P-channel SOI MOSFET.

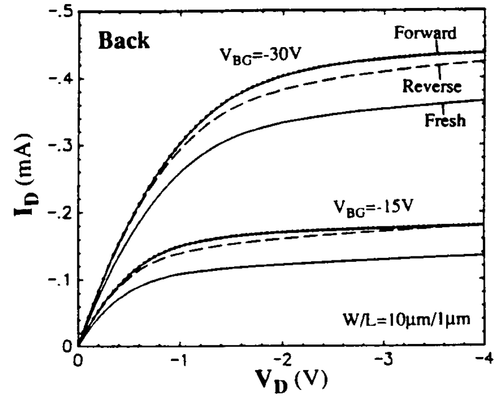

Fig.4 Back gate drain current before and after front channel hot-electron stressing.

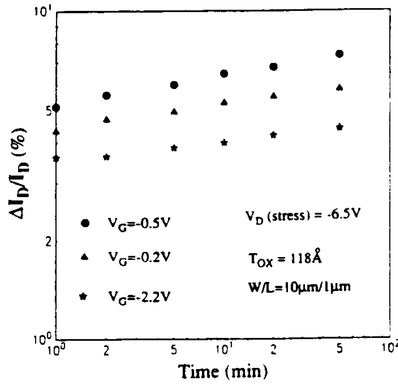

Fig.5 Drain current $\Delta I_D/I_D$ degradation as a function of stress time T_{STRESS}.

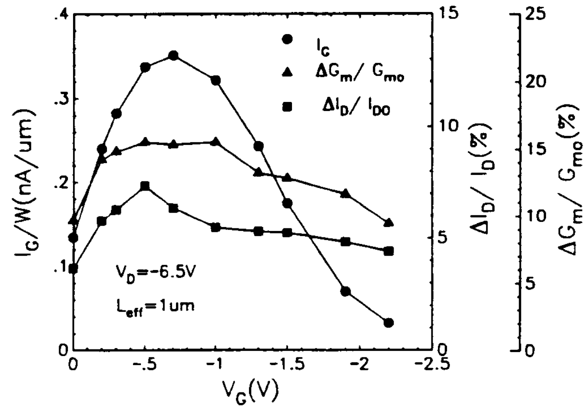

Fig.6 Correlation between I_G/W, degradation $\Delta I_D/I_D$ and $\Delta G_m/G_{mo}$.