

Characterizing a Single Hot-Electron-Induced Trap in Submicron MOSFET Using Random Telegraph Noise

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Summary

Individual interface traps generated by hot electron stress are observed for the first time. Single trap filling and emptying can cause 0.1% step noise in I_d due to coulombic scattering. Trap location (3-10 Å from interface), time constant, energy and escape frequency are found to be very different from pre-stress (process-induced) traps.

Noise due to a Single Interface Trap

The deep-submicron devices used in this study were fabricated using a photoresist-ashing technique [1]. The oxide thickness is 8.6nm and substrate doping density is $5 \times 10^{17} \text{cm}^{-3}$. The drain current fluctuation at room temperature were recorded by an HP3651A spectrum analyzer. The details of the measurement system can be found in reference [2]. Fig.1a shows the typical current fluctuation of a deep submicron n-MOSFET with $W_{\text{eff}} = 0.5 \mu\text{m}$, $L_{\text{eff}} = 0.35 \mu\text{m}$. The striking two-level current fluctuation is due to the filling and emptying of a single interface trap. It is known as the Random Telegraph Noise (RTS) and is observed only when the channel area is small enough to contain only one trap within kT 's from the fermi level.

Fig.1b shows the current noise after hot electron stress at $V_g = 2\text{V}$, $V_d = 4.5\text{V}$, $I_{\text{sub}} = 10 \mu\text{A}$ for 10 minutes. One can observe new short pulses superimposed on the original RTS noise. Fig.1c is a portion of Fig.1b in expanded time scale. Clearly the short pulses in Fig.1b is a new set of RTS due to a single hot-electron-induced trap. This is the first observation of a single hot-electron generated interface trap.

Trap Time Constant

The noise spectrum after stress is a Lorentzian spectrum with the -3db frequency at 15 Hz in Fig.2a. In the time-domain waveform shown in Fig. 2b, the time-in-high-current-level, τ_H is simply the time when trap is empty (the capture time, τ_c). Similarly the time-in-low-current-level, τ_L , is the time when the trap is filled (the emission time, τ_e). Statistical measurement of τ_H and τ_L [2] reveals two exponential distributions, as expected of Poisson processes. The two time constants are τ_c and τ_e . We found $\tau_c^{-1} + \tau_e^{-1} = 0.1/\text{ms}$. This is in excellent agreement with the corner frequency in Fig. 2a, which should be equal to $(\tau_c^{-1} + \tau_e^{-1})/2\pi$.

Table 1 list the time-constants of hot electron-induced interface trap and process-induced, i.e. pre-stress, interface traps. The former are about 50 times shorter than the later. One may wonder if hot electron stress also generate traps with large τ 's but the RTS due to them is masked by the pre-stress RTS with similar τ 's. Table 1 indicates that RTS is almost never observed in pre-stress MOSFET with channel area larger than $0.7 \times 0.7 \mu\text{m}^2$ while it is easily observed in stressed MOSFET of $1 \times 1 \mu\text{m}^2$ and above due to the small stressed area. In those cases, the hot electron stress obviously did not generate traps with large τ 's.

Distance between Trap and Interface

The ratio τ_c / τ_e is related to $E_T - E_F$, the trap energy relative to fermi energy level and degeneracy factor, g

$$\frac{\tau_c}{\tau_e} = \frac{\langle \tau_H \rangle}{\langle \tau_L \rangle} = g e^{(E_T - E_F)/kT} \approx g e^{-\frac{(E_{\text{cox}} - E_T - 3.2 + \frac{z}{T_{\text{ox}}})qV_g}{kT}} \quad (1)$$

where E_{cox} is the oxide conduction band energy, V_g is the gate voltage, T_{ox} is the gate oxide thickness, and z is the distance between the trap and the interface (see inset of Fig.4). The trap to interface distance can be found from the slope of $\ln(\tau_c/\tau_e)$ versus V_g plot as shown in Fig.3. The last step of Eq. (1) assumes that the fermi level at the surface of the substrate coincide with the Silicon conduction band edge for simplicity. The curve in Fig.3 did not use this approximation and therefore is not a straight line.

Table 1 shows that the hot-electron-stress-induced traps are 3 to 10 Å from the interface while process-induced traps in these devices are 10 to 20 Å from the interface.

Tunneling as Capture/Emission Mechanism

It is well known that electron capture and emission through tunneling should obey the following relationship between z and and the time constant, τ

$$\tau = \frac{1}{\nu} \exp\left(z \frac{4\pi}{h} \sqrt{2m^* \phi}\right) \quad (2)$$

The linear relationship between $\ln\tau$ and z is indeed verified in Fig.4 with a slope of $0.78/\text{Å}$ which is in agreement with Eq. (2) if $m^* = 0.2 m_0$ and $\phi = 3 \text{ eV}$. Also in Fig.4 we note that the process-induced traps have a much lower escape frequency ν , suggesting that the two kinds of traps might have different microstructures.

Trap Influence on Drain Current

It can be shown that the magnitude of the RTS step height is

$$\frac{\Delta I_d}{I_d} = -\frac{q}{C_{\text{ox}}(V_g - V_T)WL} + \frac{\Delta\mu}{\mu} \frac{\Delta A}{WL} \quad (3)$$

The first term is due to the modulation of channel carrier numbers and the second is due to the coulombic scattering from the charged trap, where ΔA is the channel area over which trap scattering is significant. In Fig.5, the process-induced trap produced 0.05% of $\Delta I_d/I_d$. The first term, i.e. carrier number fluctuation only account for 0.02%. So, mobility fluctuation due to the trap scattering account for 0.03%. In the case of the stress-induced trap, mobility fluctuation contributes a dominant 0.09% for a total of 0.11% in the linear region. The large mobility fluctuation of the stress-induced trap is to be expected in light of its closer proximity to the interface, i.e. smaller z .

Finally, the inset of Fig.5 shows that the well known decrease in the DC $\Delta I_d/I_d$ is due to reduced RTS step height. It can be explained by the deeper subsurface electron path at higher V_d [3].

Conclusions

RTS noise can be a useful tool for studying stress-induced interface traps. It is more easily observable for stress induced traps than process-induced traps due to the small stress area and low stress-induced trap density after light stressing. Using RTS as a characterization tool, we found the stress-induced trap to be located closer to the interface, and therefore have a shorter time constant and much stronger influence on scattering and ΔI_d than process-induced traps. One should note that RTS only reveals those traps near the fermi level, while the DC MOSFET IV degra-

ation is also influenced by all the charged traps. Finally close examination of Fig.2b suggests that there may be faster traps in addition to those studied here.

Acknowledgment

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References

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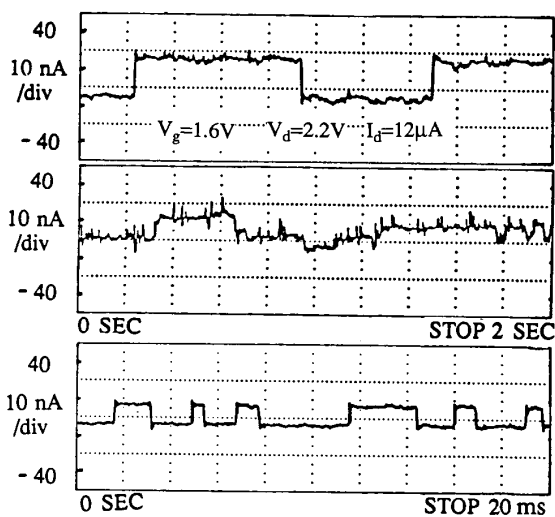


Fig.1 a) a typical pre-stress RTS. b) a post-stress RTS with small peaks. c) expanded time scale of b) shows the small peaks are RTS with shorter time constant.

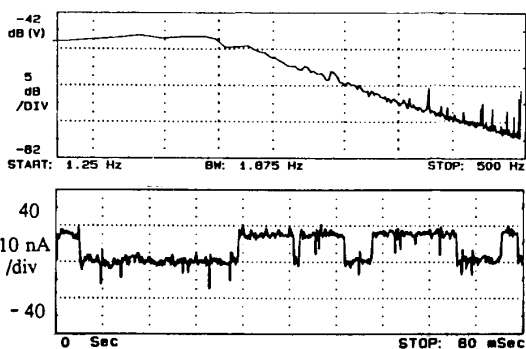


Fig.2 a) a single Lorentzian with -3db frequency about 15 Hz. b) the corresponding RTS with 10ms time constant τ .

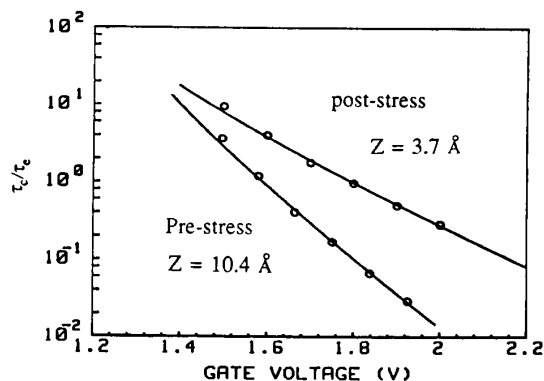


Fig.3 pre-stress and post-stress τ_c/τ_e versus V_g . z can be extracted from this plot.

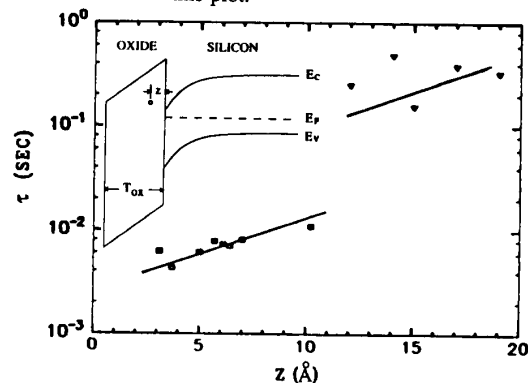


Fig.4 τ versus z for the pre-stress and post-stress RTS.

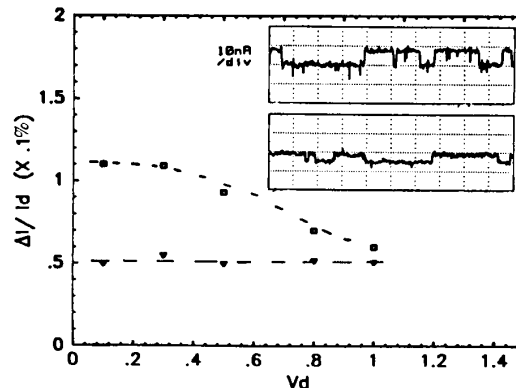


Fig.5 pre- and post-stress $\Delta I/I_d$ from linear to saturation region. The noise magnitudes of post-stress RTS decreased as V_d approaching saturation. The upper insert is the post-stress RTS in linear region; the lower, in the saturation region.

Table I: Hot electron-induced and process-induced trap parameters.

W / L ($\mu\text{m} / \mu\text{m}$)	Pre-stress		Post-stress		
	T (ms)	Z (\AA)	T (ms)	Z (\AA)	$E_{\text{cox}} - E_T$ (eV)
0.5 / 0.5	257	12	6.1	5.0	3.236
0.5 / 0.35	457	14	7.0	6.4	3.227
0.7 / 0.7	*	*	4.3	3.7	3.296
0.8 / 0.5	330	19	7.3	6.1	3.259
1.0 / 1.0	*	*	8.1	7.0	3.258