

A DEEP-SUBMICROMETER MOSFET MODEL FOR ANALOG/DIGITAL CIRCUIT SIMULATIONS

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ABSTRACT

An accurate drain current model for deep-submicrometer MOSFETs down to $L_{\text{eff}} = 0.25\mu\text{m}$ suitable for digital as well as analog applications has been developed. The basic framework of this model is based on the recent improved physical understanding of deep-submicron MOS devices. In developing this new model, meticulous care has been taken in retaining the basic functional form of fully physical models while improving model accuracy and computational efficiency. The ease of parameter extraction was also a major consideration. In addition to the effects commonly included in the MOSFET current equation, it is found that the inversion-layer capacitance effect, hot-electron induced output resistance degradation, and source/drain parasitic resistance effect are also important factors to consider in deep-submicrometer MOSFET modeling.

INTRODUCTION

Recent advances in process technology [1-4] have made deep-submicrometer MOSFETs potential candidates for next generation ULSI designs. It has been shown that properly designed deep-submicrometer devices show device characteristics similar to those of their near-micron counterparts [5-7], but significant second-order effects due to the once negligible physical phenomena make existing drain current models unsatisfactory. Since the device characteristics of such small geometry are highly sensitive to device parameters, optimal circuit designs become even more difficult to create than before. Therefore, an accurate and computationally efficient drain current model for deep-submicrometer MOSFETs are extremely crucial and indispensable in developing future ULSI systems. Furthermore, many of the drain current models used in circuit simulations are inadequate in modeling the output resistance and the weak inversion characteristics, which are very important for analog applications. One purpose of this work is to bridge the gap between deep-submicrometer devices and circuit simulation with an emphasis on analog behavior, a consideration that was lacking before.

THE MODEL

Recent studies have indicated that the basic physics involved in MOSFET is independent of device size [5], therefore, the basic functional forms of many existing drain current models can still be kept. Eq. 1 is one of the popular drain current models used in the literature.

Triode Region:

$$I_{\text{DS}} = \frac{\beta_0 (V_{\text{GS}} - V_{\text{th}} - \frac{a}{2} V_{\text{DS}}) V_{\text{DS}}}{1 + \theta (V_{\text{GS}} - V_{\text{th}}) + (V_{\text{DS}}/E_c L)} \quad (1a)$$

Saturation Region:

$$I_{\text{DSAT}} = \frac{\beta_0 (V_{\text{GS}} - V_{\text{th}})^2}{[1 + \theta (V_{\text{GS}} - V_{\text{th}})] (2aK)} \quad (1b)$$

Subthreshold Region:

$$I_{\text{subth}} = \beta_0 (V_{\text{in}})^2 e^{\frac{(V_{\text{GS}} - V_{\text{th}} - V_{\text{of}})}{mV_{\text{tm}}}} \left[1 - e^{\frac{-V_{\text{DS}}}{V_{\text{tm}}}} \right] \quad (1c)$$

where β_0 is the conductance coefficient, E_c is the critical field, L is the effective channel length, θ is the mobility degradation coefficient, a accounts for the body effect, V_{tm} is the thermal voltage, m is the subthreshold swing coefficient, V_{of} is a fitting parameter, and K can be derived by equating the drain current and its derivatives at drain saturation voltage (V_{DSAT}). To make Eq. 1 suitable for digital and analog applications and accurate down to the deep-submicrometer regime, the following effects have to be included or modified: velocity saturation, mobility degradation due to vertical field, source/drain resistance, inversion-layer capacitance, channel length modulation, and hot-electron induced output resistance degradation. In addition to the high accuracy and computational efficiency, a useful model should also be developed for ease of parameter extraction. The equations used in this model are chosen to observe the above considerations.

Velocity Saturation: The accuracy of a drain current model is directly affected by how the velocity saturation effect is implemented, especially for deep-submicrometer devices. The most commonly used carrier velocity model is (2), because it leads to simple analytical drain current equations.

$$v = \frac{\mu}{1 + (E/E_c)} \quad (2)$$

where $E_c = E_{c0} \equiv v_{\text{sat}}/\mu$ and v_{sat} is the carrier saturation velocity. However, Eq. 2 underestimates the carrier velocity in the low field region (see curve 1 in Fig. 1). An improved mobility model is the "two-section" model [8], which uses $E_c = 2E_{c0}$ in the low-field region and sets $v = v_{\text{sat}}$ when $E > 2E_{c0}$ (curve 2 in Fig. 1). But this model causes discontinuity in the derivatives of the drain current equation at V_{DSAT} . To retain the high accuracy and avoid the discontinuity problem, a compromised solution is (3), where the critical field smoothly changes from $2E_{c0}$ in the low field region to E_{c0} at $V_{\text{DS}} = V_{\text{DSAT}}$ (curve 3 in Fig. 1).

$$E_c = E_{c0} \left[1 + \frac{(V_{\text{DS}} - V_{\text{DSAT}})^2}{V_{\text{DSAT}}^2} \right] \quad V_{\text{DS}} \leq V_{\text{DSAT}}$$

$$= E_{c0} \quad V_{\text{DS}} > V_{\text{DSAT}} \quad (3)$$

The quadratic function is used in (3) to keep the first and second derivatives of the drain current equation continuous at V_{DSAT} .

Mobility Degradation: It has been shown that a universal relationship, Eq. 4, exists between the mobility and the vertical electric field [9] over a wide range of oxide thickness and channel doping concentration.

$$\mu = \frac{\mu_0}{1 + (E_{\text{eff}}/E_0)^n} \quad (4)$$

where E_{eff} is the average vertical electrical field in the inversion layer defined in [9]. E_0 and n are constants. However, Eq. 4 is seldom used in circuit simulations due to its undesirable functional form. A widely used expression to account for the mobility degradation is (5a), which can be considered as a first order expansion of (4).

$$\mu = \frac{\mu_0}{1 + \theta (V_{\text{GS}} - V_{\text{th}})} \quad (5a)$$

But for deep-submicrometer devices, which usually have thin gate oxides, Eq. 5a starts to deviate from (4) when the vertical field is high. This can be seen in Fig. 2. Therefore, higher order terms have to be included in (5a). It is found experimentally that the inclusion of the second-order term is adequate under normal bias conditions.

$$\mu = \frac{\mu_0}{1 + \theta (V_{\text{GS}} - V_{\text{th}}) + \theta_1 (V_{\text{GS}} - V_{\text{th}})^2} \quad (5b)$$

Source/Drain Resistance: To eliminate the need for extra elements in circuit simulations, the source/drain resistance effect is lumped in the model. In fact, it can be shown [10] that the source/drain resistance effect can not be separated from the velocity saturation and mobility degradation effects. Therefore, when parameters of (4) and (5b) are extracted, the source/drain parasitic resistance effect is automatically included in this model.

Inversion-Layer Capacitance: Including the inversion-layer capacitance, the effective gate capacitance is

$$C'_{\text{ox}} = \frac{dQ_n}{dV_{\text{GS}}} = \frac{C_{\text{ox}} C_{\text{inv}}}{C_{\text{ox}} + C_{\text{inv}}} \quad (6)$$

where

$$C_{\text{inv}} \approx C_d e^{\frac{V_{\text{GS}} - V_{\text{th}}}{m V_{\text{tm}}}} \quad (7)$$

and C_d is the depletion-layer capacitance [11]. Although the drain current equations in both strong and subthreshold regions can be derived, there is no simple analytical expression for the drain current near the threshold voltage, where C_{ox} and C_{inv} are equally important. The inversion-layer capacitance effect is more severe for deep-submicrometer devices because of the thin gate oxides [12] as can be seen in Fig 3, where the calculated inversion charge density is plotted against gate voltage. The deviation of the inversion charge from its linear approximation, $C_{\text{ox}}(V_{\text{GS}} - V_{\text{th}})$, near the threshold voltage increases as the oxide thickness decreases. In this model, a transition region between weak and strong-inversion is determined, taking into account the effect of C_{inv} . A cubic spline function in V_{GS} is then created for this transition region.

$$V'_{\text{GS}} = C_0 + C_1 V_{\text{GS}} + C_2 V_{\text{GS}}^2 + C_3 V_{\text{GS}}^3 \quad (8)$$

The upper and lower bounds of the cubic spline function is determined by the relative magnitude of C_{ox} and C_{inv} . For example, the upper (lower) bound can be set at which $C_{\text{inv}} = 100 C_{\text{ox}}$ ($C_{\text{ox}} = 100 C_{\text{inv}}$). Therefore,

$$V_{\text{upper}} = V_{\text{th}} + m V_{\text{tm}} \ln\left(\frac{100 C_{\text{ox}}}{C_d}\right) \quad (9a)$$

$$V_{\text{lower}} = V_{\text{th}} + m V_{\text{tm}} \ln\left(\frac{C_{\text{ox}}}{100 C_d}\right) \quad (9b)$$

The boundary conditions are chosen such that the drain current and its first derivative are continuous at the upper and lower bounds.

Boundary Conditions:

$$\begin{aligned} V'_{\text{GS}} &= V_{\text{upper}} \\ \frac{dV'_{\text{GS}}}{dV_{\text{GS}}} &= 1 \end{aligned} \quad (10)$$

and

$$\begin{aligned} V'_{\text{GS}} &= \sqrt{2aK} V_{\text{tm}} e^{\frac{V_{\text{lower}} - V_{\text{of}}}{2mV_{\text{tm}}}} \\ \frac{dV'_{\text{GS}}}{dV_{\text{GS}}} &= \frac{V_{\text{lower}}}{2mV_{\text{tm}}} \end{aligned} \quad (11)$$

This approach avoids the sophisticated physics involved and increases the computational efficiency. This cubic spline function also serves as a means to acquire a smooth transition from the subthreshold region to the strong-inversion region.

Channel Length Modulation: Basic physical modeling indicated that the output resistance exhibits a logarithmic dependence on drain voltage [10] near V_{DSAT} . In practice, however, it is found that a combination of the hyperbolic tangent function and the linear function, Eq. 9, is needed to model the output resistance correctly in this region and to discontinuity problem at V_{DSAT} .

$$\beta_0 = \beta_{0\text{lin}} + \beta_1 \tanh\left(\frac{\beta_2 V_{\text{DS}}}{V_{\text{DSAT}}}\right) + \beta_3 V_{\text{DS}} \quad (12)$$

where $\beta_{0\text{lin}}$ is the conductance coefficient extracted in the triode region, β_1 , β_2 , and β_3 are fitting parameters. This formulation also improves the computational efficiency.

Hot-Electron Induced Output Resistance Degradation: Since the substrate current is the origin of the output resistance degradation, this hot-electron effect is implemented through (10). The second term on the right hand side has the same form as that of substrate current.

$$I'_{\text{DSAT}} = I_{\text{DSAT}} \left[1 + A_1 e^{\frac{-B_1}{(V_{\text{DS}} - V_{\text{DSAT}})}} \right] \quad (13)$$

where A_1 and B_1 have the physical meaning of impact ionization coefficient.

RESULTS

The devices used in this study were fabricated using an NMOS (PMOS) technology with a photoresist-ashing technique to defined the ultra-fine gates [4]. P⁺-poly gate is used for p-channel devices. Since the model is developed for ease of parameter extraction, the extraction procedure is very simple and efficient. Linear-least-square fit is the only optimization algorithm needed. Some parameters are slightly body-bias dependent and are approximated by linear functions. The major features of this model is listed in Table I.

All data presented in this section were taken from devices with $W_{\text{eff}} = 10 \mu\text{m}$, $L_{\text{eff}} = 0.25 \mu\text{m}$, $T_{\text{ox}} = 86$ angstrom for n-channel, and $W_{\text{eff}} = 5 \mu\text{m}$, $L_{\text{eff}} = 0.4 \mu\text{m}$, $T_{\text{ox}} = 75$ angstrom for p-channel. Fig. 4 shows the calculated and the measured $I_{\text{DS}} - V_{\text{GS}}$ characteristics in the triode region for an n-channel device. The dashed line in Fig. 4 is the best fit if (5a) is used exemplifying the importance of the second-order term in (5b). The $I_{\text{DS}} - V_{\text{GS}}$ characteristics in the saturation region for the same device is shown in Fig. 5. The subthreshold characteristics is shown in Fig. 6. Region B for $V_{\text{BS}} = 0\text{V}$ was calculated from the cubic spline function. The drain current changes smoothly from the subthreshold region (region A) to the strong-inversion region (region C). Similar results are also obtained for p-channel devices. Figure 7a and 7b show the measured and calculated $I_{\text{DS}} - V_{\text{DS}}$ characteristics of both types of devices, and their corresponding output resistances are shown in Fig. 8a and 8b, respectively. The close resemblance between the calculated and measured output resistance verifies the use of (12) and (13) in

this model.

CONCLUSION

Based on the improved physical understanding of deep-submicrometer devices, a drain current model, which is accurate down to quarter-micron channel length and suitable for both digital and analog applications, is developed. The basic functional form of fully physical models is retained while important physical phenomena are implemented through a semi-empirical approach to achieve high accuracy, high computational efficiency, and ease of parameter extraction. All these properties make the model very useful in developing future ULSI systems.

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TABLE I Major Features	
Minimum oxide thickness	≈ 3.6nm
Minimum channel length	≈ 0.2μm
Analog capability	yes
Subthreshold to strong-inversion transition	Drain current and its first derivative are continuous
Triode to saturation region transition	Drain current and its first and second derivatives are continuous

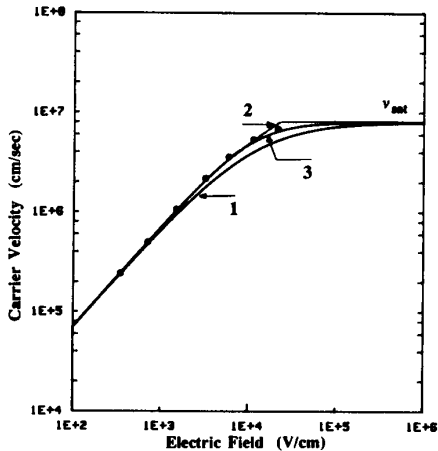


Fig. 1 The electron velocity versus horizontal electric field. The dots are measured data [8]. Curve 1 is the model in (2); curve 2 is the two-section model; and curve 3 is the proposed model.

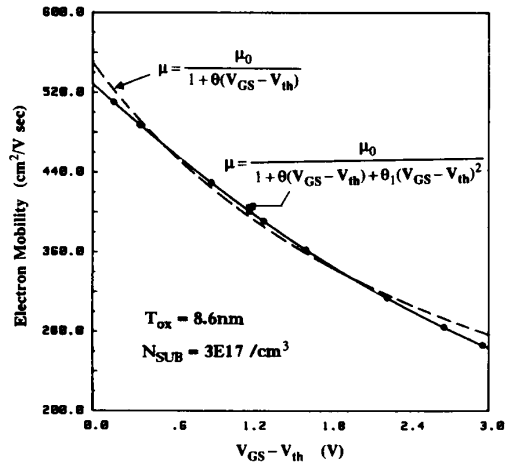


Fig. 2 The electron mobility versus gate voltage. The dots are measured data [9]. The dashed line is the first-order model. The solid line is the proposed model.

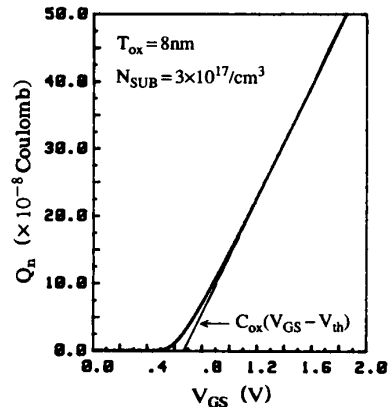


Fig. 3 The inversion charge density versus gate voltage. The inversion charge density was calculated from numerical analysis. The straight line is its linear approximation.

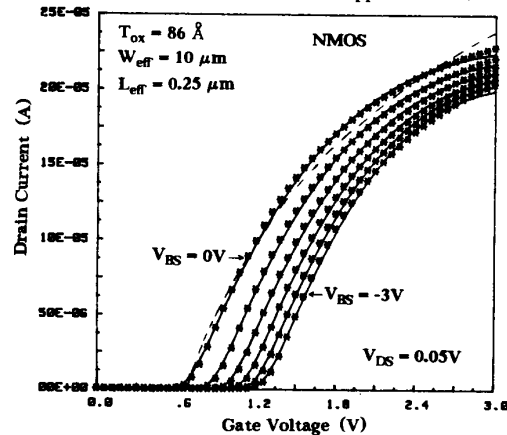


Fig. 4 Measured and simulated $I_{DS} - V_{GS}$ characteristics in the triode region. Solid lines are the model and the asterisks are measured data. The dashed line is the best fit for $V_{BS} = 0V$ if (5a) is used.

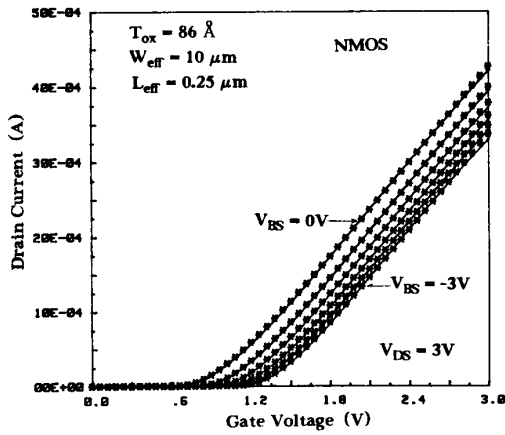


Fig. 5 Measured and simulated $I_{DS} - V_{GS}$ characteristics in the saturation region. Solid lines are the model and the asterisks are measured data.

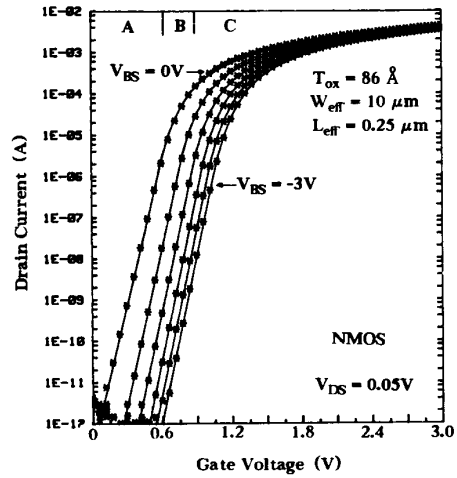


Fig. 6 The subthreshold characteristics. The current in region B for $V_{BS} = 0V$ was calculated from the cubic spline function.

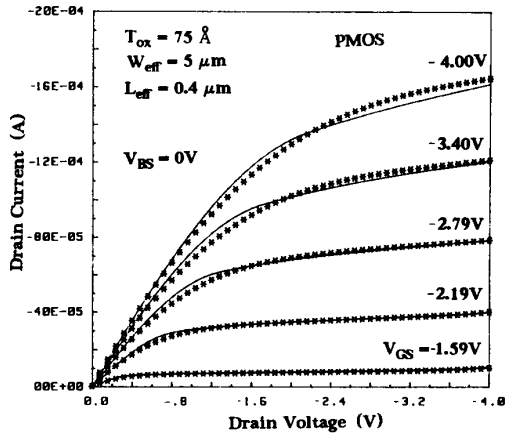
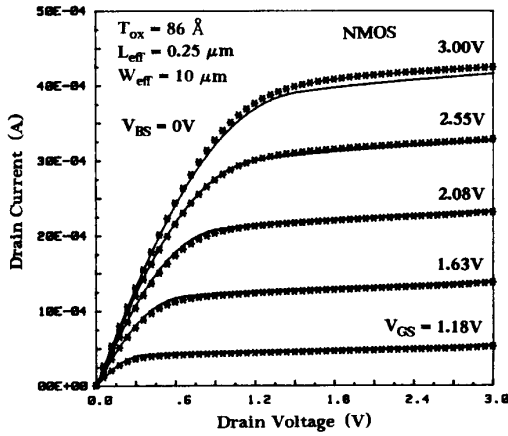


Fig. 7 The $I_{DS} - V_{DS}$ characteristics. Solid lines are the model and asterisks are measured data. (a) n-channel, (b) p-channel.

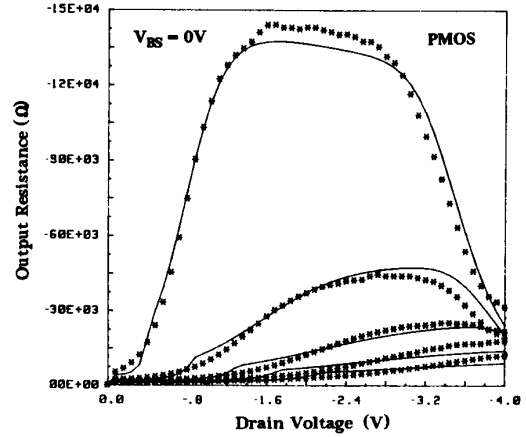
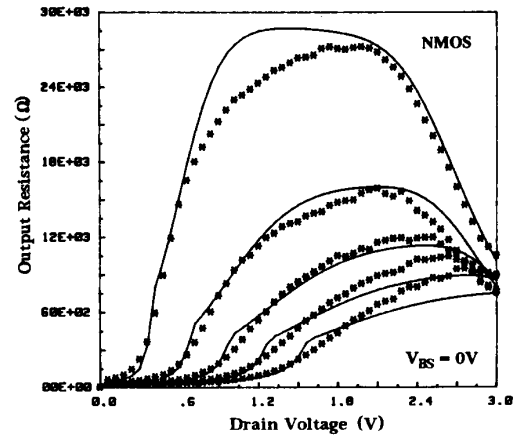


Fig. 8 The output resistances of the devices shown in Fig. 7. Solid lines are the model and asterisks are measured data. The biasing conditions are the same as those in Fig. 7. (a) n-channel, (b) p-channel.