Hot-Electron-Induced Traps Studied Through the Random Telegraph Noise

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Abstract—**Random telegraph signal (RTS) measurements have been used to study individual hot-carrier-induced trap in nMOSFET's. Single-trap filling and emptying can cause 0.1% step noise in channel current. Trap location (3–10 Å from interface), time constant (~10 ms), and energy are found to be quite different from those of prestress (process-induced) traps. The type (acceptor or donor) of the traps can also be identified by RTS measurements; both the process and stress-induced traps with energies near the conduction band edge are found to be of the acceptor type for nMOSFET's and trap levels near the valence band edge are found to be of the donor type for pMOSFET's.**

I. Hot-Carrier Induced RTS

The influence of hot-carrier injection on the performance of MOS transistors has been studied extensively during the last decade. The recent development of random telegraph signal (RTS) measurement offers a sensitive tool that may reveal some unexplored aspects of interface traps by studying the trapping–detrapping process of individual traps [1]–[3].

The deep-submicrometer MOSFET's used in this study were fabricated using a photoresist-ashing technique [4]. The oxide thickness is 8.6 nm and substrate doping density is 5×10^{17} cm^{-3}. The drain current fluctuations at room temperature were recorded by an HP3651A spectrum analyzer. Details of the measurement system can be found in [5]. Fig. 1(a) shows the typical current fluctuation of an nMOSFET with $W_{\text{eff}} = 0.5$ μm and $L_{\text{eff}} = 0.35$ μm. The striking two-level current fluctuation is due to the filling and emptying of a single interface trap. It is known as random telegraph noise, which is observed only when the channel area is small enough to contain only one trap within kT's from the surface Fermi level. Fig. 1(b) shows the current noise after 10 min of channel hot-electron stressing at $V_g = 2$ V, $V_d = 4.5$ V, and $I_{sub} = 10$ μA. New short pulses superimposing on the original RTS are observed. Fig. 1(c) is a portion of Fig. 1(b) in expanded time scale. Clearly the shorter pulse in Fig. 1(b) is the signature of a newly generated trap. This is the first direct observation of a single hot-electron-generated interface trap.

Manuscript received January 5, 1991. This work was supported by JSEP under Contract F49620-84-C-0057 and by ISTO/SDIO through ONR under Contract N00014-85-K-0603.

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IEEE Log Number 9100356.

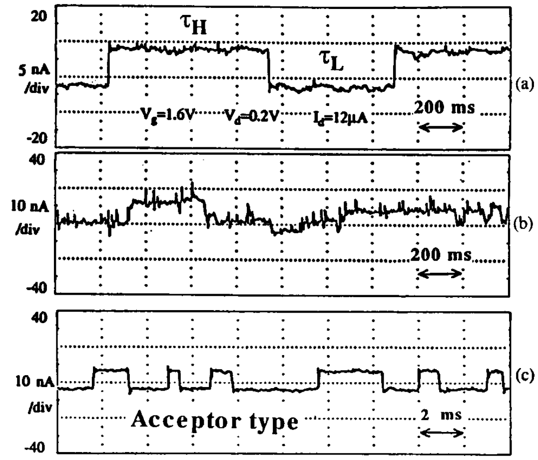

Fig. 1. (a) A typical process-induced RTS. (b) After hot-electron stress, small peaks superimposing on the prestress RTS are observed. (c) Expanded time scale of (b) shows the small peaks are an additional set of RTS with shorter time constant.

II. Trap Capture and Emission Time Constants

Referring to Fig. 1, the high-current-level time τ_H is the time when the trap is empty (equal to the capture time τ_c), whereas the low-current-level time τ_L is the time when the trap is filled (equal to the emission time τ_e). Statistical measurement of τ_H and τ_L reveals two exponential distributions, as expected from theory of trapping and detrapping [5]. The stress-induced RTS exhibits a Lorentzian spectrum in the frequency domain with a corner frequency in excellent agreement with the expecting value of $(\tau_c^{-1} + \tau_e^{-1})/2\pi$.

Table I lists the time constants $(\tau_c^{-1} + \tau_e^{-1})^{-1}$ of the process- and stress-induced interface traps measured at strong inversion. In general, the time constant of the stress-induced traps are much shorter than those of process-induced traps. One may conclude that hot-carrier-induced traps are located closer to the Si–SiO_2 interface, resulting in shorter time constants. Table I reveals that some transistors with larger channel area only exhibit stress-induced RTS but not prestress RTS. This may be explained by the different nature (energy level, location, etc.) of the two types of traps. It should be remarked that hot-electron stressing may also

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TABLE I
TIME CONSTANT (τ), LOCATION (Z), AND ENERGY OF PROCESS- AND STRESS-INDUCED TRAPS

W/L (μm/μm)	Process-induced τ (ms)	Process-induced Z (Å)	Stress-induced τ (ms)	Stress-induced Z (Å)	Stress-induced $E_{cox} - E_T$ (eV)
0.5/0.5	257	12	6.1	5.0	3.236
0.5/0.35	457	14	7.0	6.4	3.227
0.7/0.7	*	*	4.3	3.7	3.296
0.8/0.5	330	19	7.3	6.1	3.259
1.0/1.0	*	*	8.1	7.0	3.258

*E_{cox} is the energy of conduction band edge.

generate traps with longer time constants, although they were not observed in our samples and measurement technique.

III. Trap Location and Energy Level

It can be shown that the gate-bias dependence of the ratio τ_c/τ_e is given by [1]–[3]

$$\frac{\langle\tau_c\rangle}{\langle\tau_e\rangle} = \frac{1-f_t}{f_t} \approx De^{(E_T-E_F)/kT} \tag{1}$$

where f_t is the trap occupancy function and $E_T - E_F$ is the trap energy level relative to the Fermi level. The pre-exponential factor D is a function of the degeneracy factor and ionization entropies of the trap [1]. In strong inversion D is a weak function of the gate bias and hence one may use (1) to extract the trap-to-interface distance (Z) from the slope of the ln $\langle\tau_c\rangle/\langle\tau_e\rangle$ versus V_g plot [2]. Such a plot is shown in Fig. 2. As shown in Table I the stress-induced traps are located within 10 Å from the interface while the process-induced traps can be as far as 20 Å from the interface.

IV. Trap Influence on Drain Current

The magnitude of the RTS step can be written as

$$\frac{\Delta I_d}{I_d} = -\frac{q}{C_{ox}(V_g - V_T)WL} + \frac{\Delta\mu}{\mu}\frac{\Delta A}{WL}. \tag{2}$$

The first term is due to the modulation of channel carrier numbers whereas the second term is due to the coulombic scattering from the charged trap. Here ΔA is the channel area over which trap scattering is significant. All the quantities in (2) are measurable except for $\Delta\mu\Delta A$. A theory evaluation of $\Delta\mu\Delta A$ requires knowledge of the scattering and screening effects [2]. Nevertheless (2) does provide a means to separate the contributions of carrier number and mobility fluctuations to the drain current fluctuation. In Fig. 3, the process-induced trap produces 0.05% of $\Delta I_d/I_d$ at $V_g - V_T = 1.2$ V. The carrier number fluctuation only accounts for 0.02% while the remaining 0.03% is attributed to trap scattering. In the case of the stress-induced RTS, trap scattering contributes a dominant portion 0.09% over the total $\Delta I_d/I_d$ of 0.11% in the linear region. The large mobility fluctuation induced by the stress-induced trap is to be expected in light of their much closer proximity to the interface [2].

V. Acceptor-Type Trap

RTS measurement provides an unambiguous means to distinguish the type of the traps. By definition an acceptor

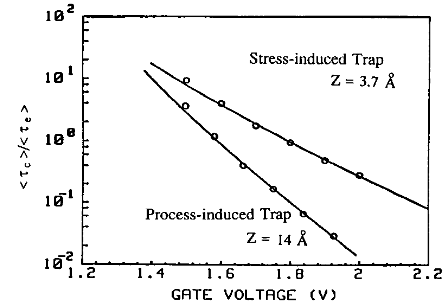

Fig. 2. $\langle\tau_c\rangle/\langle\tau_e\rangle$ of process-induced and stress-induced traps versus gate bias. The trap location Z can be determined from this plot. The lines are theoretical fitting based on (1).

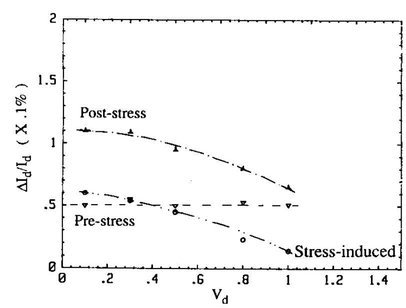

Fig. 3. Pre- and post-stress $\Delta I/I_d$ from linear to saturation regions. $W_{\text{eff}} = 0.7$ μm, $L_{\text{eff}} = 0.35$ μm, $V_g - V_T = 1.2$ V. The noise magnitudes of post-stress RTS decreased as V_d approaching saturation. The stress-induced portion is the difference of the magnitudes of post- and prestress $\Delta I_d/I_d$.

trap is neutral when it is empty and negatively charged when it is filled; a donor-type trap is positively charged when it is empty and neutral when it is filled. The type of a trap can be determined from RTS with the following arguments. From (2) one may notice that at strong inversion the drain current fluctuation is dominated by the trap-induced mobility fluctuation. Thus at strong inversion the high-current state (τ_c) corresponds to a trap at neutral state and the low-current state (τ_e) corresponds to a trap at charged state. We then have to determine whether the charged state is filled or empty. These two situations can be readily distinguished by comparison of the gate-bias dependence of $\langle\tau_c\rangle/\langle\tau_e\rangle$ obtained from the experimental results with that predicted by (1). For both process- and stress-induced traps, we found that $\langle\tau_c\rangle/\langle\tau_e\rangle$ *decreases* with increasing gate bias and agreed very well with that predicted by (1) as shown in Fig. 2. Such a bias dependence verified that τ_c corresponds to an empty trap and τ_e corresponds to a filled trap as implied by (1). Knowing that the filled trap is the charged state we can conclude that the traps are of the acceptor type. Following the same arguments we also found the traps near the valence band in pMOS FET's are of the donor type.

VI. Conclusion

Using RTS as a characterization tool, we found that the stress-induced interface traps are located closer to the interface, resulting in shorter time constants and a stronger influence on the surface mobility than the process-induced traps. A method for unambiguously distinguishing the trap types based on RTS measurements has been proposed. The traps close to the conduction band edge are identified to be acceptor type for nMOSFET's and donor type for pMOSFET's.

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