

Improvement of Charge Trapping Characteristics of N₂O-Annealed and Reoxidized N₂O-Annealed Thin Oxides

Zhihong Liu, *Member, IEEE*, Hsing-jen Wann, Ping K. Ko, *Member, IEEE*, Chenming Hu, *Fellow, IEEE*, and Yiu Chung Cheng, *Senior Member, IEEE*

Abstract—It is found that increasing N₂O annealing temperature and time monotonically reduces electron trapping in the resulting oxides. The improvement increases with oxide thickness. Reoxidation does not enhance but reduces the improvement. The behavior is different from and simpler to understand than that after NH₃ annealing, apparently due to the absence of deleterious hydrogen. Hole trapping and interface trap generation are also suppressed by N₂O annealing, though an optimum anneal condition may exist. Charge to breakdown exhibits modest improvement consistent with reduced electron trapping.

THE use of N₂O as an oxidant or a post-oxidation annealing ambient has attracted much attention recently [1]–[3]. Comparing direct oxidation of silicon in N₂O with annealing pregrown oxides in N₂O, we conclude that the latter is more promising because oxide growth in pure N₂O is self-limited to less than 50 Å under normal processing conditions (e.g., 950°C, 40 min). To increase the oxide thickness, high oxidation temperature and extended oxidation time are required. However, high-temperature processing steps are not preferable for future technologies. When N₂O is used as a post-oxidation annealing ambient, a wide range of final oxide thicknesses is achievable [4]. Although it has been reported that N₂O-annealed gate oxides can improve the electrical stability of MOSFET's [1], [3], reliability issues for the gate dielectric such as charge trapping, interface stability, charge to breakdown Q_{bd} , as well as their process dependencies, have not been reported. In this work, electron and hole trapping and their process dependencies are evaluated. The effects of reoxidation on the N₂O-annealed oxide are also examined.

MOS capacitors were fabricated with p-type, 15–25-Ω ·

cm <100> silicon substrate in a standard four-mask polysilicon-gate process. For the gate dielectric, initial oxides were grown to 50–100 Å in dry O₂. Next, N₂O annealing was done at 900 or 950°C for 10 to 80 min in pure N₂O. Reoxidation was done in O₂ to selected samples. Determined by auger electron spectroscopy, about 0.6–1 atomic% of nitrogen (depending on the annealing time and temperature) is incorporated at the oxide/substrate interface. The final effective oxide thicknesses (using $\epsilon_{ox} = 3.9$) were determined by *CV* measurement and ranged from 75 to 123 Å. Unless otherwise specified, the gate area of the test structures is 10 μm × 10 μm.

Fig. 1 depicts the quasi-static *CV* data before and after Fowler–Nordheim (FN) stress for control, N₂O-annealed, and reoxidized N₂O-annealed oxides. Before stressing, all samples had nearly identical normalized *CV* characteristics. Interface trap generation induced by FN injection is much smaller in the N₂O-annealed devices compared with the control oxide, as indicated by the much smaller *CV* distortion. Fig. 1 also shows that the flat-band and mid-band voltage shifts after stressing are less in N₂O-annealed oxides. This suggests that the net charge trapping is lower in N₂O-annealed oxides. However, reoxidation does not further improve, as in the case of NH₃ annealing [5], [6], but degrades the interface hardness of the N₂O-annealed oxide.

In order to study the bulk charge trapping characteristics, V_g shifts during 50-mA/cm² constant current stress are monitored instead of V_{fb} shifts so that the effects of the interface trap charges are minimized [7]. The results are shown in Fig. 2 for both polarities of gate voltage. Fig. 2 shows that both the amplitude of the V_g shifts and the rate of V_g change are reduced by N₂O anneal. This suggests that the electron trap generation and trapping are reduced by N₂O anneal. Again the reoxidation step tends to increase electron trapping. Low-density (0.01 mA/cm²) constant current injection is done to study the hole trapping rate of these oxides [7]. The data are shown in Fig. 3. It appears that N₂O anneal actually modifies the hole trapping rate modestly when electrons are injected from the substrate (+ V_g injection). When electrons are injected from the gate (– V_g injection), hole trapping is

Manuscript received June 22, 1992; revised June 31, 1992. This work was supported in part by the UPGC Research Grant of Hong Kong, the Semiconductor Research Corporation, the California MICRO, and AFOSR/JSEP under Contract F49620-90-C-0029.

Z. Liu, H.-J. Wann, P. K. Ko, and C. Hu are with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720.

Y. C. Cheng is with The Directorate, City Polytechnic of Hong Kong, Hong Kong.

IEEE Log Number 9203838.

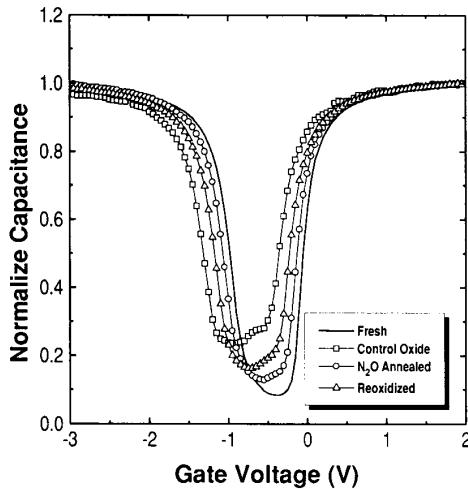


Fig. 1. Normalized quasi-static CV curves before and after 0.1-C/cm^2 $-V_g$ constant current injection ($J = 0.1\text{ mA/cm}^2$) for control, N_2O -annealed (950°C , 20 min), and reoxidized (950°C , 20-min N_2O ; 900°C , 20-min O_2) oxides. The gate area is $80\ \mu\text{m} \times 80\ \mu\text{m}$. Since the fresh CV curves for these oxides are comparable, only one set of fresh data is plotted. A comparable thickness of about 10 nm is achieved by varying the initial oxide thickness.

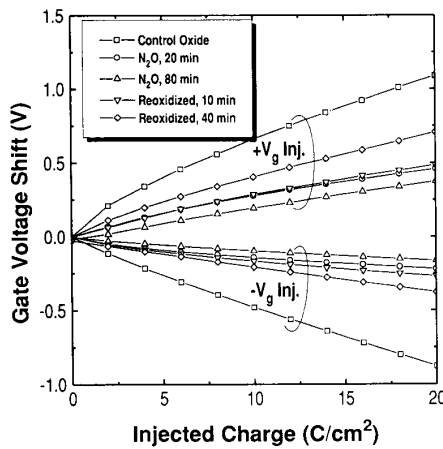


Fig. 2. Gate voltage shifts during 50-mA/cm^2 constant current injection for control ($T_{ox} = 97\ \text{\AA}$), N_2O -annealed (950°C , $T_{ox} = 91\ \text{\AA}$), and reoxidized N_2O -annealed (950°C , 20-min N_2O ; 900°C , 10- or 40-min O_2 , $T_{ox} = 96\text{--}104\ \text{\AA}$) oxides. Electrons are injected either from the gate ($-V_g$ injection) or from the substrate ($+V_g$ injection).

greatly suppressed. We speculate that this polarity-dependent hole trapping suppression is due to the presence/absence of nitrogen pileup at the oxide-substrate interface/oxide surface [1], [2]. It is worth noting that hole trapping increases when the anneal time is extended. This arises because the thickness continues increase after saturated nitrogen incorporation [4]. As expected, reoxidation also leads to increased hole trapping.

The process dependence of electron trapping is illustrated in Fig. 4. N_2O anneal significantly reduces V_g shift, and hence, electron trapping. Moreover, the effects of

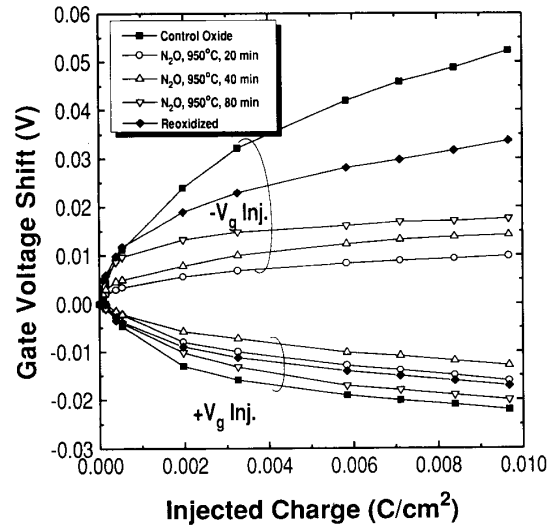


Fig. 3. Gate voltage shifts during $10\text{-}\mu\text{A/cm}^2$ constant current injection for control, N_2O -annealed, and reoxidized N_2O -annealed (950°C , 20-min N_2O ; 900°C , 20-min O_2) oxides with similar thicknesses as those used in Fig. 2.

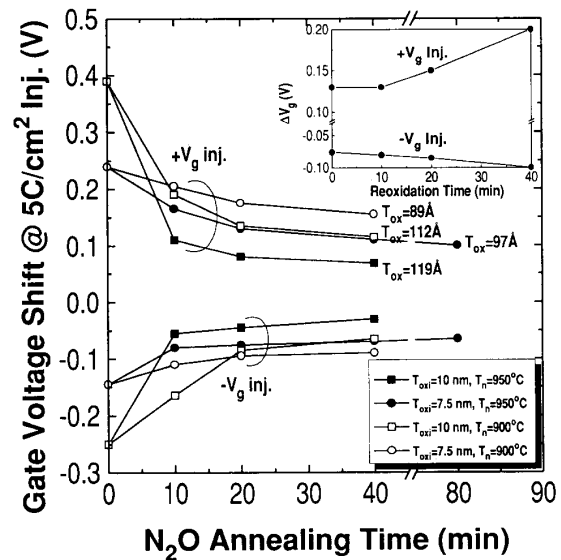


Fig. 4. Process dependence of the gate voltage shifts at 5 C/cm^2 ($J = 20\text{ mA/cm}^2$) injection. The initial (before annealed) oxide thickness T_{oxi} and the final (after annealed) oxide thickness T_{oxf} are labeled in the figure. The effects of reoxidation on gate voltage shifts for 20-min, 950°C N_2O -annealed oxide are also plotted in the inset. The temperature for reoxidation is 900°C .

N_2O anneal are more significant in thicker oxides than in thinner ones. Annealing at higher temperature and longer time produces greater benefits in the ranges studied here. Results for reoxidized N_2O -annealed devices are also shown in the same figure. No further reduction in electron trapping is achieved by the reoxidation step. Instead, it seems that the reoxidation step tends to convert the

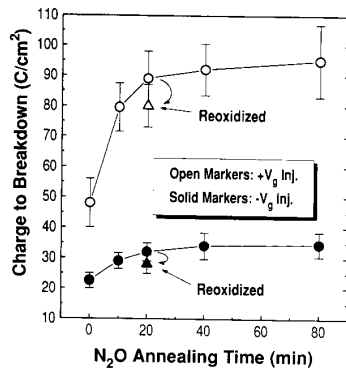


Fig. 5. Charge to breakdown Q_{bd} versus N₂O annealing time under 20-mA/cm² constant current injection. The N₂O annealing temperature is 950°C and reoxidation is performed at 900°C for 20 min. The oxide thickness is about 10 nm. Note the increase in error limits when extending annealing time.

N₂O-annealed oxide back to thermal oxide. It has been reported that reoxidation helps remove the hydrogen incorporated in the oxide during the NH₃ anneal step [5], [6]. In the N₂O anneal, there is no hydrogen involved [1]; it is therefore consistent that the reoxidation does not help to improve the quality of N₂O-annealed oxides. This observation supports the hypothesized role of hydrogen in charge trapping. Fig. 4 also shows that the N₂O annealing step does not change the polarity dependence of electron trapping, as has been observed in NH₃ nitridation [6], [8]. Some oxide thicknesses of these devices are labeled in this figure. For a specific final oxide thickness, the choice of the N₂O annealing condition tends to be high temperature and short time. This result is in agreement with the conclusions of a study of interface hardness against hot-electron injection [4].

Fig. 5 shows the Q_{bd} data for different types of oxides with comparable final oxide thicknesses. Q_{bd} is improved by N₂O annealing. This is basically consistent with the charge trapping data since it is known that Q_{bd} can be improved by reducing charge trapping [9]. Comparing the values of Q_{bd} for different polarities, one can also find that the polarity dependence is not obviously enhanced by

N₂O annealing and insuring reoxidation. For instance, the ratio of Q_{bd} under +V_g injection to Q_{bd} under -V_g injection is 2.3 for control oxide and 2.7 for N₂O-annealed oxide (950°C, 80 min), while for NH₃-nitrided oxides, the reported difference between these ratios is 3 times larger [6], [8]. Consistent with the charge trapping results, reoxidation does not further increase Q_{bd} .

In summary, the charge trapping characteristics were compared for thermal oxide, N₂O-annealed thermal oxide, and reoxidized N₂O-annealed thermal oxide. The suppression of electron and hole trapping after N₂O anneal can be significant. The reduction in electron trapping rate monotonically increases with increasing annealing time and temperature in the range studied and is greater for thicker oxides. Reoxidation does not reduce charge trapping further.

REFERENCES

- [1] A. Uchiyama, H. Fukuda, T. Hayashi, T. Iwabushe, and S. Ohno, "High performance dual gate subhalfmicron CMOSGETs with 6 nm thick nitrided SiO₂ films in an N₂O ambient," in *IEDM Tech. Dig.*, 1990, p. 425.
- [2] H. Hwang, W. Ting, D. L. Kwong, and J. Lee, "Electric and reliability characteristics of ultra thin oxynitride gate dielectric prepared by rapid thermal processing in N₂O," in *IEDM Tech. Dig.*, 1990, p. 421.
- [3] J. Ahn, W. Ting, and D. L. Kwong, "Furnace nitridation of thermal SiO₂ in pure N₂O ambient for ULSI MOS applications," *IEEE Electron Device Lett.*, vol. 13, p. 117, 1992.
- [4] Z. H. Liu, H. J. Wann, P. Ko, C. Hu, and Y. C. Cheng, "Effects of N₂O-anneal and reoxidation on thermal oxide characteristics," *IEEE Electron Device Lett.*, vol. 13, p. 402, 1992.
- [5] T. Hori, H. Iwasaki, and K. Tsuji, "Electrical and physical properties of ultrathin reoxidized nitrided oxide prepared by rapid thermal processing," *IEEE Trans. Electron Devices*, vol. 36, p. 340, 1989.
- [6] Z. H. Liu, P. T. Lai, and Y. C. Cheng, "Characterization of charge trapping and high-field endurance for 15 nm thermally nitrided oxides," *IEEE Trans. Electron Devices*, vol. 38, p. 344, 1991.
- [7] M. S. Liang, C. Chang, Y. T. Tzow, C. Hu, and R. Broderson, "MOSFET degradation due to stressing of thin oxide," *IEEE Trans. Electron Devices*, vol. ED-31, p. 1238, 1984.
- [8] A. T. Wu *et al.*, "Gate bias polarity dependence of charge trapping and time-dependent dielectric breakdown in nitrided and reoxidized nitrided oxides," *IEEE Electron Device Lett.*, vol. 10, p. 443, 1989.
- [9] Z. H. Liu *et al.*, "Field and temperature acceleration of time-dependent dielectric breakdown for reoxidized-nitrided and fluorinated oxides," *IEEE Electron Device Lett.*, vol. 13, p. 41, 1992.