Internal ESD Transients in Input Protection Circuits

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Abstract

The operation of the popular thick field device/ grounded-gate transistor combination input protection circuit under ESD stress is studied using a special test circuit. With the ability to monitor internal voltages and currents, we were able to observe how each element in the protection circuit contributed to the overall ESD protection. The special test circuit also allowed us to determine that no degradation of the first gate oxide transistor took place under ESD stress.

1. Introduction

The susceptibility of integrated circuits to electrostatic discharge (ESD) damage has become a major reliability concern especially for present day MOS technologies which use advanced processes with thin gate oxides and shallow junctions [1,2]. Various protection circuits have been used to protect against ESD damage but basically the configuration of most input protection circuits include a primary protection element, a resistor, and a secondary protection element (Fig. 1) [3]. The primary protection element is responsible for shunting most of the high current encountered during the ESD stress. The secondary protection element's purpose is to limit the voltage which appear across the first gate oxide. It is aided by the resistor which limits the current for low source impedance ESD stresses (Machine Model or Charged Device Model). Examples of primary protection elements include thick field devices, SCRs, and large p-n diodes while examples of secondary protection elements include grounded-gate transistors, thick field devices, and p-n diodes.

A number of studies on the operation and ESD susceptibility of the protection elements have been published [4,5]. These studies usually concentrated on each individual element separately, not on how the entire protection circuit worked as a whole. In this paper, we present a study of the internal transients of an input protection circuit under ESD stress. This type of study should facilitate the understanding of complex ESD circuits. Knowledge of the voltage and current waveforms inside the ESD protection circuit should also simplify the study of latent damages since damage due to non-destructive stresses have been studied in detail [6,7].

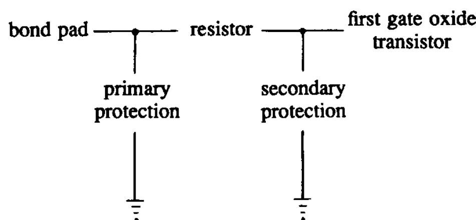
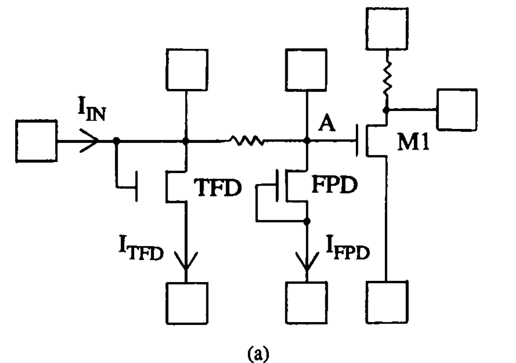


Fig. 1: Basic input protection circuit configuration.

2. Input Protection Test Circuit

Fig. 2a shows the special test circuit used in this study. A thick field device (TFD) operating in the snapback region is used for the primary protection while a grounded-gate transistor (or field plate diode, FPD), the secondary protection element, is used for voltage clamping. Fig. 2b shows the cross-section of these two devices. Separate ground pads allow the currents in the individual paths to be measured. An extra bond pad is connected to the input for Kelvin measurement of the input voltage. An inverter buffer (M1 and its load resistance) is included for on chip monitoring of the voltage at the first gate oxide node (node A) without loading it down by probe capacitance. The inverter also was used to determine if there were any transistor degradation due to repeated ESD stress. While we concentrated on this particular circuit, this type of study can be made on any input protection circuit.



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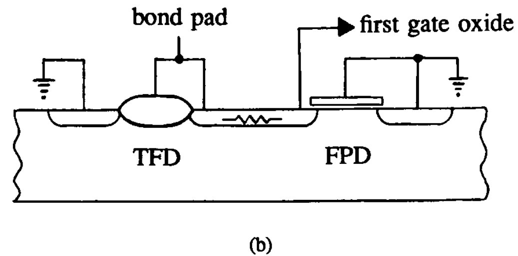

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Fig. 2: (a) Special test circuit used to study internal ESD transients. (b) Cross-section of the TFD and FPD

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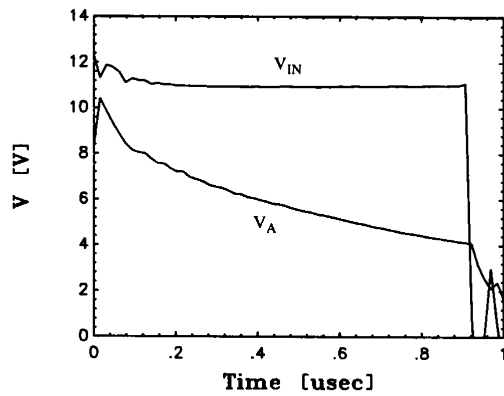
3. Input Protection Circuit Operation

Figs. 3a and 3b show the voltage and current waveforms inside the ESD protection circuit for a ESD-like high current stress at the input. A non-destructive repetitive stress was applied to allow the use of a digital oscilloscope which can gave a more quantized waveform analysis. The response of this circuit to Human Body Model (HBM) and to destructive testing will be discussed in the next section. In Fig. 3a the voltage at node A (V_A) was determined by measuring the voltage at the buffer output and using the transfer characteristics of the inverter. V_A is nicely clamped at under 11 V and decreases with time. This time resolution was made possible by the use of the inverter buffer. Fig. 3b shows that the TFD conducts most of the ESD current as expected but the FPD is seen to sink some amount of current that rises with time even though the TFD device is turned on.

To understand what is taking place in Figs. 3a and 3b, the snapback characteristics of both the TFD and the FPD are examined in Figs. 4a and 4b. Fig. 4a shows their low current characteristics measured by ramping current using a HP4145 while Fig. 4b shows their high current characteristics measured using a pulse generator and a current probe. From Fig. 4a, we see that the TFD snaps back at a lower voltage than the FPD. This suggests that the FPD never reaches its snapback voltage and therefore should not conduct any current during the ESD stress, contrary to what is seen in Fig. 3b. The reason current flowed through the FPD is not because of FPD snapback but because the substrate-source junction of the FPD was forward biased by the substrate potential produced by a hole substrate current flow from the TFD into the surrounding material. The holes are generated in the high field drain region of the TFD. This is verified by grounding node A and observing that the FPD source current can be reduced and turned off by an externally applied substrate-source reverse bias (Fig. 5).



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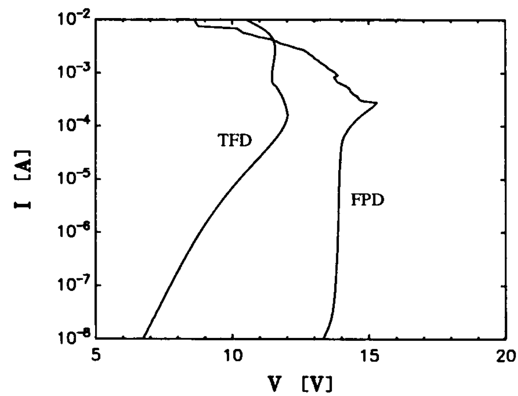

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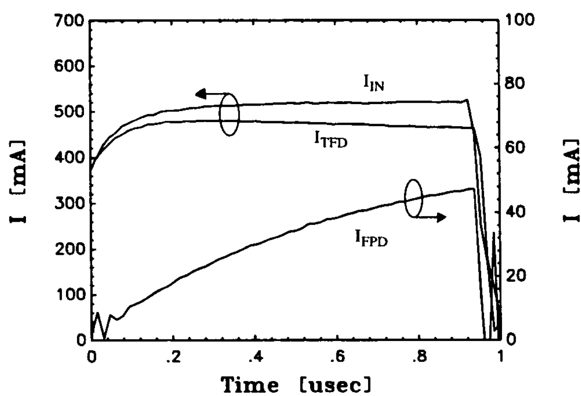

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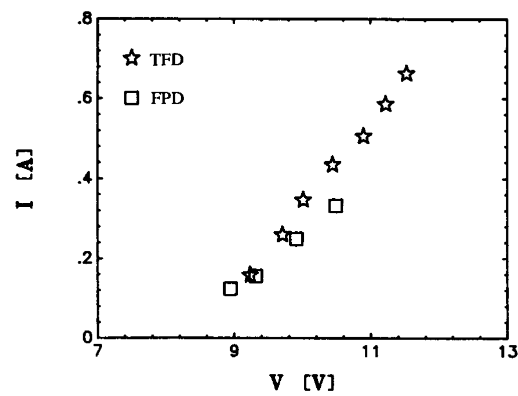


(b)

Fig. 3: (a) Voltage and (b) current transients for a non-destructive repetitive stress.

Fig. 4: (a) Low and (b) high drain current characteristics of the TFD and FPD.

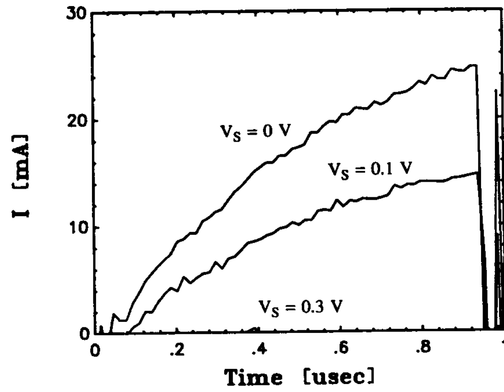


Fig. 5: FPD source current for different externally applied substrate-source reverse biases.

The time constant associated with the FPD current in Fig. 3b and Fig. 5 is due to the diffusion time required by the electrons injected from the source of the FPD to reach the TFD area so that the substrate resistance between the two devices is reduced by conductivity modulation. This would induce a larger portion of the hole current generated at the TFD drain to flow to the FPD where it serves as the base current of the lateral NPN bipolar transistor (with the FPD source as the emitter and its drain as the collector). As the base current increases, so does the emitter (FPD source) current. The estimated electron diffusion time is $L^2/2D_n$ where L is the distance between the TFD and FPD and D_n is the electron diffusion constant. For L = 50 μm and D_n = 25 cm^2/sec, the estimated diffusion time is 0.5 μsec in reasonable agreement with the current rise times of Figs. 3b and 5. Also we found the rise time of a similar current in M1 (see Fig. 2a) is about four times larger, roughly in proportion to the square of the distance from the TFD.

Because of this forward biased junction, the FPD acts as a lateral bipolar transistor and provides a small amount of ESD protection. It does not have to follow the I-V characteristics of Figs. 4a and 4b since it was "externally" triggered into snapback. In fact, the measured FPD source current, I_{FPD}, shown in Fig. 3b is larger than its drain current. This is opposed to the situation for Figs. 4a and 4b where the TFD's and FPD's drain currents are always greater than their corresponding source currents because substrate current is needed to forward bias their substrate-source junction. Since the TFD snapback was not externally triggered, it does follow the I-V characteristics of Figs. 4a and 4b.

For this particular input protection circuit, TFD snapback occurred at a lower voltage than FPD snapback because of a relatively low field threshold voltage. The low field threshold voltage allowed for MOS conduction since the gate of the TFD is tied to its drain. The mobile charge due to this conduction caused an increase of the electric field thus reducing the voltage necessary for snapback. For other technologies, the FPD may snapback first and clamp V_A to below its snapback voltage. The voltage rise across the series resistor will then cause the TFD to snapback and shunt the ESD current. This can be simulated in our protection circuit by applying a small, -1 V, substrate bias (V_{SUB} = - 1 V) so that the snapback voltage of the TFD rises above that of the FPD (Fig. 6) due to the large body-effect coefficient of the thick field oxide transistor. Fig. 7 shows the transient response of the TFD and the FPD with V_{SUB} = -1 V for a current stress which increases with time. Initially the FPD snaps back, but as the voltage across the resistor increases, the TFD turns on. The current through the FPD drops suddenly when the TFD turns on. The maximum V_A is approximately 16 V (Fig. 6) for this case of V_{SUB} = - 1 V compared to approximately 11 V (Fig. 3a) for the case of V_{SUB} = 0 V.

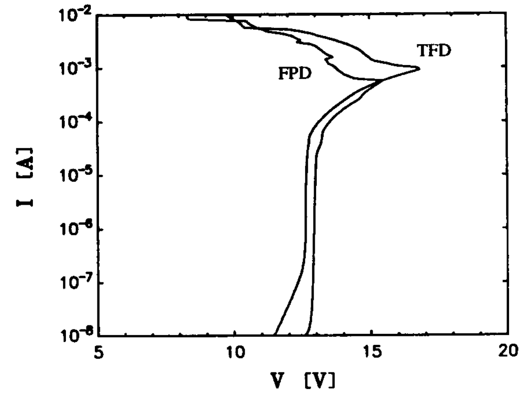


Fig. 6: Snapback characteristics for both the TFD and FPD for V_{SUB} = - 1 V.

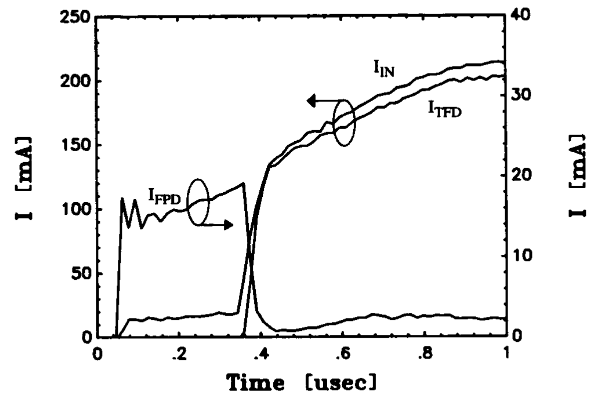
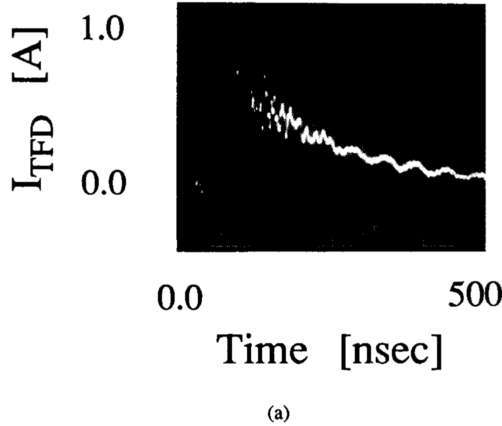


Fig. 7: Current transients for V_{SUB} = - 1 V for a current stress which increases with time.

4. Response to HBM Stress and Destructive Testing

Figs. 8a and 8b show the current flowing through the TFD and V_A for a 1.5 kV HBM stress using a commercial ESD tester (V_{SUB} = 0 V). The HBM network consists of a charged 100 pF capacitor (in this case, charged to 1.5 kV) and a 1.5 kΩ series resistor. The capacitor is discharged into the input pin through the series resistor thus providing a high current, low voltage stress since most of the voltage is

dropped across the 1.5 kΩ resistor. The peak current is approximately 1 A as expected. V_A peaks at 12 V, approximately 1 V less than the voltage expected at the input from the extrapolation of the high current I-V curve of Fig. 4b for the TFD. V_A decreases during the HBM stress because of the externally triggered snapback discussed in the previous section.



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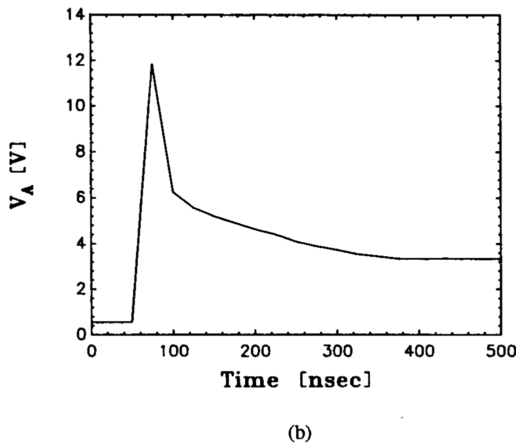

(b)

Fig. 8: (a) TFD current and (b) voltage at node A for a 1.5 kV HBM stress. V_A was determined from the buffer output voltage.

The effect of a destructive pulse on the internal waveforms of the input protection circuit is shown in Fig. 9. A current pulse of 1.0 A (V_{SUB} = 0 V) was applied to the input. When the TFD failed at 0.35 μsec into the pulse, I_{TFD} decreases because the current was shunted into the substrate due to the failure of its drain-substrate junction. This caused a drop in V_{IN} since less voltage was needed to maintain the same input current [8]. Because V_{IN} decreased for this type of failure, it did not cause an increase in V_A which could have led to unexpected damage of M1.

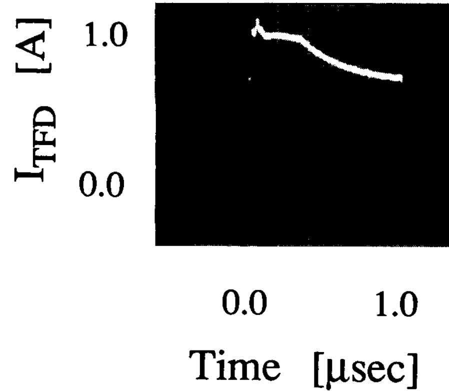

Fig. 9: TFD current for a destructive 1.0 A current stress.

5. First Gate Oxide Transistor (M1) Characteristics

The special test circuit was also used to determine the effectiveness of this input protection circuit in protecting the first gate oxide transistor, M1. In Fig. 10, the threshold voltage of M1 was measured as a function of the number of ESD-like high current pulses (500 mA for 1 μsec). The figure shows that no threshold shift occur after 1000 pulses for two cases, V_{SUB} = 0 V (TFD snapback occurs before FPD snapback) and V_{SUB} = - 1 V (FPD snapback occurs before TFD snapback). Fig. 11 shows the maximum voltage for a 100 nsec pulse which an oxide can sustain before oxide breakdown and - 10 mV threshold shift for different oxide thicknesses [6]. For this 200 Å gate oxide, a voltage greater than 25 V will be required for significant threshold shifts. Since the maximum voltages for the two cases are 11 V and 16 V respectively, no threshold shifts are expected. Fig. 10 confirms this expectation. Oxide time-to-breakdown is not expected to decrease because of the relatively low voltages encountered at node A during ESD stress.

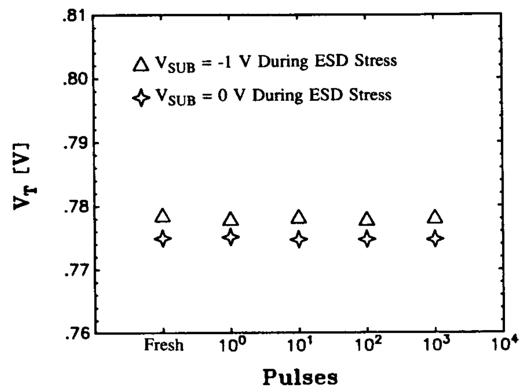

Fig. 10: Threshold shift of M1 as a function of the number of 500 mA/1 μsec current pulses for V_{SUB} = 0 V and - 1 V.

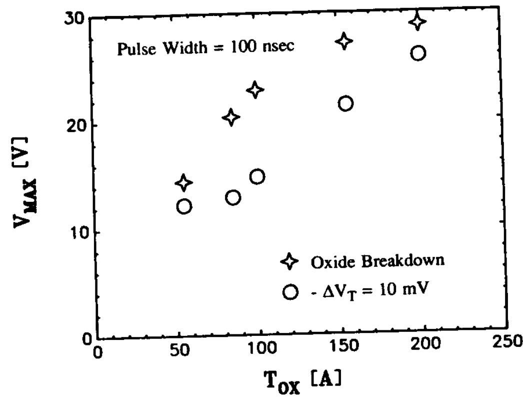

Fig. 11: Maximum voltage for a 100 nsec pulse which an oxide can sustain before oxide breakdown and - 10 mV threshold shift for different oxide thicknesses [6].

The hot-electron degradation characteristics of M1 are examined in Fig. 12. It has been noted in [7] that transistors which experienced ESD-like high current stress at the drain exhibited greater hot-electron degradation. Fig. 12 shows the hot-electron degradation of M1 after 1000 (500 mA for 1 μsec, V_{SUB} = - 1 V) pulses at the input of the protection circuit and also after a 3 kV HBM stress (V_{SUB} = 0 V). Comparing these characteristics with the no ESD stress transistor, no increased degradation is observed. Thus the input protection circuit shown in Fig. 2 protected M1 very effectively by limiting the voltage at the gate of M1. Even after destructive ESD testing, measurements on M1 revealed no change in its transistor characteristics.

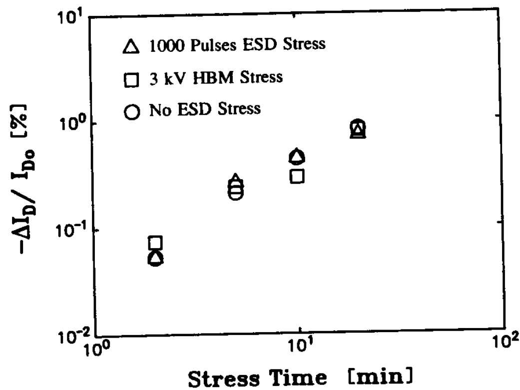

Fig. 12: Hot-electron degradation characteristics of M1 after 1000 (500 mA/1 μsec, V_{SUB} = - 1 V) pulses, 3 kV HBM stress, and no ESD stress.

6. Summary

In this paper, we presented a study of the internal transients of an input protection circuit under non-destructive and destructive ESD stress. Using a special test circuit we were able to monitor the internal voltages and currents in the protection circuit to determine how each element in the protection circuit contributed to the overall ESD protection and also the interaction of these elements. The response of this circuit to repetitive non-destructive stress, HBM stress, and destructive stress were presented. According to the measured internal voltage, no significant latent damage to the 200 Å transistor is expected. Indeed, no change in V_T and hot electron degradation rate were found after 1000 (500 mA/1 μsec) pulses. Oxide time-to-breakdown is not expected to decrease. This suggests that the onset of latent damage may be predictable from the measured internal waveforms.

7. Acknowledgement

This research is supported by Texas Instruments and the University of California MICRO program.

8. References

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