

The Effects of Oxide Stress Waveform on MOSFET Performance

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Abstract

Device degradation after oxide stress is dependent on the stress waveform. Specifically, bi-directional tunneling current creates a larger number of interface traps than does uni-directional gate current. Even though unipolar stressed devices suffer more bulk trapping and TDDB degradation than do bipolar stressed devices, the degradation in transconductance, mobility and threshold voltage is worse in bipolar stressed devices.

Experiment

We use three different waveforms (Fig. 1) to study the behavior of n-MOSFETs after dynamic oxide stress. Oxide thickness is 11 nm and 8.5 nm. Time dependent dielectric breakdown was monitored on devices with W/L (in microns) of 5/5, 5/10, 10/5, and 10/10. Time to breakdown was independent of device size for the range of device sizes used. A description of the time to breakdown experimental set-up may be found in [1]. Larger devices (50/50) were

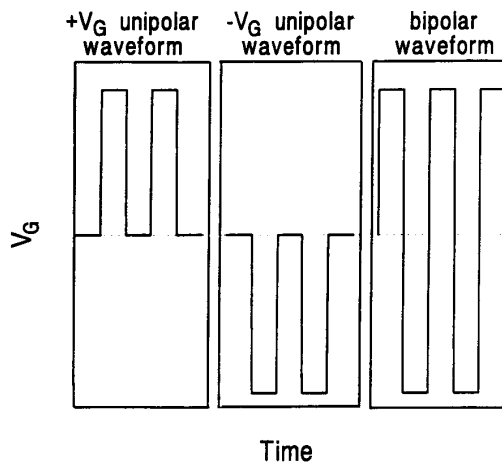


Fig. 1 Three waveforms were used to study the degradation of oxide under dynamic stress. Maximum values of $+V_g$ and $-V_g$ were selected using the criterion that both give similar t_{BD} under DC bias. These waveforms were applied to n-MOSFETs with the drain, source and substrate connected to ground.

used for the trials in which C-V characteristics before and after stressing were measured. Quasi-static C-V was measured using a HP4140 Voltage Source/Ammeter; high-frequency C-V was measured using a HP4192 LCR Meter. Device I-V characteristics were measured with a HP4145 Parameter Analyzer. The HP8115 pulse generator was under computer control so that stressing could be stopped at specified intervals and these measurements could be conducted.

Time Dependent Dielectric Breakdown

As reported in [1], time to breakdown t_{BD} is a strong function of frequency under bipolar stress and its value is larger than that under unipolar or DC stress (Fig. 2). Note that at low frequencies, bipolar t_{BD} approaches the unipolar value, while at high frequencies, bipolar t_{BD} saturates. A new study of this phenomenon at a variety of electric fields shows that the saturation frequency is a strong function of electric field (Fig. 3). This point will be discussed in greater detail later in the text.

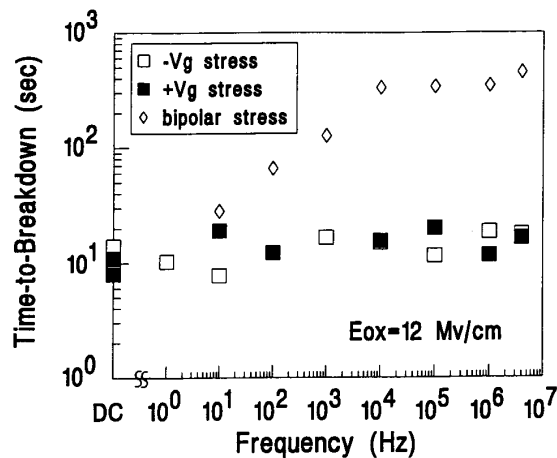


Fig. 2 t_{BD} under DC and unipolar dynamic stress conditions is similar but is longer and frequency dependent under bipolar stress. t_{BD} is defined as the experiment duration multiplied by the duty cycle. Duty cycle for bipolar stressed devices is the fraction of time the signal spends at maximum $+V_g$. $X_{ox}=11\text{nm}$. (Data is from [1].)

Quasi-static and high frequency C-V were used to examine the different ways in which unipolar and bipolar stress affect the oxide. Quasi-static C-V curves for devices stressed with oxide electric field of 12.1 MV/cm at 100 kHz for 2 seconds are shown in Fig. 4. Change in flat band voltage (ΔV_{fb}) as a function of stress time is shown in Figure 5; this was calculated from high frequency C-V. Figures 4 and 5 indicate that interface trap generation is greater in bipolar stressed devices, while bulk trapping is greater in unipolar stressed devices. C-V data for devices subject to 100 Hz bipolar stress (not shown) demonstrate interface trap generation similar to that found after stressing at 100 kHz and bulk trapping similar to that caused by unipolar stress. Figure 2 shows that t_{BD} for a device which is bipolar stressed with an electric field of 12 MV/cm at 100 Hz is much lower than t_{BD} measured after stressing at 100 kHz, leading to the conclusion that bulk trapping is correlated with oxide breakdown, while interface trap generation is not.

There is evidence that hole trapping in oxide precipitates breakdown (see, for example, [2]). This is consistent with our observation that the early time ΔV_{fb} shifts are negative and are largest in the unipolar stressed devices (Fig. 5). Holes are generated near the anode in thin oxides [3]; some of these may become trapped. To explain the observation that bipolar t_{BD} is longer than unipolar t_{BD} , we hypothesize that the field reversal impedes movement of holes toward the bulk and that the field reversal enhances detrapping. Hole transport in SiO₂ has been shown to be quite dispersive in time and strongly electric field activated [4]; this is the same behavior displayed by bipolar t_{BD} . If one interprets time to breakdown as inversely proportional to the number of holes trapped in the bulk per unit time, then our bipolar stress t_{BD} data can be explained by hole transport. Trapped holes which hop toward the cathode under the influence of the electric field are less likely to be detrapped

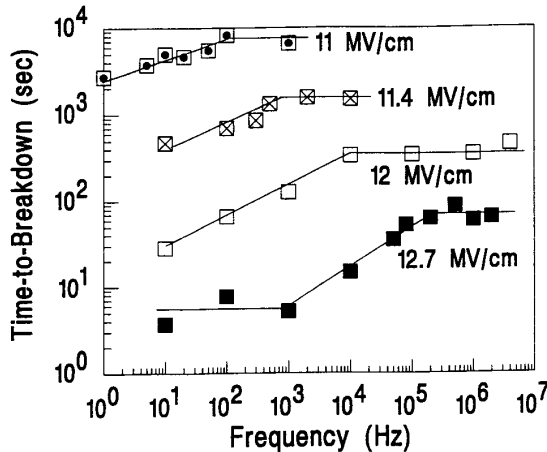


Fig. 3 The shape of the bipolar t_{BD} versus frequency curve does not change as the electric field is varied. However, the saturation ("knee") frequency decreases with decreasing electric field. $X_{ox}=11nm$.

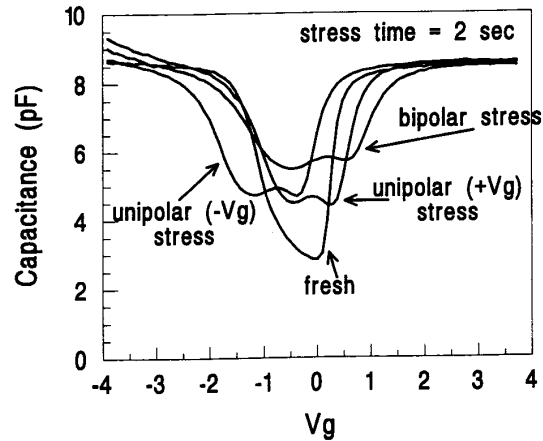


Fig. 4 Distortion of quasi-static C-V curves after oxide stressing at 12.1 MV/cm for 2 seconds of elapsed time indicates that bipolar stressing causes more interface trap generation than does unipolar stressing in either polarity. $X_{ox}=11nm$, Area= $50\mu m \times 50\mu m$.

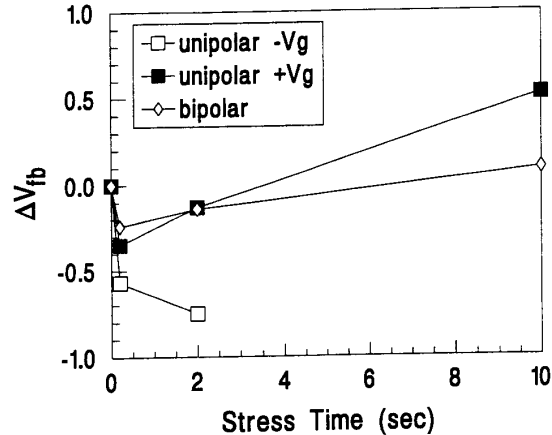


Fig. 5 Change in flat-band voltage, as measured from shifts in high-frequency C-V, is smaller in bipolar stressed devices than in unipolar stressed devices, showing that bulk trapping is less in bipolar stressed devices. Stress time is elapsed time, $X_{ox}=11nm$, $E_{ox}=12.1MV/cm$. Oxide breakdown in the $-V_g$ device occurred at 6.9 seconds. The first set of stressed data points are not plotted to scale on the time axis; they were measured at .02 sec.

when the field reverses, since the probability of detrapping decreases with increasing distance from the interface [4]. If the signal frequency is sufficiently low, then many holes will have moved into the bulk before field reversal; therefore, ΔV_{fb} and t_{BD} will be similar to that under unipolar stress. At sufficiently high frequency (the "saturation frequency" which can be seen on each of the curves in Figure 3), even the fastest holes don't have time to move away from the interface. The field dependence of saturation frequency is not surprising in light of the fact that hole mobility in SiO₂ is field dependent.

The scenario of hole generation near the anode and detrapping when the field reverses can also explain why we observe large interface trap generation under bipolar stress. Interface traps are known to result when electrons recombine with holes trapped near the interface [5]. Interface trap density saturates quickly in unipolar stressed devices; however, it continues to increase in bipolar stressed devices as can be seen from Figure 6.

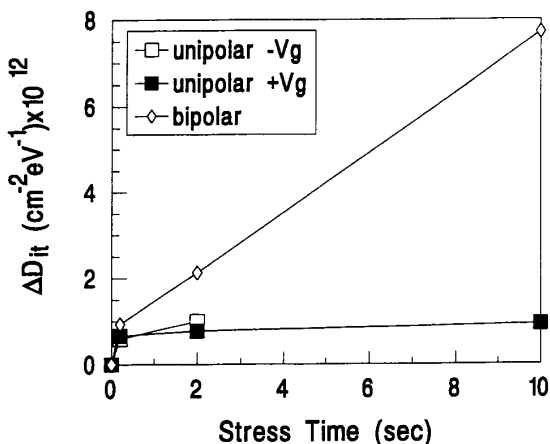


Fig. 6 Interface trap density, as measured from changes in quasi-static C-V, was calculated at mid-gap for the same devices as in Fig. 5. Interface trap generation quickly levels off in unipolar stressed devices but not in bipolar stressed devices.

MOSFET Performance Degradation

We monitored the performance of transistors which were unipolar and bipolar stressed at 10 MV/cm. It is worthwhile to examine this because, in ordinary MOS circuits, the gate-drain overlap region and the nearby channel region are subject to bipolar stress. Furthermore, as device scaling continues for ULSI applications, the oxide electric field will rise. Figures 7 and 8 show I-V characteristics of 8.5 nm n-MOSFETs before and after $+V_g$ unipolar stress and bipolar stress, respectively. The unipolar stress experiment was conducted for twice the duration of the bipolar stress experiment to emphasize that the differences are real, not just due to duty cycle. Threshold voltage shifts are evident in both figures but current drive in the bipolar stressed device is further degraded by a decrease in the transconductance, G_m . Transconductance before and after stress is plotted in Figure 9. Mobility is known to be affected by interface traps, this is clearly seen in Figure 10 where we plot effective electron mobility μ_{eff} versus the effective vertical field E_{eff} .

Subthreshold characteristics are plotted in Figures 11 and 12. The degradation in S (subthreshold swing) after stressing correlates nicely with the growth in interface trap

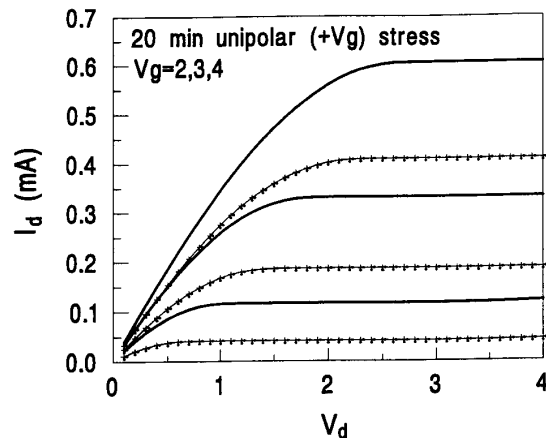


Fig. 7 Fresh I_d - V_d curves are plotted with smooth lines, stressed curves are plotted with hatched lines. A V_{th} shift is very noticeable after stressing. $X_{ox}=8.5$ nm, Area= $50\mu\text{m}\times 50\mu\text{m}$, $E_{ox}=10$ MV/cm, stress time is elapsed time.

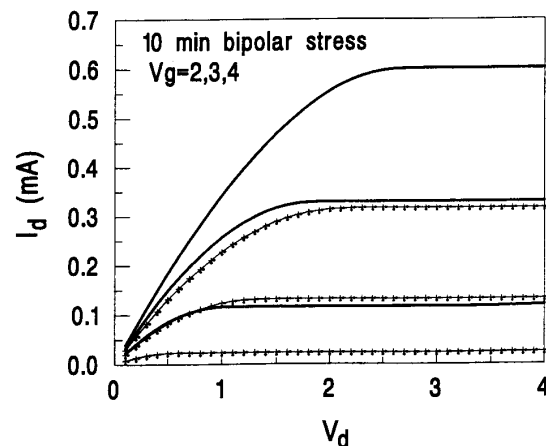


Fig. 8 Degradation of I_d - V_d after 10 minutes of bipolar stress is greater than that found after 20 min. of unipolar stress (see Fig. 7). The enhanced degradation arises from the negative effect of interface traps on transconductance. Fresh curves are plotted with smooth lines, stressed with hatched. $X_{ox}=8.5$ nm, Area= $50\mu\text{m}\times 50\mu\text{m}$, $E_{ox}=10$ MV/cm, stress time is elapsed time.

density as calculated from quasi-static C-V. D_{it} in the subthreshold region was found to be $6.38\times 10^{11}\text{cm}^{-2}\text{eV}^{-1}$ after 20 minutes $+V_g$ unipolar stress and $1.39\times 10^{12}\text{cm}^{-2}\text{eV}^{-1}$ after 10 minutes bipolar stress. The D_{it} data predicts a 18% increase in S after unipolar stressing and a 40% change increase in S after bipolar stressing; the measured changes were 18% and 39%, after unipolar and bipolar stressing, respectively.

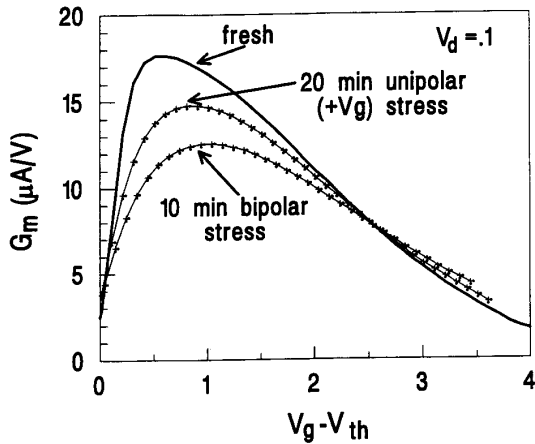


Fig. 9 Transconductance before and after stressing is plotted versus $V_g - V_{th}$. G_m was calculated for the same devices whose $I_d - V_d$'s are plotted in Figs. 7 and 8.

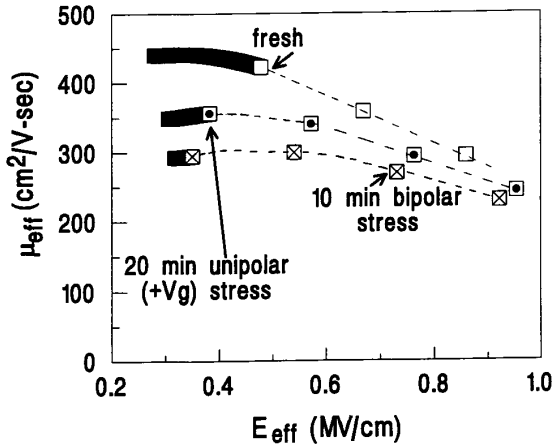


Fig. 10 When mobility is plotted versus effective vertical field, the enhanced degradation of bipolar stressed devices is very clear. μ_{eff} was calculated for the devices in Figs. 7 and 8.

Conclusions

The transport and detrapping properties of holes generated near the anode can account for the differences observed after unipolar and bipolar oxide stressing. Bipolar stress yields a lower rate of bulk charge trapping and longer time to breakdown than unipolar stress. The difference is dependent on both field and frequency. At the same time, bipolar stress leads to enhanced interface trap generation. Since the gate-drain overlap region of MOSFETs in circuits is subject to bipolar stress, DC transistor stress tests may underestimate the MOSFET degradation rate. The observation that interface trap density does not saturate during bipolar stress as readily as during unipolar stress is particularly alarming.

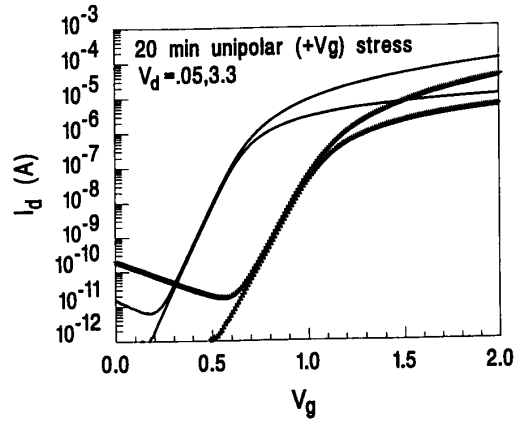


Fig. 11 Subthreshold characteristics before and after unipolar stressing show the effects of bulk trapping (V_{th} shift) and interface trap generation (increase in subthreshold swing). These curves are for the same device as in Fig. 7.

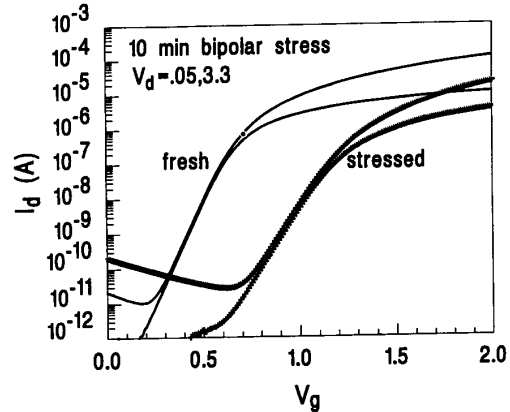


Fig. 12 Subthreshold characteristics after bipolar stressing show greater distortion than those measured after unipolar stressing. These curves are for the same device as in Fig. 8.

References

- [1] E. Rosenbaum and C. Hu, *IEEE Electron Device Lett.*, Vol. 12, no. 6, p. 267, 1991.
- [2] I.C. Chen, et al., *IEEE Trans. on Electron Devices*, Vol. 32, no. 2, p. 413, 1985.
- [3] Y. Nissan-Cohen, et al., *J. Applied Physics*, Vol. 57, no. 8, p. 2830, 1985.
- [4] F.B. McLean, et al., "Electron-Hole Generation, Transport and Trapping," in *Ionizing Radiation Effects in MOS Devices and Circuits*, ed. T.P. Ma and P.V. Dressendorfer, 1989.
- [5] S.K. Lai, *Applied Physics Lett.*, Vol. 39, no. 1, p. 58, 1981.