Transient Behavior of Subthreshold Characteristics of Fully Depleted SOI MOSFET's

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Abstract—**It has been found that the subthreshold currents of fully depleted silicon-on-insulator (SOI) MOSFET's show a transient behavior under certain front-gate and back-gate voltage conditions. The cause of this anomaly is explained, and applications for the above phenomenon are pointed out. Particularly, a simple way to measure the silicon film thickness is suggested.**

Nomenclature

V_{fg} Front-gate voltage.
V_{bg} Back-gate voltage.
ϕ_{fs} Surface potential at the front silicon-oxide interface.
ϕ_{bs} Surface potential at the back silicon-oxide interface.
$C_{fg} = \epsilon_{ox}/T_{fg}$, $C_{bg} = \epsilon_{ox}/T_{bg}$, $C_{si} = \epsilon_{si}/T_{si}$, $V'_{fg} = V_{fg} - V_{fb,f}$, $V'_{bg} = V_{bg} - V_{fb,b}$.

I. Introduction

SILICON-on-insulator (SOI) MOSFET's are very attractive for radiation-hardened IC's and future high-performance VLSI [1]. Two important parameters for fully depleted SOI MOSFET's—the threshold voltage and the subthreshold swing $\{S = dV_{gs}/d\log(I_d)\}$—are studied here.

It is well known that for fully depleted SOI MOSFET's the front-channel threshold voltage V_{tf} is dependent on the back-gate voltage V_{bg}. Particularly, as V_{bg} is made more negative, V_{tf} increases until the back silicon surface enters accumulation. At this point, V_{tf} becomes independent of V_{bg}, and making V_{bg} more negative will not change V_{tf} any more [2] (the solid line in the inset of Fig. 1).

In this paper we will show that the above characteristics exhibit transient behavior. We provide an explanation for this phenomenon, and point out its possible applications. First, a simple and convenient way to measure the silicon film thickness is suggested. Second, the potential application of the above effect for studying the quality of the front and back silicon-oxide interfaces is pointed out.

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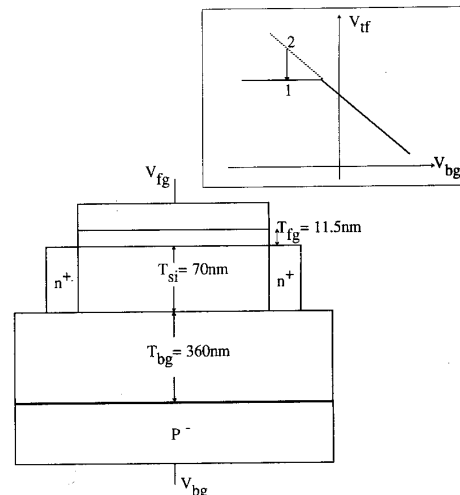

Fig. 1. Schematic cross section of an n-channel SOI MOSFET. The inset represents front-channel threshold voltage V_{tf} as a function of back-gate voltage V_{bg}.

II. Experiment and Discussion

The SOI devices used in the study were n-channel MOSFET's on SIMOX wafers fabricated with a modified submicrometer CMOS technology. The gate oxide thickness T_{fg}, silicon film thickness T_{si}, and buried oxide thickness T_{bg} were approximately 11.5, 70, and 360 nm, respectively. The doping concentration was approximately 1×10^{17} cm^{-3}. LOCOS was used to isolate the SOI devices. All the measurements reported here were performed using a HP4145 parameter analyzer.

Fig. 2 shows the subthreshold characteristics when −20 V is applied to the back gate and the front gate is scanned from 0.2 to 1.2 V with two different scan rates. Curve #1 corresponds to a slow scan rate (~3 mV/s), while curve #2 corresponds to a fast scan rate (100 mV/s). We notice that both subthreshold swings and threshold voltages differ significantly for these two curves.

When $V_{bg} = -20$ V, the back surface should be accumulated under steady-state conditions. However, the accumulation layer cannot form immediately after the back-gate voltage is applied (due to a lack of source of holes). This implies that V_{tf} still increases with decreasing of V_{bg}. Thus, V_{tf} is larger than its steady-state value. This "transient" value of

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V_{tf} is shown as branch 2 in the inset of Fig. 1. As time elapses, the generation of holes through interface states, junction leakage, and bulk generation centers allows the accumulation layer to form. While the back surface becomes accumulated, V_{tf} moves gradually toward branch 1 in the inset of Fig. 1. This transient behavior of V_{tf} is illustrated in Fig. 2. Curve #1 in Fig. 2, which is measured at a slow scan rate, always allows enough time for the accumulation layer on the back side to form, and represents the steady-state characteristics. In contrast, curve #2 in Fig. 2 is measured at a fast scan rate, so the accumulation layer is not formed and V_{tf} is larger. This explains why curve #2 is shifted to the right with respect to curve #1.

If we define the value of V_{fg} where $I_d = 10$ nA as the threshold voltage (point 1 in Fig. 2), then $V_{tf} = 0.62$ V for curve #1. Thus, if we set $V_{fg} = 0.62$ V, $V_{bg} = -20$ V, and measure I_d versus time, we expect the final steady-state value of I_d to be 10 nA. This is shown as curve #1 of Fig. 3. It is seen that after approximately 32 s I_d reaches 90% of its final value. It is expected that the better the interface quality and the lower the junction leakages, the longer this transient behavior will last. Thus, applications that rely on the dependence of V_{tf} on V_{bg} should be carried out with great care (such as silicon film thickness measurement suggested in [3]). Otherwise, erroneous results will be obtained.

Based on the above reasoning, the difference between the two subthreshold swings can be analytically evaluated. When the silicon film is fully depleted we have

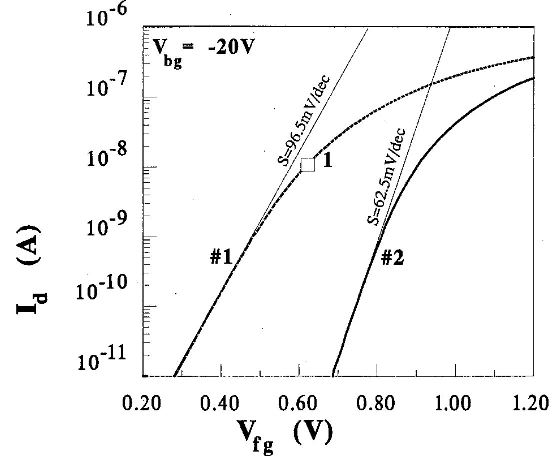

Fig. 2. Drain current for two different scan rates of front-gate voltage. Curve #1 is for the slow scan, and curve #2 is for the fast scan. V_{bg} and V_{ds} are −20 and 0.1 V, respectively.

measured value of 96.5 mV/decade of curve #1 in Fig. 2. The difference could be due to C_{it} which we assumed to be small in our calculations. Conversely, the above formulation can be used to determine T_{si} if T_{fg} and T_{bg} are known, and the two subthreshold swings are measured.

The above experiment can also be performed with the back surface inverted and the front surface accumulated. Thus, the current is completely carried by the inversion layer at the lower silicon-oxide interface. The result is shown in Fig. 4.

$$\phi_{fs} = \frac{\frac{-qN_aT_{si}}{C_{fg}}\left(1 + C_{bg}/2C_{si}\right) + V'_{fg}\left(1 + C_{bg}/C_{si}\right) + V'_{bg}C_{bg}/C_{fg}}{1 + C_{bg}/C_{fg} + C_{bg}/C_{si}}. \tag{1}$$

Subthreshold swing is $S = (60\ \text{mV/decade})n$, where n is given by $n = (d\phi_{fs}/dV_{fg})^{-1}$. From (1) we can determine n:

$$n = 1 + \frac{\frac{C_{bg}C_{si}}{C_{bg} + C_{si}}}{C_{fg}} = 1 + \left(C_{sub,\text{eff}}/C_{fg}\right). \tag{2}$$

Notice that $V_{fg} = -4$ V guarantees that the front surface will be accumulated under the steady-state conditions. Curve #1 shows the result for the slow scan (~20 mV/s), and curve #2 shows the result for the fast scan (600 mV/s). In curve #2 the accumulation layer has not formed yet, and V_{tb} (back-channel threshold voltage) is larger than that of curve #1. The slope of these two subthreshold currents can be calculated in a similar fashion:

$$\phi_{bs} = \frac{\frac{-qN_aT_{si}}{C_{fg}}\left(1 + C_{fg}/2C_{si}\right) + V'_{fg} + V'_{bg}\left(C_{bg}/C_{fg} + C_{bg}/C_{si}\right)}{1 + C_{bg}/C_{fg} + C_{bg}/C_{si}}. \tag{3}$$

When the silicon film is fully depleted, ϕ_{fs} is determined by the voltage division between C_{fg} and $C_{sub,\text{eff}}$, which is the series combination of C_{bg} and C_{si} as expected. Since C_{bg} is very small, $C_{sub,\text{eff}} \cong 0$, $n \cong 1$, and $S \cong 60$ mV/decade. This agrees very well with the measured value of 62.5 mV/decade for curve #2 of Fig. 2. However, if enough time has elapsed such that the accumulation layer forms, this layer becomes an ac ground plane in the voltage divider circuit (C_{bg} is shielded off), and $C_{sub,\text{eff}} \cong C_{si} = \epsilon_{si}/T_{si}$. Using T_{si}, T_{fg}, and T_{bg} values for our device we obtain $S = 89.6$ mV/decade, which again agrees well with the

$S = (60\ \text{mV/decade})(d\phi_{bs}/dV_{bg})^{-1} = (60\ \text{mV/decade})(1 + C_{sub,\text{eff}}/C_{bg})$, and $C_{sub,\text{eff}}$ is now the series combination of C_{fg} and C_{si}. Thus, when the accumulation layer is not formed $C_{sub,\text{eff}} = 1/(T_{si}/\epsilon_{si} + T_{fg}/\epsilon_{ox})$. When the accumulation layer is formed, $C_{sub,\text{eff}}$ is only C_{si}. If we use the known values of T_{si}, T_{fg}, and T_{bg} as above, we get $S = 986$ mV/decade for curve #1, and $S = 680$ mV/decade for curve #2, which agree within 12% with the measured results. A combination of this measurement and previous measurement (Fig. 2) provides a more accurate value for T_{si}. Table I compares T_{si} measured by this method and the *CV*

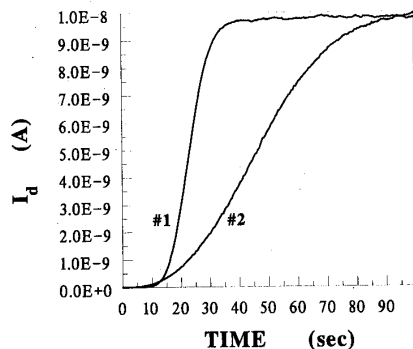

Fig. 3. Transient response of the drain current. In curve #1 the inversion layer is at the front silicon-oxide interface; in curve #2 the inversion layer is at the back silicon-oxide interface.

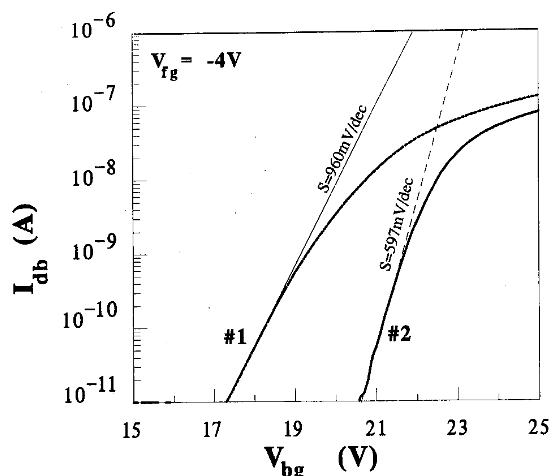

Fig. 4. Drain current for two different scan rates of back-gate voltage. Curve #1 is for the slow scan, and curve #2 is for the fast scan. V_{fg} and V_{ds} are –4 and 0.1 V, respectively.

method suggested in [4]. The two methods agree within 10%.

On curve #1 (slow scan) of Fig. 4 we choose the threshold point to correspond to I_{db} = 10 nA, where V_{bg} = 20.8 V. If we set V_{bg} = 20.8 V, V_{fg} = −4 V, and measure I_{db}

TABLE I
SILICON FILM THICKNESSES MEASURED BY THE *CV* METHOD DESCRIBED IN [4] AND BY THE METHOD PRESENTED IN THIS PAPER

	Die *A*	Die *B*	Die *C*	Die *D*
CV method	91.7 nm	76.3 nm	71.4 nm	75.7 nm
Subthreshold method	96.3 nm	68.3 nm	76.1 nm	75.3 nm

versus time, curve #2 of Fig. 3 is obtained. It is seen that after approximately 75 s I_{db} reaches 90% of its final value. The explanation for the transient behavior of curve 2 is similar to that of curve 1. The difference in response times between the two curves is a qualitative measure of the silicon-oxide interface qualities for the front and back surfaces. It should be mentioned that it is difficult to determine the quantitative difference of the quality of the two interfaces. The difficulty arises from the fact that the bulk and the two interfaces are all in nonequilibrium condition, and the generation of holes occurs at all three places. However, under certain bias conditions one interface might become the dominant contributor of holes. Currently, experiments are being carried out to investigate the feasibility of this idea.

III. SUMMARY

The transient behavior of subthreshold currents in fully depleted SOI MOSFET's is reported. The cause of this phenomenon is explained, and some applications are pointed out. Particularly, a simple way to measure the silicon film thickness is suggested.

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