F7.

Implications of Waveform and Thickness Dependence of SiO_2 Breakdown on Accelerated Testing

E. Rosenbaum, R. Moazzami and C. Hu

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA 94720

Abstract

Oxide breakdown characteristics under accelerated test conditions are different from those under normal operating conditions. While oxide lifetime under unipolar pulse stress is roughly equal to the DC lifetime multiplied by the recip.o-cal of the duty cycle, lifetime under bipolar pulse stress is extended by an additional factor of 40 or more. At the high electric fields used during accelerated testing, oxides with thickness greater than 15 nm suffer lifetime degradation which may be attributed to hole trapping. This will lead to overly conservative projections of lifetime under normal operating conditions.

Introduction

This paper presents recent results on several practically important, but little studied, aspects of gate oxide breakdown. Results of DC, pulse and bipolar testing up to 4 MHz, as well as the thickness dependence of the breakdown field, demonstrate that oxide lifetime under accelerated test conditions may be significantly different from lifetime under normal operating conditions.

Effect of Bias Polarity on Breakdown Voltage

Figure 1 shows the results of a series of ramp voltage breakdown (V_{BD}) tests on structures of varying oxide thickness. All devices were fabricated on p-type substrate and have n+ polysilicon gates. The devices were biased with negative gate voltage, *i.e.*, in accumulation. Small device sizes were used to ensure that we would observe intrinsic breakdown characteristics rather than those related to defects. The slope in the thin oxide region is in excellent agreement with that predicted by the model detailed in [1] and plotted as "Theory" in the figure.

One striking feature of Figure 1 is that the experimental data does not intercept the axes origin. This anomaly occurs because the applied gate voltage is not necessarily equal to the voltage drop

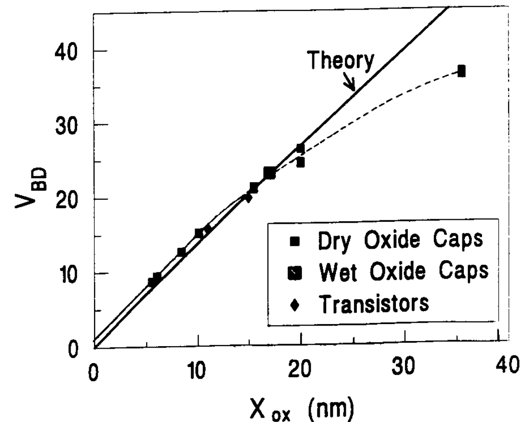

Fig. 1 A comparison of predicted and measured ramp voltage breakdown values. Samples were 5μx5μ p-type capacitors biased in accumulation. The ramp rate was .5 volt/sec.

across the oxide. The actual oxide voltage is obtained by subtracting the work function difference and amount of substrate band bending from the applied voltage. We performed a series of experiments to quantify the difference between $V_{applied}$ and V_{ox}. This voltage offset was determined by comparing I_g-V_g curves in both polarities. One data set is shown in Figure 2. Based on this and similar data, we conclude that devices fabricated with n+ poly gates and biased with $-V_g$ have approximately a 1.2 volt difference between $V_{applied}$ and V_{ox}. The results of all our experiments are summarized in Table 1.

Figure 2 suggests that, in the high field region, even devices biased with $+V_g$ may need to have a quantity subtracted from $V_{applied}$. The closing, at high oxide electric fields, of the gap between positive and negative biased I_g-V_g curves was found in several n+ poly gate devices, specifically, p-type capacitors, n-type capacitors, and n-MOSFETs. This phenomenon is process dependent. Prelim-

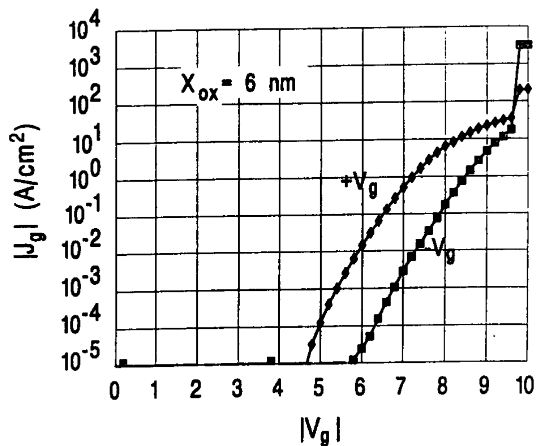

Fig. 2 6 nm p-type capacitors were subjected to a voltage ramp of .5 V/sec in both polarities as part of an experiment to determine the offset between V_g and V_{ox}.

$\|V_{OX}\| \approx \|V_G\|$ – the following:			
	n^+ poly on p sub	n^+ poly on n sub	p^+ poly on n sub
$+V_G$	0.0	0.0	1.2
$-V_G$	1.2	1.2	0.9

Table 1 I-V experiments show that V_{ox} is dependent on bias polarity and work function difference.

inary experiments indicate that this "bending" of the $+V_g$ curves can be attributed to electron trapping in the oxide. It has also been suggested that depletion of the n+ polysilicon may play a role [2].

Thickness Effects

The data in Table 1 should only be considered accurate for oxide thicknesses less than 20 nm. As oxide thickness increases, we observe that the onset of Fowler-Nordheim tunneling in the $-V_g$ polarity moves toward lower electric fields. This is illustrated in Figure 3. The devices used to generate Figure 3 are from the same technology as those used to generate Figure 2. A comparison of the two figures shows that the low field voltage difference between the positive and negative polarity I_g-V_g curves has started to narrow when oxide thickness reaches 20 nm. Capacitors with oxide thickness of 35 nm actually show the onset of Fowler-Nordheim tunneling at a lower voltage in the $-V_g$ polarity than in the $+V_g$ polarity, a result which is opposite that expected when one considers

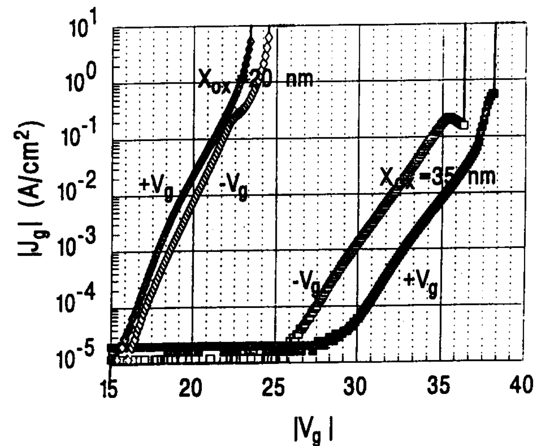

Fig. 3 The onset of Fowler-Nordheim tunneling moves toward lower electric field as oxide thickness increases for devices biased with $-V_g$. Samples were 5μx5μ p-type capacitors with n+ poly gates.

work function and band bending effects. We hypothesize that the movement of the $-V_g$ curves toward lower voltages is due to cathode field enhancement at the poly-oxide interface. If the poly-oxide interface causes a percentage field enhancement, then this field enhancement would only be noticeable on an I_g-V_g curve for thick oxides. This theory implies that the effect should be process dependent which is indeed what we observe. Figure 4 shows an I_g-V_g plot for n-MOSFETs with X_{ox} = 30 nm from a different technology. The movement of the $-V_g$ curve toward lower voltages is significant but not as dramatic as that shown for the 35 nm samples in Figure 3.

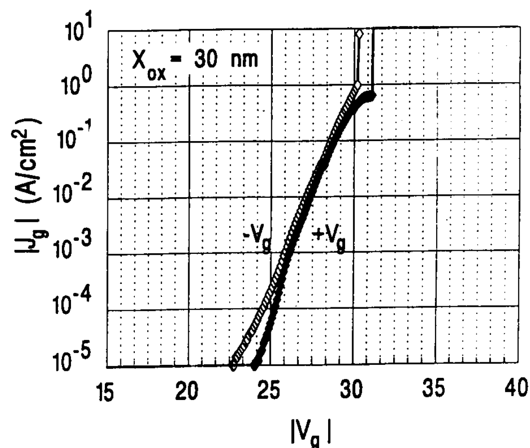

Fig. 4 I-V data for thick oxide devices from another lab show that the results in Figure 3 are process dependent. Samples used are n-MOSFETs with n+ poly gates.

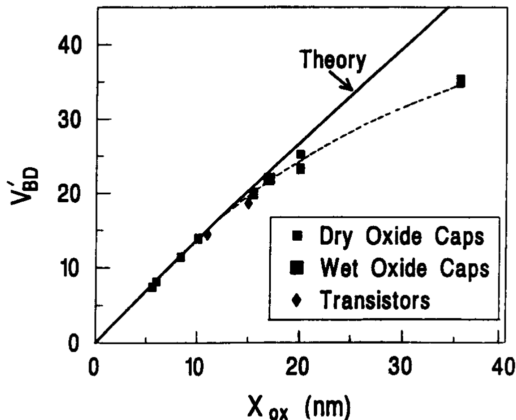

Fig. 5 The V_{BD} values from Figure 1 are replotted as V'_{BD} taking into account the 1.2 volt difference between $V_{applied}$ and V_{ox}. Good agreement is obtained between theory and experiment for thin oxides.

Figure 5 shows the V_{BD} data from Figure 3 replotted using the information in Table 1. Good agreement is obtained between theory and experiment for thin oxides, but for oxides thicker than 15 nm, the data diverges from theoretical projections. Figure 6 indicates the reason; it shows that the I_g-V_g characteristics for thick oxides diverge from Fowler-Nordheim theory at high fields. Thicker oxides break down at a lower "applied" electric field than do thin oxides, but at roughly the same current density. This indicates that the cathode electric field, which determines current density, is the same for thin and thick (up to 20 nm) oxides. Presumably, holes are generated and trapped under high electric field, thus increasing the electric field near the cathode over the value of the "applied" field [3]. This modification of the cathode electric field increases with oxide thickness [4]. The theoretical V_{BD} drawn in Figure 5 should be used to project the value of time-to-breakdown (t_{BD}) at normal operating electric fields which are too low to cause significant hole generation. Ref. 1 shows that, for a given X_{ox}, $\log[t_{BD}] \propto V_{BD}$; therefore, failure to correct V_{BD} for the effects of hole trapping may lead to overly conservative projections of t_{BD}.

Figure 7 provides further evidence that the cathode field at breakdown is approximately constant for devices with oxide thickness in the range 5 - 20 nm. Current density at breakdown is plotted as a function of electric field ramp rate for a variety of devices. The devices tested include capacitors and transistors from different laboratories. All the data points fall near the theoretical projection which was determined as follows.

$$R = \frac{E_{BD}^2}{3.5x10^{-9}} \exp\left[-\frac{350}{E_{BD}}\right] \quad (1)$$

(after [1],[5]) where R is the ramp rate in MV/cm-sec and E_{BD} is the electric field at breakdown in

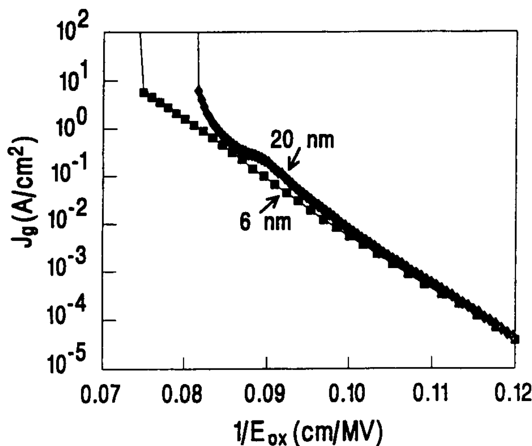

Fig. 6 I-V data transformed to J and $1/E_{ox}$. E_{ox} is equal to V_{ox} (from Table 1) divided by X_{ox}. In contrast with thin oxides, thick oxide I-V characteristics diverge from Fowler-Nordheim theory at high fields due to cathode field modification by trapped holes.

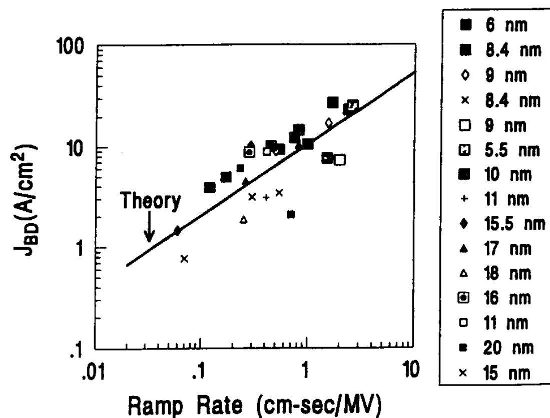

Fig. 7 A comparison of predicted and measured J_{BD}. Shaded symbols represent p-type capacitors, while open symbols represent n-type capacitors. Cross-type symbols represent n-MOSFETs. All devices have n+ poly gates. These results show that while V_{BD} can be misleading due to oxide trapping, J_{BD} provides the expected results.

MV/cm. We also use the Fowler-Nordheim equation,

$$J = 1.25x10^6 E_{ox}^2 \exp\left[-\frac{240}{E_{ox}}\right] \quad (2)$$

where E_{ox} is in MV/cm and J is in A/cm^2. Equation (1) is solved for E_{BD} as a function of ramp rate; the result is substituted into equation (2) to obtain J_{BD}. A comparison of equations (1) and (2) reveals that ramp rate and J_{BD} are approximately related via a power law relation with slope equal to .69 $(=\frac{240}{350})$.

The scatter of the data in Figure 7 is random with respect to both oxide thickness and polarity. This and the good agreement of the data with the theoretical projection, indicate that the physical model for oxide breakdown, as quantified in equation (1), is valid despite the low values of measured V_{BD}.

Polarity Dependence of Defect Distribution

When characterizing oxide defects with ramp voltage breakdown or constant voltage time-to-breakdown tests, it is common to choose the test polarity for convenience alone, *e.g.*, to avoid deep depletion. Figure 8 shows the importance of characterizing the oxide defect distribution using the same bias polarity as expected during circuit operation because the defect distribution obtained is dependent on polarity. This result is not unexpected as the two interfaces are different.

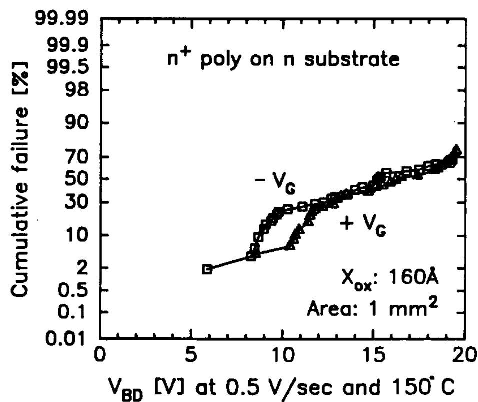

Fig. 8 Defect distribution is dependent on the polarity of the applied bias.

Unipolar and Bipolar Stress

Another difference between conditions during oxide testing and those during circuit operation is the waveforms applied to the oxide. To study this, devices were stressed under unipolar and bipolar conditions at a range of frequencies from DC up to 4 MHz. The goal was to determine if lifetime under AC conditions could be projected from that under static conditions simply by accounting for the duty factor. Results of this experiment are shown in Figure 9. n-MOSFETs were used for this experiment to avoid deep depletion when $+V_g$ stress was applied. The frequency range was limited by the requirement that clean waveforms be obtained. Figure 10 shows an oscilloscope trace of the waveform used to conduct bipolar stressing at 1 MHz. The values of $+V_g$ and $-V_g$ used in this experiment were selected such that the devices had approximately equal DC lifetimes in both polarities. As explained earlier in this paper, this requires using a smaller voltage value in the $+V_g$ polarity.

Under unipolar conditions, t_{BD} (defined to be the product of the experiment duration and the duty cycle) is seen to be, at most, a weakly increasing function of frequency. It is, therefore, reasonable to use the measured value of DC lifetime and the duty cycle to project the lifetime of oxide under unipolar AC conditions. The projection will be somewhat conservative (by a factor of 2-3).

However, when a bipolar signal is applied, t_{BD} increases dramatically as frequency increases.

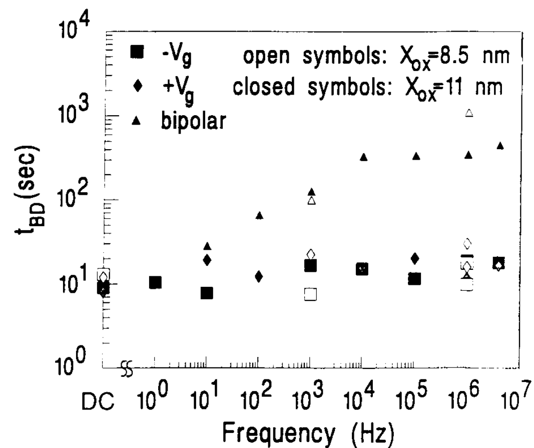

Fig. 9 Time-to-breakdown is longer under bipolar stress than under DC or unipolar pulse stress. Positive and negative voltage levels were kept constant as frequency was increased. t_{BD} is equal to experiment duration multiplied by duty cycle.

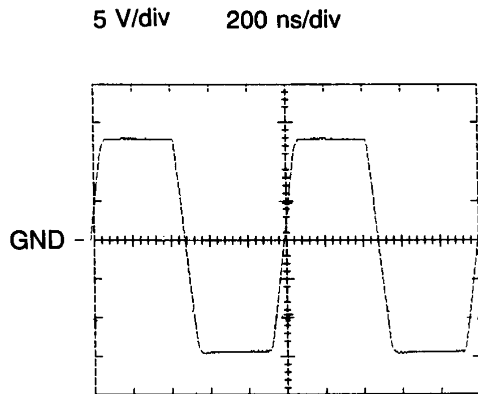

Fig. 10 The waveform used to determine t_{BD} for the 11 nm devices under bipolar conditions at 1 MHz. A clean waveform was obtained at all frequencies studied.

Around 10 KHz, the increase in lifetime saturates. The increase in lifetime was a factor of 40 for transistors with X_{ox} = 11 nm and a factor of 100 for transistors with X_{ox} = 8.5 nm. We believe that the increase in lifetime is caused by a reduction in the steady- state trapped hole density in the oxide [6].

In a circuit environment, it is generally only the drain-gate overlap region which will experience bipolar stress. We conclude that a quasi-static approach to calculating oxide lifetime is valid in most cases. Such a quasi-static approach is used by the Berkeley Reliability Tools to generate oxide breakdown projections for circuits [7].

Conclusions

In order to make accurate projections of oxide reliability from accelerated tests, the effects described herein need to be incorporated. These include the dependence of breakdown voltage on signal polarity and oxide thickness. Furthermore, consideration should be paid to the waveform which will be applied to the oxide in a circuit environment, before projecting lifetime from DC tests.

Acknowledgments

This research is sponsored by SRC, Sandia Laboratories, AMD, MICRO, and ISTO/SDIO under contract N00014-85-K-0603.

References

[1] I.C. Chen et al., *Proc. IRPS*, p. 24, 1985.

[2] B. J. Fishbein and D. B. Jackson, *Proc. IRPS*, p. 159, 1990.

[3] Y. Nissan-Cohen et al., *Solid State Electronics*, vol. 28, no. 7, p. 717, 1985.

[4] Y. Nissan-Cohen et al., *J. Appl. Phys.*, vol. 57, no. 8, p. 2830, 1985.

[5] R. Moazzami et al., *IEDM Tech. Digest*, p. 710, 1988.

[6] E. Rosenbaum and C. Hu, to appear in I. Elect. Dev. Let., June 1991.

[7] E. Rosenbaum et al., *IEDM Tech. Digest*, p. 331, 1989.