

# THE EFFECTS OF HOT-ELECTRON DEGRADATION ON ANALOG MOSFET PERFORMANCE

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## ABSTRACT

This paper presents a study of the effects of hot-electron degradation on analog MOSFET performance. First, an overview is presented of how hot-electron degradation affects many common analog performance parameters such as drain output resistance, device matching, and flicker noise. Next, hot-electron-induced degradation in NMOS drain output resistance is examined in detail; physical models and techniques for evaluating device reliability are developed. Finally, how NMOS drain output resistance degradation affects the performance of a CMOS single-ended output differential amplifier is analyzed.

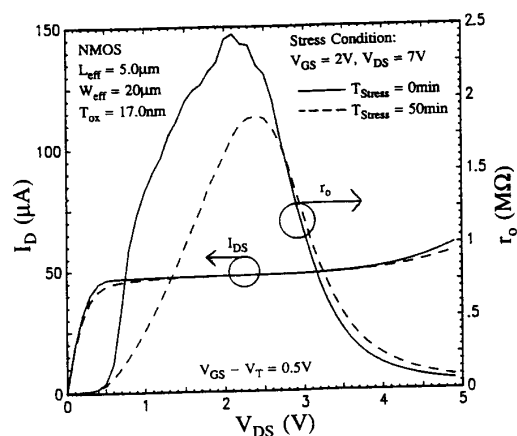
## INTRODUCTION

Because hot-electron degradation imposes limits on ULSI scaling, its characteristics and physical mechanisms have been extensively studied [1-6]. The effect of hot-electron degradation on MOSFETs operating in digital circuit and memory cell applications has also been examined [7-12]. Analog circuits, which are sensitive to device parameter variation, are expected to be strongly affected by hot-electron degradation. However, the hot-electron reliability of MOSFETs performing analog functions has been the subject of only limited study, primarily focusing on design methods to bypass the problem (at the expense of additional circuit area and complexity) [13]. In this paper, a study of the effects of hot-electron degradation on analog MOSFET performance is presented.

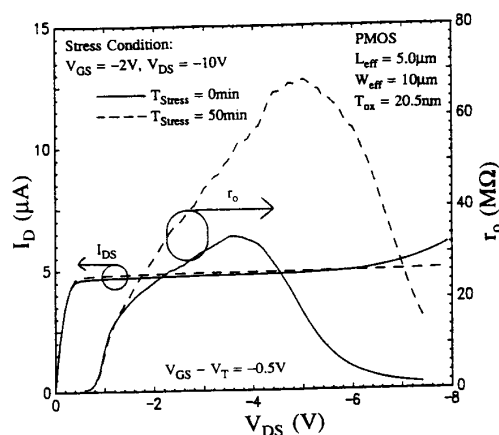
The NMOS and PMOS non-LDD surface-channel transistors examined in this study were fabricated using a LOCOS-isolated, single-metal process [14]. The NMOS dimensions range from  $L_{eff} = 1.0 - 10.0\mu\text{m}$  and from  $T_{ox} = 5.6 - 17.0\text{nm}$ . The PMOS dimensions are  $L_{eff} = 5.0\mu\text{m}$  and  $T_{ox} = 20.5\text{nm}$ . For many analog parameter measurements, the devices were biased at  $V_{DS} = \pm 1$  and at  $V_{GS} = V_T \pm 0.3\text{V}$ . This roughly approximates the quiescent bias conditions typically seen by MOSFETs performing many analog functions. To distinguish between fresh and stressed parameters in this study, the subscript "0" is used to denote the original unstressed parameter.

## ANALOG MOSFET PERFORMANCE DEGRADATION

**Drain Output Resistance  $r_o$ :** Figs. 1a and 1b show that hot-electron degradation affects drain output resistance for NMOS and PMOS devices quite differently. The NMOS  $r_o$  decreases for  $0.5\text{V} < V_{DS} < 2.5\text{V}$ ; whereas, the PMOS  $r_o$  increases for  $V_{DS} < -0.5\text{V}$ . Note that hot-electron stress can significantly alter  $r_o$  even though little change in the I-V characteristic may be apparent; this is true even for long-channel devices stressed under moderate conditions. The large variations in drain output resistance shown in Fig. 1 are directly reflected in the small-signal voltage gain  $g_m \times r_o$  (Fig. 2).



(a)



(b)

Figure 1. Drain current  $I_D$  and drain output resistance  $r_o$  characteristics before and after hot-electron stressing for (a) NMOS and (b) PMOS transistors.

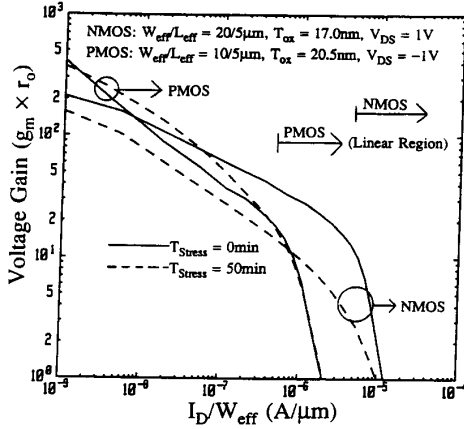


Figure 2. NMOS and PMOS small-signal voltage gain  $g_m \times r_o$  before and after hot-electron stressing. Stress conditions are identical to those in Figs. 1a-b.

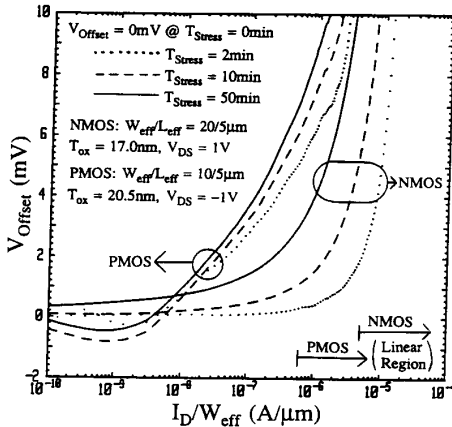


Figure 3. NMOS and PMOS differential offset voltage  $V_{offset}$  between fresh and stressed devices. Stress conditions are identical to those in Figs. 1a-b.

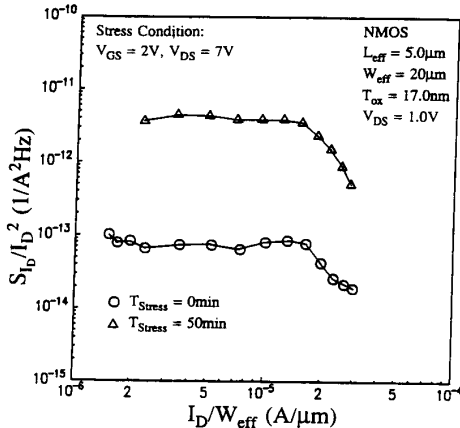


Figure 4. Normalized NMOS drain current noise  $S_{I_D}/I_D^2$  before and after hot-electron stressing.

Simple physical explanations exist for the observed changes in  $r_o$ . NMOS hot-electron damage is primarily acceptor-type interface states created near the drain [1-5]. At low  $V_{DS}$ , the states are occupied and negatively charged; this lowers the inversion-layer mobility which reduces  $I_D$ . Increasing  $V_{DS}$  lowers the quasi-fermi level near the drain which empties the states; this raises  $I_D$  which approaches its original unstressed value. The additional  $I_D$  with increasing  $V_{DS}$  results in a reduced NMOS  $r_o$ .

When a MOSFET enters the saturation region, the increase in  $r_o$  is governed by channel-length modulation and drain-induced-barrier-lowering. As  $V_{DS}$  is raised further, hot-carrier effects become significant, reducing  $r_o$  [15]. PMOS hot-electron damage is primarily fixed electron traps [6]. These traps diminish the drain lateral electric field causing the onset of hot-carrier effects to occur at higher  $V_{DS}$ . Thus, the peak PMOS  $r_o$  moves to higher  $V_{DS}$  and increases in magnitude.

**Device Matching:** For many analog applications, device matching is a major concern. Consider a "virtual" differential pair where a fresh MOSFET is matched in a source-coupled configuration with a stressed version of itself after having undergone hot-electron degradation. The offset voltage is defined as the difference in gate bias required to sustain a particular  $I_D$  for a fixed  $V_{DS}$  between the original and degraded versions of the device. The use of a "virtual" differential pair (where for  $T_{Stress} = 0$ ,  $V_{Offset} = 0$ ) separates the effects of hot-electron degradation from other factors that may affect  $V_{Offset}$ .

Fig. 3 shows that  $V_{Offset}$  is a sensitive function of  $I_D$ . The offset voltage can be modeled as [16]

$$V_{Offset} = \pm \Delta V_T - (I_D/g_m) \times \Delta \mu_{eff}/\mu_{eff} \quad (1)$$

where  $\Delta V_T = V_T - V_{T0}$ ,  $\Delta \mu_{eff} = \mu_{eff} - \mu_{eff0}$ , and the  $\pm$  sign applies to NMOS and PMOS devices respectively. For small  $I_D$ ,  $V_{Offset}$  is due primarily to change in the inversion-layer charge density; for large  $I_D$ ,  $V_{Offset}$  is due primarily to inversion-layer mobility degradation. For NMOS devices,  $\Delta V_T > 0$  and  $\Delta \mu_{eff} < 0$  [1-5]; from Eq. 1,  $V_{Offset} > 0$  for all  $I_D$ . For PMOS devices,  $\Delta V_T > 0$  and  $\Delta \mu_{eff} < 0$  [6]; from Eq. 1,  $V_{Offset} < 0$  for small  $I_D$  and  $V_{Offset} > 0$  for large  $I_D$ . Fig. 3 displays these dependencies.

**Drain Current Flicker Noise:** In Fig. 4, NMOS normalized drain current flicker noise is observed to increase significantly after undergoing hot-electron degradation. This additional  $1/f$  noise arises from hot-electron-generated interface states which induce fluctuations in the inversion-layer charge density and mobility [17,18].

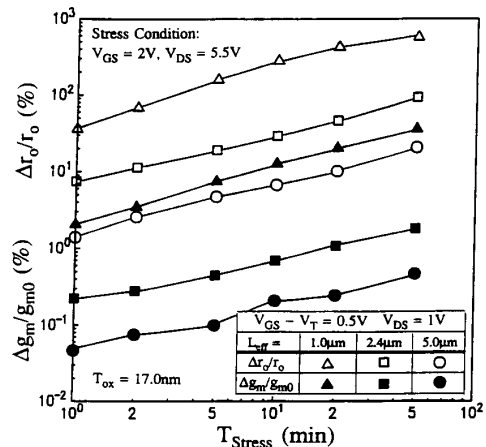


Figure 5. Drain output resistance  $\Delta r_o/r_o$  and transconductance  $\Delta g_m/g_{m0}$  degradation as a function of  $T_{Stress}$ .

### DRAIN OUTPUT RESISTANCE $r_o$ DEGRADATION

**Characteristics of  $r_o$  Degradation:** Next, this study concentrates on characterizing and modeling the hot-electron degradation of NMOS drain output resistance. In Fig. 5,  $\Delta r_o/r_{o0}$  and  $\Delta g_m/g_{m0}$  both have time dependences of the form  $T_{Stress}^n$ , where  $n \approx 0.6$ . Fig. 5 also indicates that degradation in the NMOS small-signal voltage gain (Fig. 2) is primarily due to degradation in  $r_o$  rather than in  $g_m$ . The correlation between  $\Delta r_o/r_{o0}$  and the increase in charge-pumping current  $\Delta I_{CP}$  shown in Fig. 6 supports the concept that interface-state generation is responsible for the  $r_o$  degradation. In addition, Fig. 6 also indicates that  $I_{Sub}$  can be used to monitor the severity of the hot-electron stress. A semi-empirical hot-electron degradation model has been developed which relates device lifetime to  $I_{Sub}$  and  $I_D$  [1]

$$\tau \times (I_D/W_{eff}) \propto (I_{Sub}/I_D)^{-3} \quad (2)$$

Figs. 7a and 7b display lifetime correlation plots for differing  $L_{eff}$  and  $T_{ox}$ . Overall, Figs. 5-7 suggest that existing hot-electron reliability concepts and lifetime prediction models appear applicable to  $r_o$  degradation.

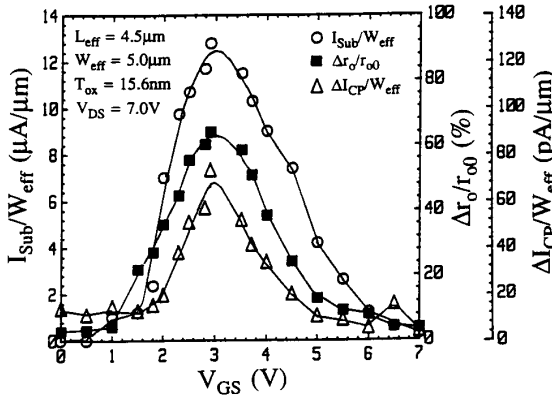


Figure 6. Correlation between  $\Delta r_o/r_{o0}$ ,  $\Delta I_{CP}/W_{eff}$ , and  $I_{Sub}/W_{eff}$ .

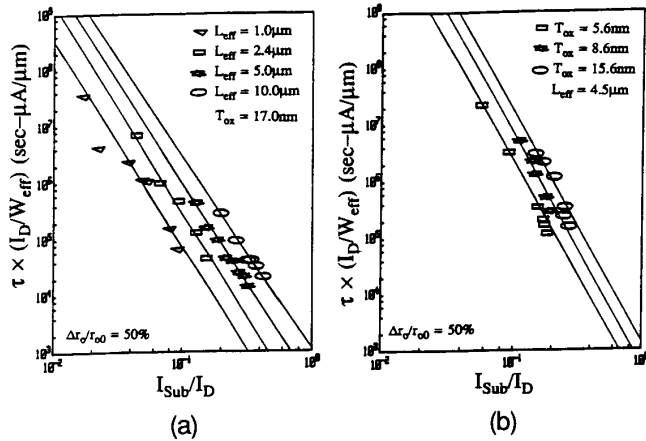


Figure 7. Lifetime correlation plots (a) for different  $L_{eff}$ , (b) for different  $T_{ox}$ . Lifetime is defined as  $\Delta r_o/r_{o0} = 50\%$ .

**Relation between  $\Delta r_o/r_o$  and  $\Delta I_D/I_{D0}$ :** Fig. 8 displays a correlation between drain output resistance degradation and linear current degradation. MOSFETs with different  $L_{eff}$  were stressed under identical bias conditions. The lines indicate contours of constant  $T_{Stress}$ . Using Fig. 8, the relative importance of hot-electron degradation for a device of a particular  $L_{eff}$  performing a digital application can be compared with another device of a different  $L_{eff}$  performing an analog application.

**A Model for  $r_o$  Degradation:** A semi-empirical model for NMOS drain output resistance degradation can be developed. In Fig. 1a, as  $V_D$  is increased, the degraded  $I_D$  is observed to merge with the original  $I_D$ . Let the functions  $I_{D0}(V_D)$  and  $I_D(V_D)$  represent the drain currents for the fresh and stressed devices respectively. Define  $V_{D1}$  as the drain bias at which  $r_o$  is determined; define  $V_{D2}$  as the drain bias at which  $I_{D0}(V_{D2}) \approx I_D(V_{D2})$ . The original and degraded output resistances, and their difference can be approximated as

$$r_{o0} \approx (V_{D2} - V_{D1}) / (I_{D0}(V_{D2}) - I_{D0}(V_{D1})) \quad (3)$$

$$r_o \approx (V_{D2} - V_{D1}) / (I_D(V_{D2}) - I_D(V_{D1})) \quad (4)$$

$$\Delta r_o = r_{o0} - r_o = \left[ \frac{(V_{D2} - V_{D1}) \Delta I_D}{(I_{D0}(V_{D2}) - I_{D0}(V_{D1})) (I_D(V_{D2}) - I_D(V_{D1}))} \right] \quad (5)$$

where  $\Delta I_D = I_{D0}(V_{D1}) - I_D(V_{D1})$ . Combining Eqs. 3-5 yields

$$\Delta I_D \propto \Delta r_o / (r_{o0} r_o) \approx \Delta r_o / r_{o0}^2 \quad (6)$$

This correlation is shown in Fig. 9.

### DIFFERENTIAL AMPLIFIER GAIN DEGRADATION

The impact of NMOS  $r_o$  degradation on the performance of a CMOS single-ended output differential amplifier was analyzed using the hot-electron circuit reliability evaluation program BERT [19]. Figs. 10a and 10b show the circuit diagram and the simulated voltage/current waveforms ( $V_{CC} = 5V$ ,  $T_{Cycle} = 80ns$ , Input Ramp Rate = 20ns/V). Significant substrate current (and hot-electron stress) is present only during voltage transitions. For the voltage waveforms shown in Fig. 10b, only transistor M4 experiences any significant hot-electron degradation.

For the differential amplifier in Fig. 10a, the percent degradation in gain can be written as

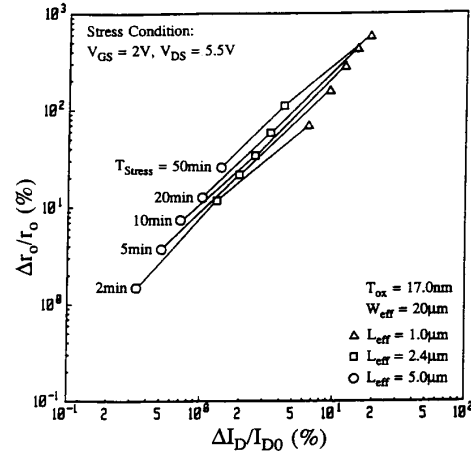


Figure 8. Correlation between  $\Delta r_o/r_o$  and  $\Delta I_D/I_{D0}$  for different  $L_{eff}$ . The lines indicate contours of constant  $T_{Stress}$ .

$$\frac{\Delta G}{G_0} \approx \frac{g_{o0n}}{g_{o0n} + g_{o0p}} \times \frac{\Delta r_{o0n}}{r_{o0n}} \quad (7)$$

where  $g_{o0n}$  and  $g_{o0p}$  are the NMOS and PMOS drain conductances. Assuming an ideal PMOS load,  $g_{o0p} \ll g_{o0n}$  and

$$\Delta G/G_0 \approx \Delta r_{o0n}/r_{o0n} \quad (8)$$

BERT was used to calculate the amount of  $r_o$  degradation for each transistor. Eq. 8 was then used to estimate the differential amplifier gain degradation after 10 years of operation (Fig. 11).

Care must be taken in determining the hot-electron reliability of dynamically-operated circuits from the static degradation of individual devices. Consider Fig. 7a which shows that  $\Delta r/r_o$  worsens as  $L_{eff}$  is reduced for devices with the same amount of hot-electron stress. However, for the differential amplifier in Fig. 10a, the common-source node voltage decreases as  $I_{bias}$  and/or  $L_{eff}$  increases. This causes a larger  $V_{DS}$  to appear across M4 and increases the duration of the hot-electron stress; M4 is consequently subjected to greater hot-electron degradation. Thus,  $\Delta G/G_0$  worsens with increasing  $I_{bias}$  and/or longer  $L_{eff}$  as shown in Fig. 11. This example illustrates the necessity of accounting for the details of a particular circuit design and its exact mode of operation when evaluating circuit-level hot-electron reliability.

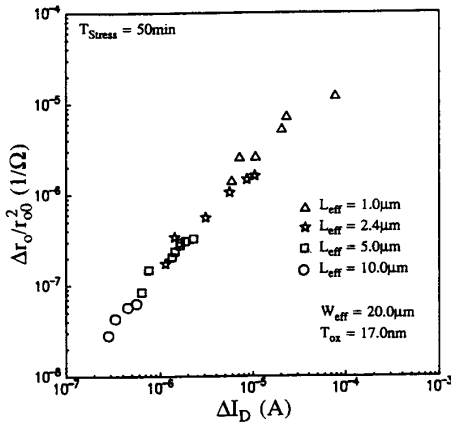


Figure 9. Correlation between  $\Delta r_o/r_{o0}^2$  and  $\Delta I_D$  for different  $L_{eff}$ .

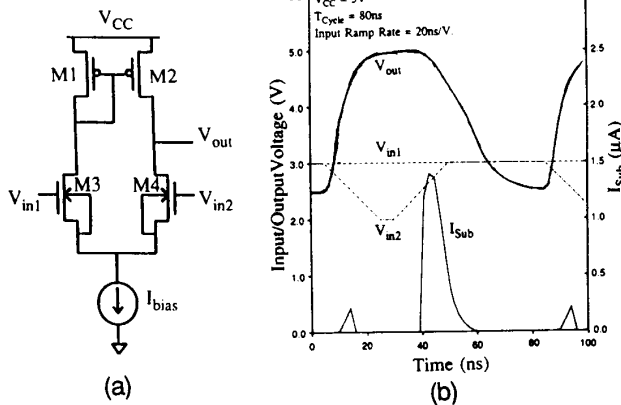


Figure 10. (a) Circuit diagram of a CMOS single-ended output differential amplifier. (b) Simulated input/output voltage waveforms and the substrate current of transistor M4.

## CONCLUSION

Many analog MOSFET performance parameters have been found to be very sensitive to hot-electron stress especially compared with digital parameters that are normally monitored. Drain output resistance degradation has been characterized in detail using existing hot-electron reliability concepts and lifetime prediction models. The impact of  $r_o$  degradation on the performance of a CMOS single-ended output differential amplifier has been found to be a sensitive function of the particular circuit design and operating conditions.

## ACKNOWLEDGEMENT

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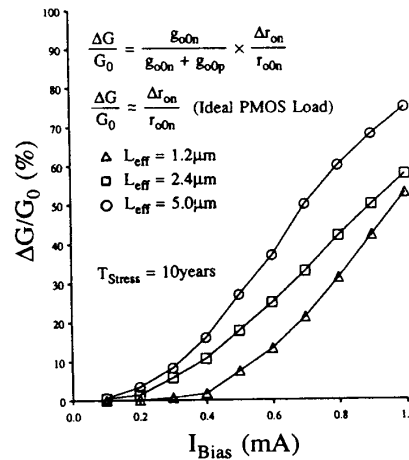


Figure 11. Simulated differential amplifier gain reduction  $\Delta G/G_0$  as a function of the bias current  $I_{bias}$  for different  $L_{eff}$ .