FLICKER NOISE CHARACTERISTICS OF ADVANCED MOS TECHNOLOGIES

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ABSTRACT

The flicker noise behaviours of MOSFETs fabricated by different technologies have been characterized. It is found that the technology has very significant influence on the noise characteristics. Random telegraph noise is observed in some deep submicron MOSFETs with very small channel area. A detailed analysis of the telegraph noise suggests that the mobility fluctuation induced by charge trapping plays an important role in the origin of the flicker noise. A new flicker noise model incorporating both carrier number and mobility fluctuations is proposed.

INTRODUCTION

Recently the flicker (1/f) noise characteristics of MOSFETs have received increasing attention due to their widespread application in the area of analog integrated circuits [1]. It is generally believed that the oxide trap induced carrier number fluctuation lies the origin of the flicker noise [2]. However, a coherent picture on the overall noise characteristics has not yet emerged. Specially, there are controversies on their bias and technology dependence. In this paper we shall report our extensive effort on characterizing the noise behaviour of MOSFETs fabricated by different technologies . The effects of hot-carrier stressing on the noise characteristics will also be addressed. For deep submicron devices with very small channel area, the conventional flicker noise may reduce to discrete drain current fluctuations resembling a random telegraph signal [3]. Our detailed study of the telegraph noise reveals that the oxide trap induced mobilitity fluctuation plays an equally important role in the origin of the flicker noise. In the next section, we shall present a new flicker noise model taking into account both the carrier number and mobility fluctuations.

A NEW FLICKER NOISE MODEL

Consider a section of channel with width W and length Δx. A fluctuation of the trapped oxide charge will induce CORRELATED fluctuations in channel carrier number and mobility. Mathematically,

$$\frac{\delta I_d}{I_d} = \left[\frac{1}{\Delta N}\frac{\delta \Delta N}{\delta \Delta N_t} + \frac{1}{\mu}\frac{\delta \mu}{\delta \Delta N_t} \right] \delta \Delta N_t \ , \tag{1}$$

where $\Delta N = NW\Delta x$, $\Delta N_t = N_t W \Delta x$, N and N_t are respectively the number of channel carriers and occupied traps per unit area. A generally accepted mobility model is [4]

$$\frac{1}{\mu} = \frac{1}{\mu_0} + \frac{1}{\mu_I} = \frac{1}{\mu_0} + \alpha N_t \ , \tag{2}$$

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where μ_I is the mobility limited by oxide charge scattering. It is expected that the scattering coefficient α is bias dependent due to carrier screening effect. Using (2) and noting that $\delta\Delta N/\delta\Delta N_t \approx -1$ in moderate to strong inversion [5], (1) can be rewritten as

$$\frac{\delta I_d}{I_d} = -\left(\frac{1}{N} + \alpha\mu\right)\frac{\delta \Delta N_t}{W\Delta x} \ ,$$

or

$$S_{\Delta I_d}(f) = \frac{I_d^2}{W^2\Delta x^2}\left(\frac{1}{N}+\alpha\mu\right)^2 S_{\Delta N_t}(f) = \frac{I_d^2}{W\Delta x}\left(\frac{1}{N}+\alpha\mu\right)^2 \frac{N_T(E_F)kT}{\gamma f} \ , \tag{3}$$

where $N_T(E_F)$ is the oxide trap density at the quasi-Fermi level and $\gamma \approx 10^8 cm^{-1}$ is the tunneling constant. It turns out that the drain current noise power is [6]

$$S_{I_d}(f) = \frac{1}{L^2}\int_0^L S_{\Delta I_d}(f)\Delta x dx = \frac{kTI_d^2}{\gamma f W L^2}\int_0^L N_T(E_F)\left[\frac{1}{N(x)}+\alpha\mu\right]^2 dx \ , \tag{4}$$

where L is the channel length. Since $N_T(E_F)$, α, and μ are bias dependent, (4) may be written in an semi-empirical form as

$$S_{I_d}(f) = \frac{kTI_d^2}{\gamma f W L^2}\int_0^L \frac{A+BN+CN^2}{N^2} dx \ , \tag{5}$$

where A,B,C are technology dependent model parameters. A,B,C can be determined by fitting the measured noise data with (5). It is noted that $A+BN+CN^2$ is the apparent oxide trap density extracted from the noise measurement if one ignores the contributions from the mobility fluctuation.

FLICKER NOISE CHARACTERISTICS OF DIFFERENT MOS TECHNOLOGIES

Fig.1 shows the bias dependence of the drain current noise power of an n-MOSFET fabricated by a conventional 3μm CMOS technology (T_{ox}=50nm, $N_B=1.5\times10^{15}cm^{-3}$). It is noted that the noise power is almost independent of the gate voltage in the linear region. In contrast, the noise power for another MOSFET fabricated by a deep submicron technology (T_{ox}= 8.6nm, $N_B=5\times10^{17}cm^{-3}$) shows significant dependence on the gate voltage, as shown in Fig.2. These results demonstrate that the technology can have very significant impact on the noise characteristics. To explain the difference in bias dependence, we extracted the apparent oxide trap density from the noise data for the two technologies and plotted the results in Fig.3. The apparent density serves as a good estimate of the real density. Due to the use of thin gate oxide and high substrate doping, the traps

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that are contributing to the flicker noise of the deep submicron technology are those with energy near the bandedge. The bias dependence of the noise power is a direct consequence of the non-uniform oxide trap distribution over the bandgap. Solid lines in Fig.1 and 2 are model predictions based on Eqn.(5) and the extracted oxide trap density.

The situation for p-MOSFETs is slightly more complicated. For those with a surface channel, the noise characteristics are similar to those of n-MOSFETs and can be well predicted by our model (Fig.4). However, for those with a buried channel, there may be an additional noise source which is important at the onset of inversion. Fig.5 shows the noise characteristics of a p-MOSFET on a CMOS wafer which is a buried channel device. The additional noise source is believed to be the generation-recombination noise arising from the substrate defect centers which were introduced during boron implantation [7]. In general p-channel devices have noise levels one to two orders of magnitude lower than those of n-channel devices. This can be attributed to the different tunneling barrier heights for electrons and holes, different oxide trap density near the conduction and valence bandedge, and different electron and hole mobility resulting in different degree of mobility fluctuation.

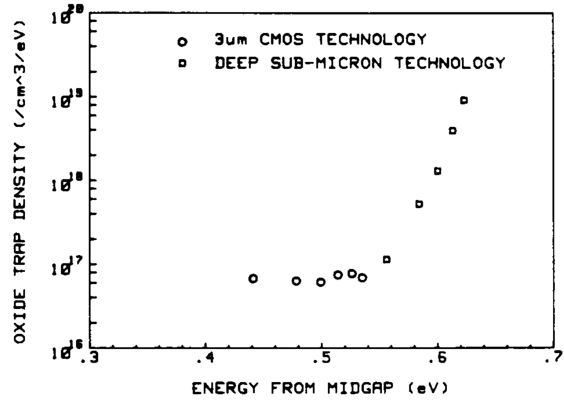


FIG.3. Apparent oxide trap density vs. energy for the 3μm CMOS and deep submicron technologies.

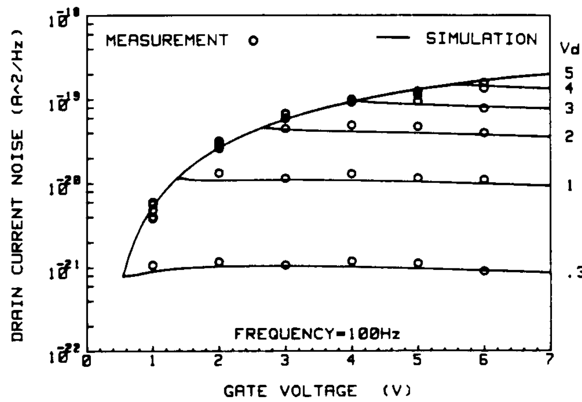


FIG.1. Bias dependence of the drain current noise power of an n-MOSFET fabricated by a conventional 3μm CMOS technology (W=9.5μm, L=4.5μm). The measured data (circles) are compared with the model prediction (lines).

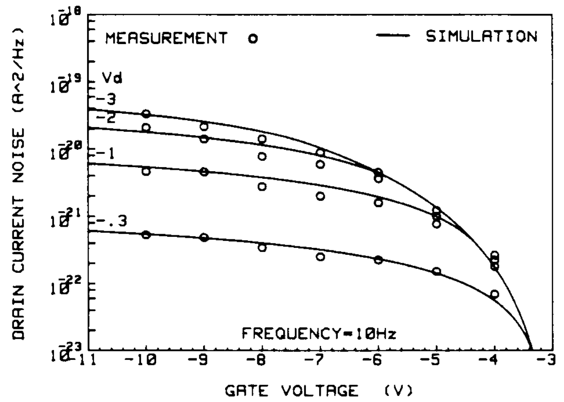


FIG.4. Bias dependence of the drain current noise power for a surface-channel p-MOSFET (T_{ox}=43.5nm, N_B= $3\times10^{16}cm^{-3}$, W=4 μm, L=5μm). The measured data (circles) are compared with the model predictions (lines).

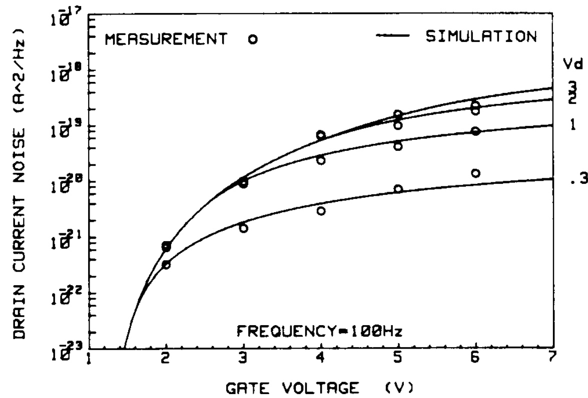


FIG.2. Bias dependence of the drain current noise power of an n-MOSFET fabricated by a deep submicron technology (W=L=4.5μm). The measured data (circles) are compared with the model prediction (lines).

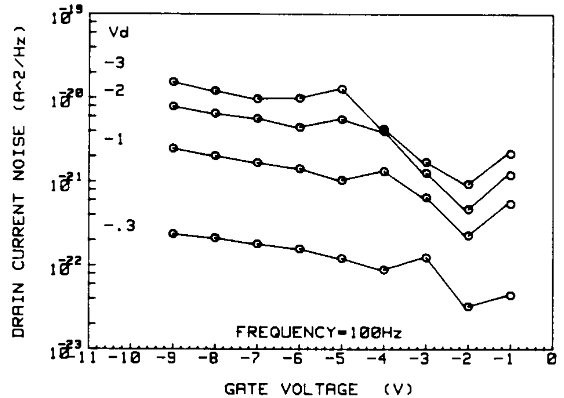
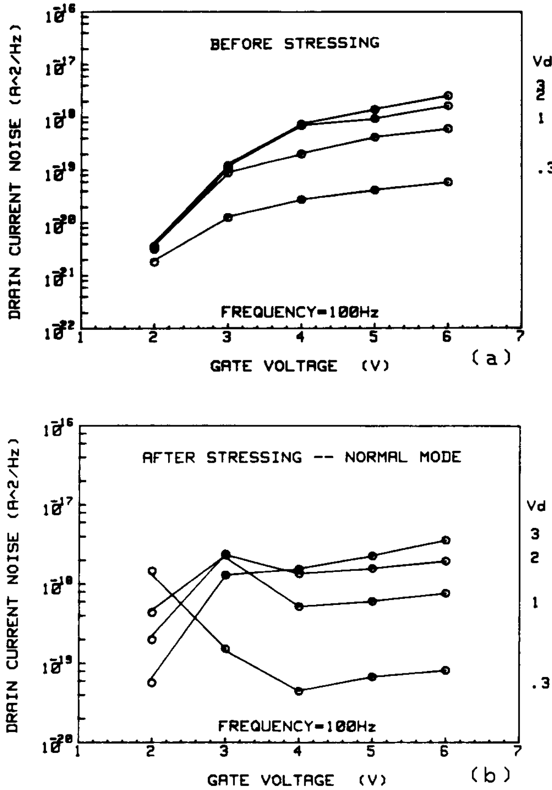


FIG.5. Bias dependence of the drain current noise power for a buried-channel p-MOSFET (T_{ox}=55.5nm,W=3.2μm, L=2μm).

EFFECTS OF HOT CARRIER STRESSING ON FLICKER NOISE CHARACTERISTICS

It is well known that hot carrier stressing can introduce MOSFET degradation through the generation of new interface traps [8]. Flicker noise measurement can provide additional insight on the degradation mechanism. We found that for n-MOSFETs an hot-carrier stressing that causes a 0.1V threshold voltage shift can increase the noise power at low gate bias by one to two orders of magnitude, whereas for p-MOSFETs the noise is hardly affected even after a stressing that caused a considerable threshold shift. Fig.6 shows the noise characteristics before and after stressing for an n-MOSFET fabricated by a deep submicron technology (T_{ox}=8.6nm, W=4.5μm, L=1.5μm). The device was stressed at V_g=2.3V, V_d=4.5V, and $I_{sub.}$=130μA for 60 min resulting in a threshold shift of 0.2V. The data in Fig.6c were taken with the drain and source reversed during measurement. Comparison of the noise data measured in the "normal" and "reverse" modes clearly reveals that the demage due to stressing is localized in the drain end of the channel. The increase in noise power at low gate bias indicates that the density of the generated traps have peaks below the conduction energy bandedge.



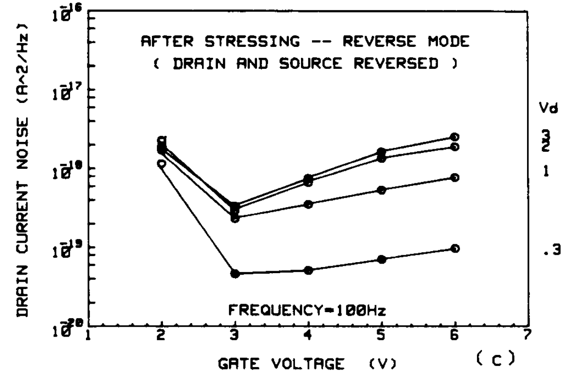


FIG.6. The effects of hot-electron stressing on the flicker noise characteristics of an n-MOSFET. (a) Before stressing. (b) and (c) After stressing. The results in (c) are obtained with the drain and source reversed during noise measurement.

RANDOM TELEGRAPH NOISE OF DEEP SUBMICRON DEVICES

For MOSFETs with very small channel area (<= 1μm^2), it is possible to have only one single active oxide traps over the entire channel at certain bias. Trapping and detrapping of a single carrier cause discrete current fluctuation generating random telegraph noise [3]. A detailed study of the telegraph noise may lead to a better understanding of the trapping mechanism and provides hints to a proper modeling of the flicker noise. Of particular interest is the bias dependence of the relative amplitude ($\Delta I_d/I_d$) and the mark-space ratio of the I_d fluctuation. The latter is in fact the ratio of the mean capture time (τ_c) to the mean emission time (τ_e) [3]. The theoretical expressions for these parameters are:

$$\frac{\Delta I_d}{I_d} = \frac{1}{WL}\left(\frac{1}{N} + \alpha\mu\right) , \tag{6}$$

and

$$\frac{\tau_c}{\tau_e} = g \exp\frac{E_T - E_F}{kT} , \tag{7}$$

where g is the trap degeneracy and $E_T - E_F$ is the trap energy relative to the quasi Fermi level. For direct comparison with measurement, (7) may be rewritten as

$$\ln\frac{\tau_c}{\tau_e} = K - \frac{q}{kT}\left[(1-\frac{z}{T_{ox}})\psi_s + \frac{z}{T_{ox}}V_g\right] , \tag{8}$$

where z is the distance of the trap from the interface, ψ_s is the surface potential, and K is a constant.

Fig.7 shows the I_d fluctuations of a deep submicron n-MOSFET (W=1.2μm, L=0.35μm) at different gate biases. The bias dependence of $\Delta I_d/I_d$ is shown in Fig.8. The scattering coefficient α extracted from the measured $\Delta I_d/I_d$ is plotted as a function of carrier density in Fig.9. The solid line is the best fit with the empirical expression :

$$\alpha = K_1 + K_2 \ln N . \tag{9}$$

Eqn.(9) has a functional form resembling the Conwell-Weisskopf formula for a screened coulomb scatterer [9]. It is interesting to note that the magnitude of α is consistent with the values used in modeling the oxide charge scattering effect in conventional mobility models [4]. These results suggest that the trapped charges generate noise by modulating the mobility through scattering in addition to the carrier number. The bias dependence of τ_c/τ_e is depicted in Fig.10. Fitting of the data with (8) yields z=13A. In general we found that the values of z extracted for different devices may vary from a few A to 20A.

SUMMARY

We have characterized extensively the flicker noise behaviours of MOSFETs fabricated by different technologies. It is found that the technology has very significant effects on the noise characteristics and all the results can be explained within a unified framework with an oxide trap density distribution. Hot carrier stressing of n-channel MOSFETs can result in a tremendous increase of flicker noise, whereas for p-channel MOSFETs the noise is hardly affected. A detailed study of the random telegraph noise exhibited by small channel area MOSFETs provides evidence that the oxide trap induced mobility fluctuation plays an important role in the origin of the flicker noise. A new flicker noise model is developed which incorporates both the carrier number and mobility fluctuations in a correlated manner.

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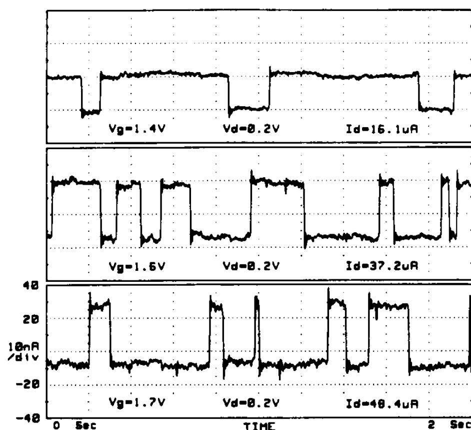

FIG.7. The fluctuations of drain current at different gate voltage for an n-MOSFET with very small gate area (W=1.2μm, L=0.35μm, T_{ox}=8.6nm, N_B=5×10^{17}cm^{-3}).

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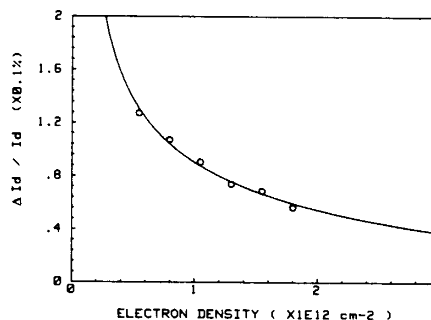

FIG.8. A plot of $\Delta I_d/I_d$ vs. electron density for the device in FIG.7. The solid line is the best fit with Eqns.(6) and (9).

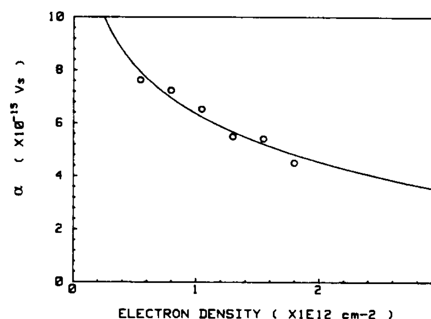

FIG.9. A plot of the extracted scattering coefficient versus electron density. The solid line is the best fit with Eqn.(9).

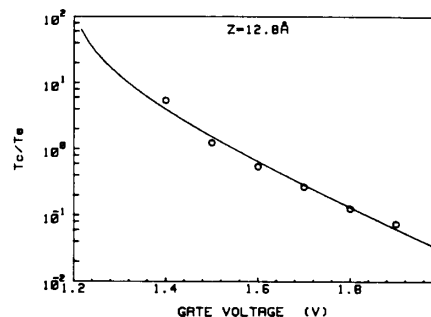

FIG.10.A plot of the mark-space ratio versus electron density. The solid line is the best fit with Eqn.(8).