Reliability Issues of MOS and Bipolar ICs
(Invited Paper)

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ABSTRACT

Reliability issues affecting MOS and bipolar ICs are reviewed. Hot carrier induced degradation of MOS and bipolar circuits are used to illustrate the potential role of reliability CAD tools. Electromigration lifetimes under pulse DC and AC current stressing are longer than previously thought. Oxide breakdown offers a case study for accelerated test modeling, defect statistics, and burn-in optimization.

Introduction

The reliability of memory and logic IC's is affected by many failure mechanisms. A partial list could include

- Electromigration
- Gate oxide breakdown
- Hot carrier induced degradation
- Single event soft error
- Charge drift instability
- Passivation failure
- Mechanical stress effects
- CMOS latchup
- Electrostatic discharge

An excellent source of information on these and other failure mode is the proceedings of the annual IEEE International Reliability Physics Symposium. Electromigration affects both MOS and bipolar components. Voids on protrusions are created in metal interconnect lines and contacts, eventually leading to opens, shorts or leakage problems. The process is accelerated by current density and temperature. Oxide breakdown affects mostly the MOS IC's, particularly those with large oxide areas such as DRAMs and some switched-capacitor analog circuits. Hot carrier induced degradation occurs in MOS transistors as the energetic carriers (electrons and/or holes) damage the interface or are trapped in the oxide near the drain and causes the IV characteristics of the transistor to change. When and if the base emitter junction of a bipolar transistor is reversed biased, hot carriers can cause a permanent decrease in the transistor current gain. These first three failure mechanisms are closely coupled with advanced technology and device development and will be addressed in more details later.

Single event soft error or α-induced soft error mainly affects DRAMs as α generated charges interfere with the storing and sensing of charges in the DRAM circuit. Charge drift is classically associated with N_a and K ions, but other unidentified mobile charge specifies seem to be responsible for the electrical instability in advanced CMOS processes. Passivation layer can have cracks that allow moisture and/or mobile ions to enter the metal/oxide system underneath and cause corrosion and/or instabilities in threshold voltages. Mechanical stress can cause th passivation to crack or cause metal lines to develop void or even to shift their positions on the chip. CMOS latch-up is less of a concern now than in the early 80's when CMOS technologies were becoming a widely practiced technologies. Finally, electrostatic discharge (ESD) remains a serious concern although considerable new information has been reported on the ESD protection circuits in the last few years.

Failure Mode Distribution and the Impact of Technology Trends

Up to date data on the statistics of IC failures due to the various mechanisms are nearly nonexistent in the literature. This is understandable as it requires time and considerable effort to gather meaningful field failure statistics by the users and the manufactures do not publish what they may know about failure mode distribution.

W.B. Wright [1] reported Digital Equipment Corporation's experience with TTL small scale and medium scale integration (SSI/MSI) components. His graphs are reproduced in Fig. 1. Package-related failures including wire bond and interconnect account for about 40% of all failures. In the remainder, metalization and oxide (even in these TTL components) failures dominate. In 1976, the primary failure mode of DRAMs was reported to be oxide breakdown [2]. Mielke [3] reported that the main failure mode of floating EPROMs is charge loss or gain due to oxide defects and mobile ion contamination.

Technology scaling into VLSI and ULSI is known to have particularly narrowed the reliability margin of electromigration, oxide breakdown, hot carrier degradation and single event upset [4]. These so called "process reliability" issues have come to the forefront of process and device development and research. For example hot carrier degradation, not

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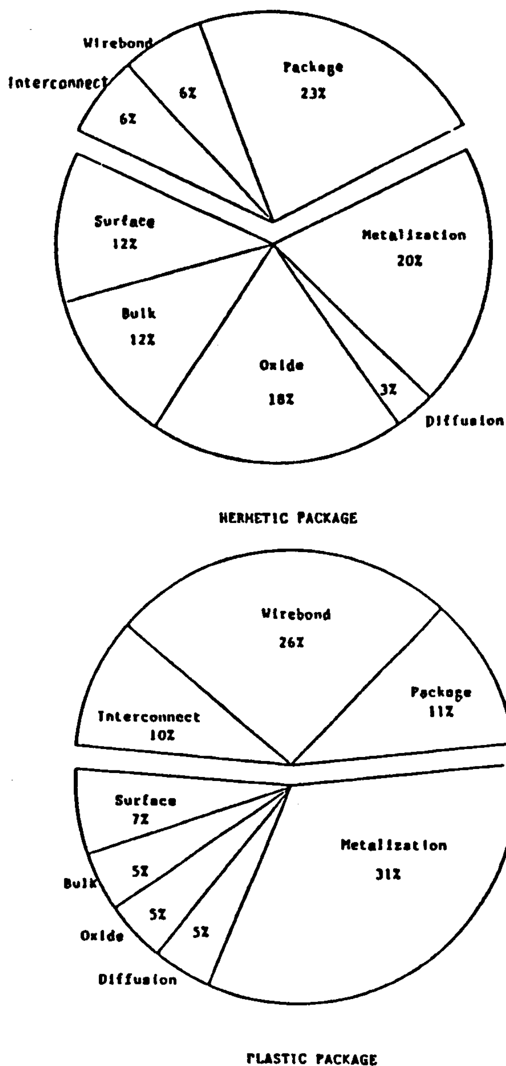

Fig. 1. Failure mode distributions for TTL SSI/MSI components [1].

seen in Fig. 1, is intensely studied now. One may perhaps also expect these process reliability failures to grow in importance relative to package reliability failures.

A list of other technology trends and their impact on reliability would surely, include the increasing complexity of multi-level interconnect technologies and its impact. The interconnect processing steps are often the yield limiting steps now and interconnect and contact failures may be the dominant failure modes. On the other hand, if an all tungsten metal system is developed, metal failures may cease to be an issue. Mobile charge species introduced by the complex processing may become an increasingly serious concern. Lightly doped drain (LDD) structure will continue to be the standard drain structure and keep the hot carrier degradation in check. Testing and processing techniques for thin oxide are improving, but the pace of oxide scaling will also accelerate to gain maximum circuit speed such that oxide reliability will always be at the threshold of acceptability. At the 64Mb level single event upset will require either very aggressive dielectrics, eg. under 50 Å oxide-nitride film, or new dielectrics such as ferroelectrics.

Reliability CAD -- Hot Carrier Induced Circuit Degradation

In designing a complex circuit, designers make a large number of circuit simulations, design changes and optimizations and can predict the circuit's performance and optimizations and can predict the circuit's performance reasonably accurately before committing it to silicon. It would be unthinkable to bypass the circuit simulation and analysis and rely instead on the testing of finished IC's to discover errors or to find out if the performance of the circuit meet specifications. Yet, this is the way IC reliability is treated today.

A logical alternative is to predict circuit reliability at the circuit design stage. To achieve this goal, we must, for each failure mechanism, identify a set of parameters relevant to circuit reliability (these would be the device model parameters in the analogy of circuit performance simulations) and develop simple methods of extracting these parameters for a given process or technology usually involving accelerated DC stress tests on test structures. We must also develop computer programs to predict circuit degradation or failure from these parameters and the current and voltage waveforms. All these steps require understanding of the underlying physical mechanisms of the reliability failures or accurate, general and computationally efficient phenomenological models of the failure mechanisms.

For an example, let's consider CAS (Circuit Aging Simulator) [5], developed at University of California, Berkeley. This is a SPICE-like simulator that can simulate circuit waveforms at arbitrary time in the future considering the hot-carrier degradation of the transistors in the circuit. The key physical model is the realization that transistor parameters are functions of Age, where

$$\mathrm{Age} = \int \frac{I_{ds}}{WH} \left[\frac{I_{sub}}{I_{ds}}\right]^{m} dt \qquad (1)$$

where W is the transistor width; W and m are functions of the oxide field, i.e., functions of V_{gd}, and are determined from dc transistor stress tests [6].

CAS first simulates $V_{ds}(t)$ and $V_{gs}(t)$ of each transistor in the circuit, and from which calculates the Age of each transistor according to (1) at the specified future time. From the Age, MOSFET model parameters at this future time are found by interpolating a set of measured model parameters at

several (dc stress) Age. Finally, the future circuit waveforms are simulated.

Figure 2 shows a comparison between the measured and

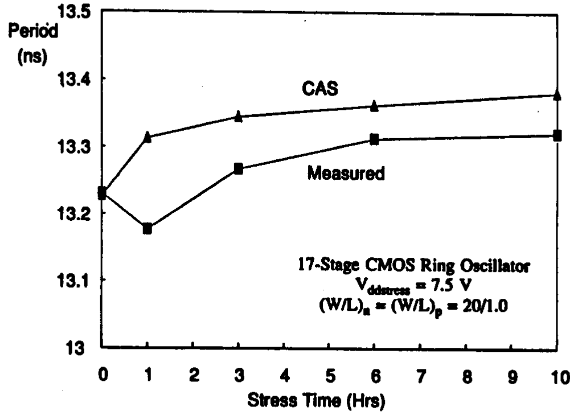

Fig. 2. CAS is developed to simulate the speed and waveforms of a circuit after any specified hot carrier stress time at any voltage.

simulated period of a 17 state 1 μm CMOS ring oscillator at approximately 75 MHz. The simulator did not consider the increase in P-MOSFET current due to hot carrier stressing, thus overestimated the increase in oscillator period.

Hot Carrier Induced BJT Degradation

Under emitter-base reverse bias, a small reverse current, I_R, flows through the junction due to band-to-band tunneling and impact ionization. These carriers apparently generate interface traps near the junction and introduce a component of non-ideal base forward current, ΔI_B, which causes the current gain to decrease. It can be shown that [7]

$$\Delta I_B = D J_c^a \left[\int I_R^b \, dt \right]^c \tag{2}$$

Figure 3 shows an example of gain degradation and the model prediction. This mechanism is not important in ECL circuits, where the base-emitter junctions do not experience reverse bias stress. It is a potential reliability factor in BICMOS circuits [8]. Figure 4 shows the simulated increase in the low-to-high propagation delay of a BICMOS inverter at 300K and 110K. Simulations were carried out in a manner similar to CAS.

Projecting AC Stress Lifetime From DC Stress Data-Electromigration

CAS calculates the Age of a transistor by assuming that the damage to the transistor over a short incremental time is equal to the damage of a very short dc stress; and AC stress damage is simply the sum of the damages of many incremental time periods. This quasi-static model has been found to

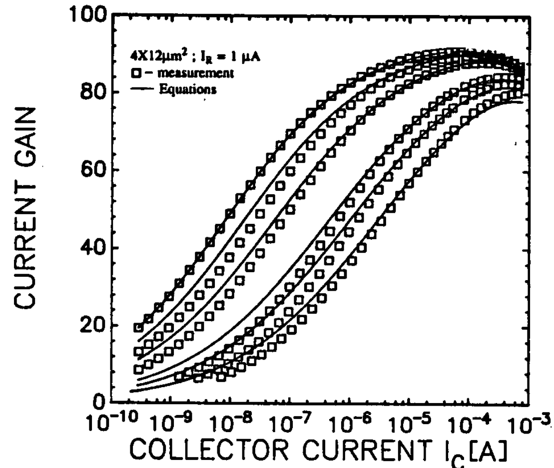

Fig. 3. Measured and predicted BJT current gains. The top curve is the gain of a fresh device. Other curves are the gains after base-emitter junction reverse stress at 1 μA or 4.8V for increasing periods of time [7].

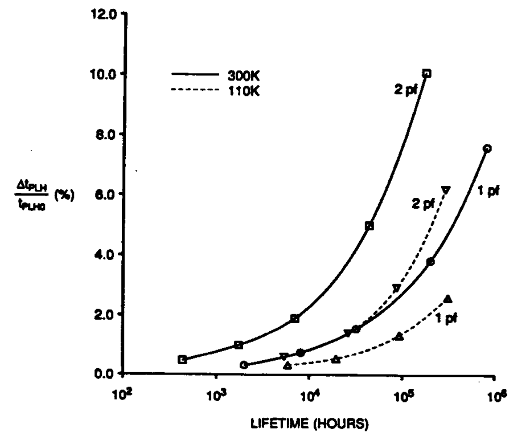

Fig.4. Simulated low-to-high propagation delay of a BICMOS inverter due to hot-carrier induced BJT degradation.

agree with data within experimental error [6], but does not have universal support [9]. Quasistatic model also seems applicable to oxide breakdown when a conservative AC stress lifetime is desired [10,11].

Electromigration, on the other hand, is an example where the quasi-static model is not followed. The time-to-failure of a conductor under constant current stressing is commonly expressed by the Black's equation as:

$$TTf_{dc} = A(T)J^{-2} \tag{3}$$

A has a statistical distribution to be determined by testing; J is the current density.

We have recently developed a vacancy relaxation model for the electromigration lifetime under arbitrary current waveform [10,11]

$$TTF = A(T) \Big/ \overline{J} \cdot \overline{|J|} \qquad (4)$$

where $\overline{J}$ stands for the average value of J. A special case of Eq. (4) for unidirectional rectangular current waveforms is that TTF $\propto \overline{J}^{-2}$ or TTF $\propto$ 1/(duty factor)^2. (The quasistatic model predicts TTF $\propto$ 1/duty factor.) This is in good agreement with data as shown in Fig. 5. Equation (4) also

$MTF_{PULSE\ DC}/MTF_{DC}$ vs Duty Factor

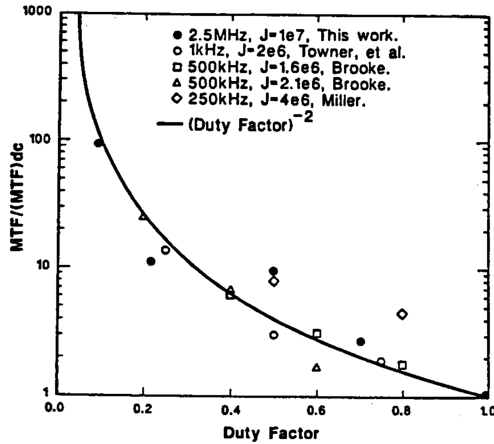

Fig. 5. Pulse DC electromigration lifetime is inversely proportional to the second power of duty factor or average current rather than the rms current [12].

explains the very long lifetimes when currents of both polarities alterately flow in the conductor [13,14,15]. According to Eq. (4), TTF becomes infinity when pure AC (|J|=0) current flows in the conductor. A more accurate model and data [10] show that the pure AC lifetime is about 10,000 times longer than DC lifetime as shown in Fig. 6 [12].

These recent results on pulse DC and AC electromigration will probably considerably loosen today's design rule constraints based on TTF $\propto 1/J^2_{rms}$. Also, the simplicity of Eq. (4) is quite suitable for a reliability CAD tool.

Defect Dominated Reliability Failures -- Oxide Breakdown

By defect dominated failures, I refer to failures with a very wide (many orders of magnitude) spread of lifetimes, oxide breakdown being the best example. Defect dominated failure modes highlight three issues that are important for all failure modes: statistical distribution, highly accelerated test, and screen/burn-in.

Highly Accelerated Test: In order to take a large amount of statistical data, one needs to perform highly accelerated

AC and DC Time-to-failure Distribution

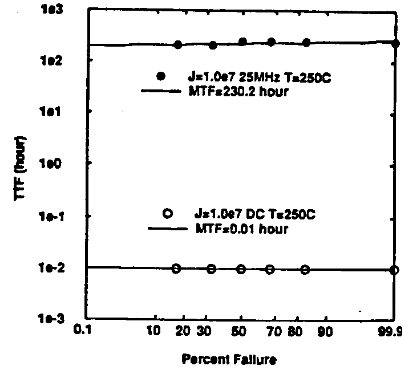

Fig. 6. Pure AC (no DC current) stress electromigration lifetime is about 10,000 longer than DC stress lifetime [12].

tests. To translate (extrapolate) the test data taken in seconds on the wafer level to tens of years of projected lifetime, one should ideally be guided by a plausible theory of the mechanisms involved. A hole induced oxide breakdown theory [16], for example, related the oxide lifetime at voltage V_{ox} (tens of years) to the voltage ramp breakdown voltage, V_{BD}, obtainable in seconds:

$$t_{BD} = 1\times10^{-11} \left[4\times10^{8} \frac{V_{BD}^2}{R} \right]^{V_{BD}/V_{ox}} \qquad (5)$$

Temperature dependencies [16] are not shown in Eq. (5) for simplicity. R is the voltage ramp rate. Figure 7 shows that

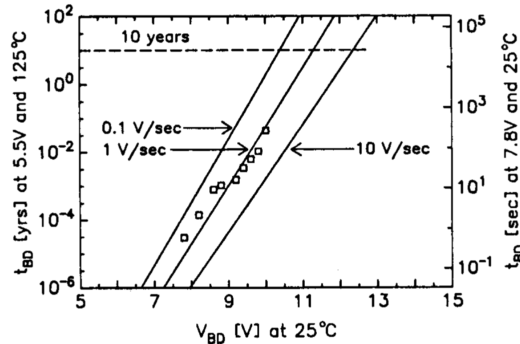

Fig. 7. Simple correlation between 5.5V/150°C oxide lifetime and 25°C ramp test breakdown voltage. Oxides failing ramp test below about 12V would have less than 10 years of lifetime at 5.5V.

V_{BD} = 12.5 at 25°C is equivalent to t_{BD} = 10 years at 5.5V and 125°C.

Defect Statistics: There does not appear to be a preponerance of data justifying the use of lognormal, Weibull, or

any other statistical distribution to replace the task of sufficient data except as a last resort. The total area of the oxide test structures, for example should be at least several hundred times the oxide area in a product, if one wishes to have accurate information about the first 1% of the product failures. This argues for the use of large reliability test vehicles.

On the other hand, once the actual early failure test data is available, one can use either lognormal, Weibull, or other fitting functions to fit the relevant portion of the data (first a few percent) for further mathematical manipulation.

For example, a normal distribution of V_{BD} in Eq. (5) would yield approximately a lognormal distribution of t_{BD}. However, if the measured V_{BD} distribution fits some other function better [16], there is no reason and no need to force a normal distribution on it.

Screen/Burn-In: From the measured distribution of V_{BD}, one can easily estimate the cumulative oxide failures in 10 years (some as the percentage failing ramp breakdown test under V=12.5V). One can actually predict the cumulative failure as a function of the burn-in or screen time, voltage, and temperature. Oxides 155Å and 200Å thick and having relatively high defect densities measured as examples in Fig. 8 [17]. As the burn-in time increases, the 10 year cumulative

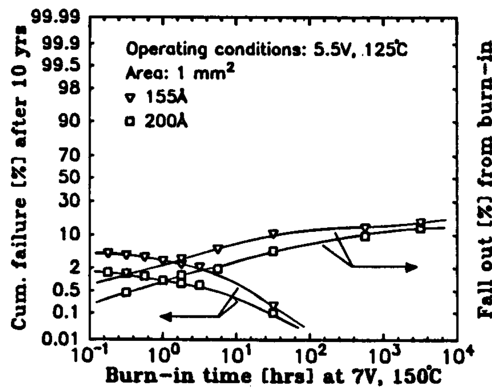

Fig. 8. Analysis of oxide ramp breakdown statistics and yield predictions of failure rate and burn-in fall-out as functions of burn-in time (and of burn-in voltage and temperature) [17].

failure decreases while the burn-in fall-out increases. One can thus intelligently optimize the burn-in time, temperature and voltage.

Summary

Technology scaling continues to push reliability issues such as electromigration, hot carrier degradation, and oxide breakdown to the forefront of technology development and tradeoff. Reliability CAD tools that can predict the chip reliability at the design stage will be invaluable. Simulation of circuit speed degradations of CMOS and BICMOS inverter circuits have been demonstrated. Electromigration lifetime under arbitrary waveforms can be calculated from the measured DC lifetime. Pulse DC and AC lifetimes are longer than previously thought. Oxide breakdown highlights the need for accurate accelerated test model, proper use of statistics, and the potential of predicting the optimal burn-in condition and effects.

Acknowledgement

This research is sponsored by SRC, ISDO/STIO administered through ONR under Contract N0019-85-K-0603 and Sandia Laboratory under California MICRO program.

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