Electromigration Characteristics of Tungsten Plug Vias Under Pulse and Bidirectional Current Stressing

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Abstract—**Using Kelvin test structures, electromigration performances of selective CVD tungsten filled vias under dc, pulsed dc, and ac current signals have been studied. The metallization consists of Al-Cu/TiW multilevel metals. The via electromigration lifetime exhibits a current polarity dependence. The via ac lifetimes are found to be much longer (more than 1000 ×) than dc lifetimes under the same peak stressing current density. The via lifetimes under pulsed dc stress of 50% duty factor are twice the dc lifetimes at low-frequency regions (< 200 Hz) and 4-5 times the dc lifetimes at high-frequency regions (> 10 kHz). The results are in agreement with the vacancy relaxation model.**

I. Introduction

As THE IC technology advances toward ULSI levels, the improved multilevel metallization technologies with increasing number of metal levels have been developed. Blanket and selective CVD W have been used in contact and via filling to improve planarity and electromigration. DC electromigration reliability of tungsten-plug vias have been reported [1]-[3]. These electromigration studies were done under constant current conditions even though integrated circuits operate under time-varying and bidirectional current conditions. Experiments have shown that high-frequency varying currents cause different electromigration characteristics with respect to those induced by continuous currents in metal interconnects [4]. In this work we address the electromigration behaviors under the time-varying electrical current of an advanced multilevel metallization system containing selective CVD tungsten plug.

II. Experiment

Kelvin test structures consisting of two patterned metal levels connected by $0.7 \times 0.7\text{-}\mu m^2$ selective CVD-W filled vias were used to investigate electromigration characteristics of vias. Metal 1 (M1) consists of TiW(1500 Å, bottom layer)/Al-Cu(4 wt%)(5000 Å)/TiW(700 Å, top layer) and metal 2(M2) consists of Al-Cu(4 wt%)(5000 Å)/TiW(700 Å, top layer). The two metal layers were separated by 7000 Å of SiO_2 and all samples were passivated with 5000-Å TEOS, as shown in the insert of Fig. 1. Both TiW and Al-Cu layers were deposited using sputtering methods. Metal lines and vias were defined by using standard photolithographic and dry etching techniques. During the via hole etching, the top TiW layer of M1 is mostly etched away from the bottom of the via hole with perhaps only 100 Å of TiW left.

A current source regulated by a transistor and driven by the output of a TTL gate was used to generate pulsed dc and ac currents [5]. Electromigration testing was performed on wafers placed directly on the heated stage of a probe station. All electromigration testing were carried out at an ambient temperature of 250°C. Via resistance was monitored periodically during testing. Device failure was defined to be when the circuit was completely open.

III. Results and Discussion

Aluminum atoms electromigration is in the direction of the electron flow; therefore, it is better to think about the electron flow direction than the current direction. The effects of electron flow direction passing though the via on the median time to failure (MTTF) under dc currents are shown in Fig. 1. In the case of electron flow from M2 to M1, some samples failed in the interconnect rather than at the via. Therefore, the lifetime in that case should be considered to be the low limit of the via lifetime. It is obvious that the via lifetime is shorter for electron flow from M1 to M2 than the reverse. For this direction of electron flow, we believe, aluminum is pushed away from the top surface of the W plug leading to the open failure. For the other direction of electron flow (M2 to M1), the top TiW layer of M1, which is more electromigration resistant than aluminum, served as a more robust current spreader, i.e., open failure will not occur even when Al is pushed away from the plug area. This observation is consistent with [1]. The scanning electron microscopy(SEM) micrographs shown in Fig. 2 illustrate the sequence of electromigration-induced failure process when electron flow was from M1 to M2. Aluminum voiding in M2 at the via area and the accumulation of aluminum nearby in the downstream direction of electron flow can be seen in Fig. 2(b) at the early stage of stressing test. After an open circuit is detected, the M2 layer at the via area was found to have disappeared as

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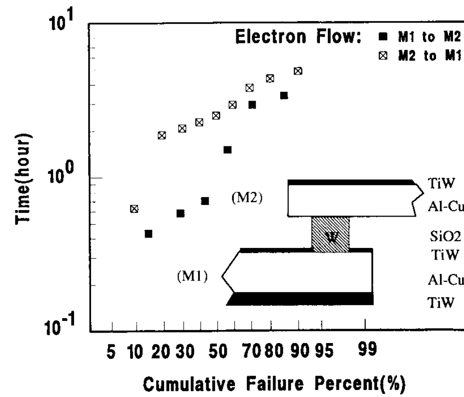
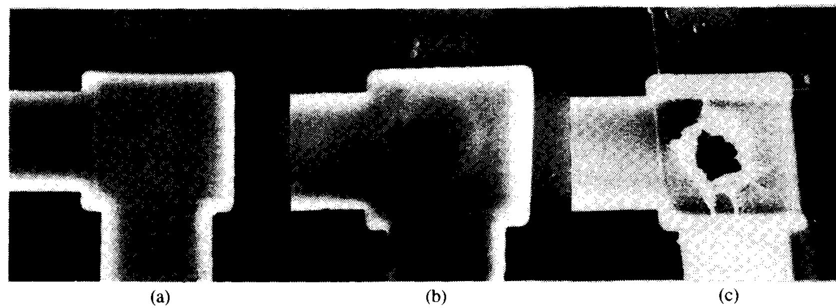


Fig. 1. Log-normal plot of cumulative failure rate for electron flow from M1 to M2 and M2 to M1 under $J_{DC} = 3.5 \times 10^7$ A/cm^2, $T = 250°$C. The layer structure of electromigration test samples is shown in the insertion.



(a) (b) (c)

Fig. 2. SEM micrographes (3K ×) of (a) fresh test sample, (b) during the early stage of stressing test, and (c) a totally open failed via for electron flow from M1 to M2 under $J_{DC} = 3.5 \times 10^7$ A/cm^2, $T = 250°$C.

shown in Fig. 2(c). Severe Joule heating toward the end of the electromigration test after Al has been pushed away from most of the plug top is believed to be responsible for the disappearance. Using SEM after failure, the morphologies of M1 layer were inspected after striping the M2 layer. No obvious damages were observed in M1 independent of the stressing current polarity. The lack of electromigration-induced damage in M1 can be attributed to the additional top TiW layer in M1, and the encapsulation of M1 with a thicker SiO_2 layer.

According to the vacancy recombination model proposed by Liew *et al.* [6], when the stressing current frequency f is much smaller than $1/\tau$ (τ is the vacancy recombination time), the lifetime under pulse-dc stressing conditions can be written as

$$\frac{\text{MTTF}_{\text{pulse-DC}}}{\text{MTTF}_{\text{DC}}} = \frac{1}{D} \tag{1}$$

where D is the duty factor. When the frequency f is much higher than $1/\tau$,

$$\frac{\text{MTTF}_{\text{pulse-DC}}}{\text{MTTF}_{\text{DC}}} = \frac{1}{D^2}. \tag{2}$$

Repetition frequency dependence on $\text{MTTF}_{\text{pulse-DC}}/\text{MTTF}_{\text{DC}}$ at a peak current density 4.5×10^7 A/cm^2 and a duty factor of 50% is shown in Fig. 3. The via temperature has been calibrated by measured via resistance, which has been used to normalize the MTTF to 250°C using a measured activation energy of 0.57 eV for our Al–Cu(4 wt%) interconnection lines. We found that at a low-frequency region (< 200 Hz), the $\text{MTTF}_{\text{pulse-DC}}$-to-$\text{MTTF}_{\text{DC}}$ ratio is about 2, while at a high-frequency region (> 10 kHz), the ratio is about 4 to 5. It is in good agreement with the vacancy recombination model shown above, and the vacancy recombination time constant τ in our Al–Cu sample is found to be about 0.1 ms (at 250°C), shorter than Al–Si's [4], [5].

For bidirectional (ac) electromigration tests with a peak current density of 4.5×10^7 A/cm^2 and a duty factor of 50%, no failure was detected or observed after stressing for 350 h. This means that the ac lifetime is much longer (more than 1000 ×) than the dc lifetime, as shown in Fig. 4. The inset shows the 1-MHz ac waveform used in the test. This is similar to the results reported for aluminum interconnects [4]–[6]. The longer MTTF can be attributed to the healing effect of the two vacancy fluxes in opposite directions. It appears that the damage incurred during the first half-cycle is mostly "repaired" during the second half-cycle.

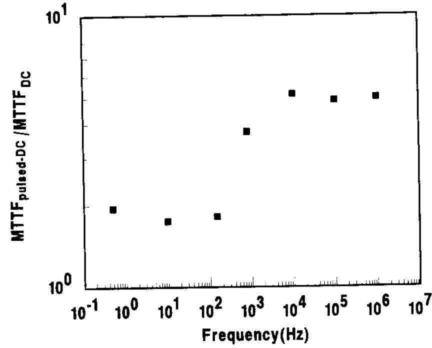


Fig. 3. Plot of normalized pulsed dc lifetime $MTTF_{pulse\text{-}DC}/MTTF_{DC}$ as a function of current repetition frequency. The test structure was stressed at $J = 4.5 \times 10^7$ A/cm^2 and $T = 250$°C, and electron flow was from M1 to M2.

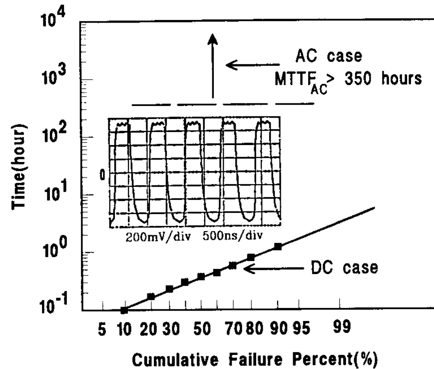


Fig. 4. Log-normal plot of cumulative failure rate for ac and dc cases stressed at $J = 4.5 \times 10^7$ A/cm^2, $T = 250$°C. The insert shows the ac waveform used in the ac electromigration stressing.

IV. Conclusion

Via electromigration lifetime is limited by the migration of Al away from the W plug along the direction of electron flow. In this study, the via electromigration wearout is always observed at the via area in the M2 layer independent of stressing current polarity. No electromigration-induced damage was found in M1 layer. We also find that the ac lifetimes of the via structure are much longer (more than 1000 ×) than the dc lifetimes. Finally, for pulsed dc electromigration stressing, we find that the ratio of $MTTF_{pulse\text{-}DC}/MTTF_{DC}$ at a high-frequency region (> 10 kHz) is about 4–5, and at a low-frequency region (< 200 Hz) it is about 2. The failure lifetime as a function of pulse frequency agrees well with the behavior predicted by the vacancy relaxation model.

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