

Simulation of CMOS Circuit Degradation due To Hot-Carrier Effects

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ABSTRACT

Comparing long term ring-oscillator hot-carrier degradation data and simulation results we show that a public-domain circuit simulator BERT can predict CMOS digital circuit speed degradation from transistor DC stress data. Initial fast degradation is noted and attributed to the "zero crossing" effect caused by PMOSFET current enhancement. Relationship between circuit lifetime and transistor DC stress is examined and a first order circuit lifetime model is developed.

I. INTRODUCTION

Static (DC) hot-carrier degradation has been extensively studied and well understood [1]; however much controversy still exists regarding dynamic (AC) degradation. Although different mechanisms for enhanced dynamic degradation have been proposed [5-6], recent studies on the dynamic degradation of MOSFETs in actual circuit environment [7] have concluded that despite the presence of different mechanisms, the quasi-static method is still valid for digital circuits. Inductive noise [8] and errors in substrate and gate currents can contribute more variation to the degradation than the proposed enhanced AC degradation mechanisms.

A clear understanding of hot-carrier effects in an actual circuit environment is essential to ensure product reliability and to evaluate hot-carrier reliability concerns in the early stages of process optimization. Hot-carrier reliability simulation programs, which can predict circuit reliability under operating conditions, can form an integral part of this process. The key issue

is whether model parameters based on DC stressing and substrate and gate current measurements can be used to simulate actual circuit degradation. This paper presents correlation between experimental long-term ring oscillator degradation results and BERT simulation based on hot-carrier quasi-static model. Next the impact of PMOSFET degradation on ring oscillator frequency degradation is evaluated. We then examine the relationship between circuit lifetime and transistor DC stress and present simple rules of thumb to predict circuit degradation from DC stressing data.

II. BERT -- An Overview

BERT (Berkeley Reliability Tools) is a public domain simulator for hot-carrier as well as oxide and electromigration reliability simulation distributed by University of California, Berkeley [9-10]. It includes both NMOSFET and PMOSFET hot-carrier models [11]. The amount of degradation, ΔD , suffered by a MOS device due to hot-carrier stressing of duration, t , is given by [1],

$$\Delta D = f(t) \quad (1)$$

The NMOSFET device lifetime, τ can be expressed as,

$$\tau \left[\frac{I_{DS}}{W} \right] = Hf^{-1}(\Delta D) \left[\frac{I_{Sub}}{I_{DS}} \right]^{-m} \quad (2)$$

and the PMOSFET device lifetime τ is given by,

$$\tau = Hf^{-1}(\Delta D) \left[\frac{I_g}{W} \right]^{-m} \quad (3)$$

where H and m are the gate-bias dependent degradation parameters and I_{Sub} , I_g , and I_{DS} are the substrate, gate, and drain currents respectively. A parameter "Age" (amount of stress experienced by each device) based on the model by Hu et al. [1] is used to quantify device degradation during circuit operation. For NMOSFET Age is defined as [10]:

$$Age = \int \frac{I_{DS}}{WH} \left[\frac{I_{Sub}}{I_{DS}} \right]^m dt \quad (4)$$

and for PMOSFET it is given by [10,12],

$$Age = \int \frac{1}{H} \left[\frac{I_g}{W} \right]^m dt \quad (5)$$

where W is the device width and t is the circuit operating time. By using weighting factors W_g and W_b PMOSFET Age has been further refined to include the effects of both substrate and gate currents [11]. Thus the total PMOSFET Age then takes the following form,

$$Age = W_g \times \int \frac{1}{H} \left[\frac{I_g}{W} \right]^m dt + W_b \times \int \frac{I_{DS}}{WH} \left[\frac{I_{Sub}}{I_{DS}} \right]^m dt \quad (6)$$

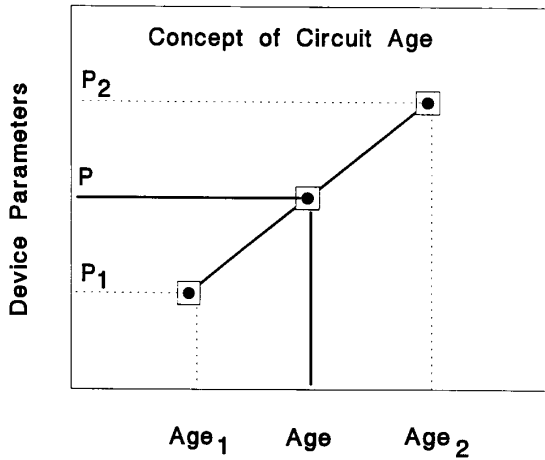


Fig. 1. Method of determining aged parameters during circuit operation. Age1, Age2 are prestressed model parameters and Age represents the circuit device age.

During circuit simulation, the Age is calculated for each device and at each timestep and then integrated to obtain the total Age of the SPICE

analysis. After the Age of each transistor in the circuit is calculated by this quasi-static method, the aged process files corresponding to the individual transistors is then used to simulate the actual circuit degradation for a specified period of time. Fig. 1 graphically explains the process of calculating aged device parameters. Age1, Age2, etc. are ages of device parameters based on prestressed DC data. Circuit device age is then calculated by user specified interpolation or regression analysis. If the age of the circuit device falls outside the prestressed age data, then extrapolation using the two closest parameter sets is used.

Fig. 2 is a plot of $\Delta I_{DS}/I_{DS}$ versus time on a log-log scale. Fig. 3 shows a plot of τ_{DS}/W versus I_{Sub}/I_{DS} for NMOSFET and fig.4 shows a plot of τ vs I_g/W for PMOSFET. The slope and intercept of these plots give the m and H degradation parameters. In [13], it has been shown that H and m are, in general, gate-bias (V_{gd}) dependent. Thus, by including the bias-dependence of H and m , BERT can accommodate all known quasi-static models such as recently proposed low and high gate voltage hot-carrier models [14]. [14] assigns specific physical mechanisms to the low V_g , medium V_g , and high V_g regions. There are still disagreements on these assignments [15]. Because BERT does not assume any physical degradation model, these disagreements do not affect BERT's validity.

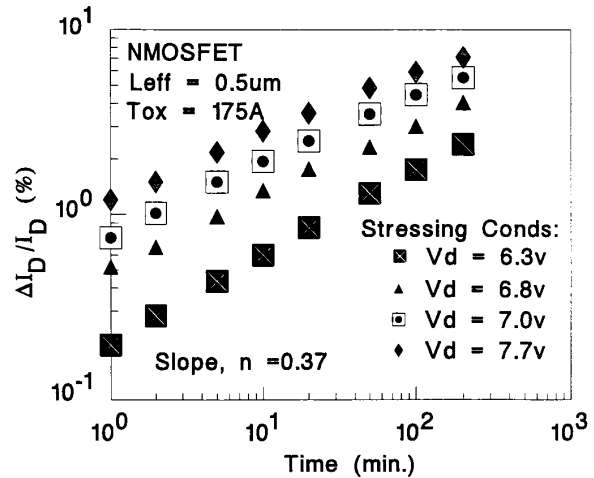


Fig. 2. NMOSFET Linear drain current percentage change versus time. All devices stressed under peak substrate current condition.

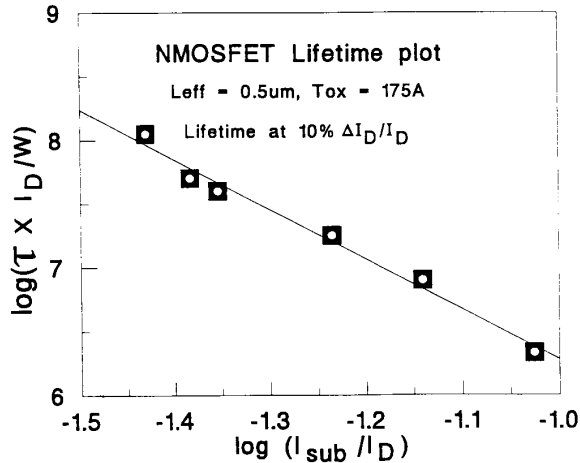


Fig. 3 NMOSFET lifetime plot. Degradation parameters m and H are obtained from slope and intercept respectively.

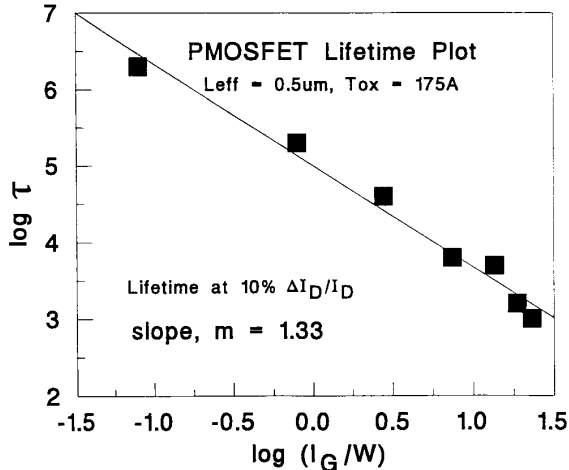


Fig. 4. PMOSFET lifetime plot. Degradation parameters m and H are obtained from slope and intercept respectively.

III. EXPERIMENTAL AND SIMULATION RESULTS

A $0.7\mu\text{m}$ LDD CMOS technology with 175\AA gate oxide was used to fabricate the ring-oscillators and the discrete devices. Devices with $L_{\text{eff}} = 0.5\mu\text{m}$ and a 91-stage ring oscillator with a fanout of 1 has been used in this study. The most important DC stresses were those done under peak substrate condition for NMOSFET and peak gate current condition

for PMOSFET. $V_{\text{DS}} = 8\text{v}$ was used for all stresses and $V_{\text{DS}} = 5\text{v}$ was used for all measurements. D.C. parameter degradation were monitored at $V_{\text{GS}} = 5\text{V}$ and $V_{\text{DS}} = 0.1\text{v}$.

SPICE model parameters for substrate and gate currents were first extracted for N- and P-MOSFETS. Then degradation parameters H and m were determined using the method outlined in the previous section. Constant H and m were used for this study for simplicity. Fig. 5 shows the experimental and simulated linear drain current degradation of N- and P-MOSFETS and the long term experimental and BERT-simulated ring oscillator frequency degradation. This is the first verification of long term circuit degradation using a hot-carrier simulator. The figure also shows excellent correlation between simulation and experimental results which confirms the theory that circuit degradation can be predicted using the quasi-static method.

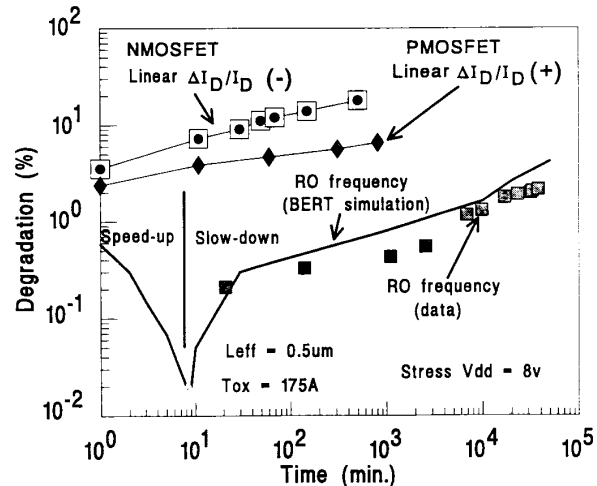


Fig. 5. Experimental and BERT-simulated frequency degradation versus time for a 91-stage ring oscillator. Correlation with DC stress data is also shown. Initial speed-up is clearly shown.

IV. ZERO CROSSING EFFECT

Fig. 5 shows an initial speed-up (frequency enhancement) of the ring oscillator and a very steep rise of the slow-down (frequency degradation) portion of the of the $\Delta f/f$ curve. Both of these phenomena are due to the drain current

increase of PMOSFET due to hot-carrier effect. Fig. 6 shows the frequency degradation curves due to NMOSFET degradation only (negative $\Delta f/f$), due to PMOSFET degradation only (positive $\Delta f/f$) and due to combined PMOSFET and NMOSFET degradation. We notice that the combined frequency degradation

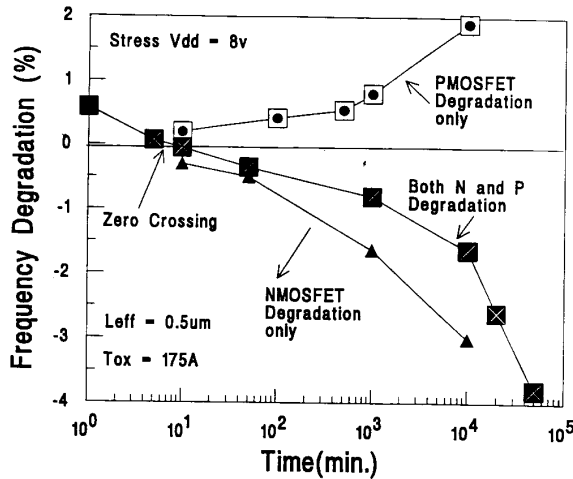


Fig. 6. BERT-simulation showing the effect of NMOSFET, PMOSFET and the combined N- and P-MOSFET hot carrier degradation on the ring oscillator frequency degradation. "Zero crossing" effect is apparent.

curve has an enhancement portion and a degradation portion. This can be explained in the following way. If the PMOSFET shows a large initial drain current enhancement, then initially the PMOSFET enhancement dominates and the frequency will show an enhancement (positive $\Delta f/f$). However, since the PMOSFET degradation saturates much earlier than the NMOSFET, the NMOSFET degradation catches up with the PMOSFET enhancement resulting in a reduction of the frequency enhancement. Ultimately the NMOSFET degradation dominates which then causes the frequency to degrade (negative $\Delta f/f$). The hot-carrier induced frequency change will then move from enhancement (positive $\Delta f/f$) to degradation (negative $\Delta f/f$) thus crossing the "zero" $\Delta f/f$ point. This "zero crossing" on a log-log plot shows up as a steep slope around the zero as shown in fig. 5. The impact of the "zero crossing" gets further

enhanced by large PMOSFET enhancement, typically found in oxides with large density of electron traps. Fig. 7 illustrates this fact by

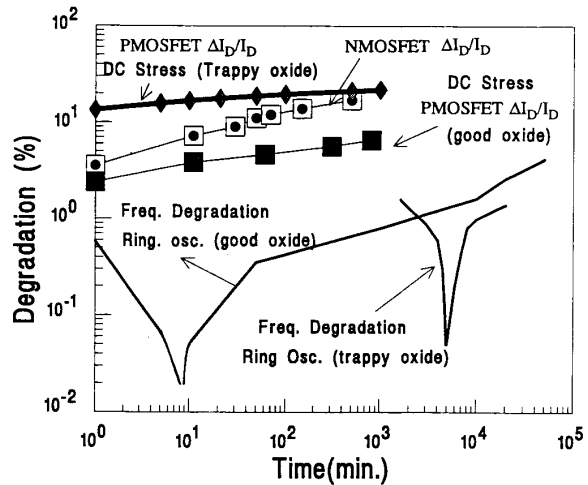


Fig. 7. Impact of PMOSFET degradation on the "zero crossing" effect. Trappy oxide simulation shows much steeper slope due to large PMOSFET degradation.

comparing the simulated frequency degradation behaviour of good versus trappy oxide. It shows the linear change in drain current due to hot-carrier stressing of good and trappy oxides for both PMOSFET and NMOSFET devices. Notice the larger PMOSFET drain current change of the trappy oxide. Fig. 7 also shows that the trappy oxide which has a very large PMOSFET drain current enhancement shows a much larger initial frequency increase and this frequency enhancement portion of the curve stretches for a much longer stressing time since it requires a lot longer for the NMOSFET degradation to catch up with the PMOSFET enhancement. The large initial frequency enhancement also causes a much steeper initial rise of the slow-down portion of the curve as shown in fig. 7.

V. RULE OF THUMB

In the previous sections, it was demonstrated how BERT can be used to simulate the hot-carrier degradation of VLSI circuits. In this

section we show how circuit lifetime is related to device DC stress lifetime commonly monitored in industrial laboratories today. This understanding is becoming increasingly important for deep submicron technologies, since criterion such as 10% drain current change at 10 years can no longer be easily achieved. Lee et al. [16] first introduced simple rules of thumb to translate discrete device degradation to actual circuit performance degradation of inverter based CMOS VLSI circuits. In this paper we extend that to include the effects of PMOSFET drain current increase on the overall performance of VLSI circuits.

The rule thumb presented here 1) translates device-level linear drain current change to circuit speed change, and 2) translates DC lifetime to AC lifetime. Fig. 8 shows the simulation results of linear $\Delta I_D/I_D$ of a DC stressed NMOS device, linear $\Delta I_D/I_D$ of a NMOSFET device internal to the ring oscillator and subjected to the ring oscillator stress, and the $\Delta f/f$ of the ring oscillator with PMOSFET degradation turned off. The two rules of thumb can be

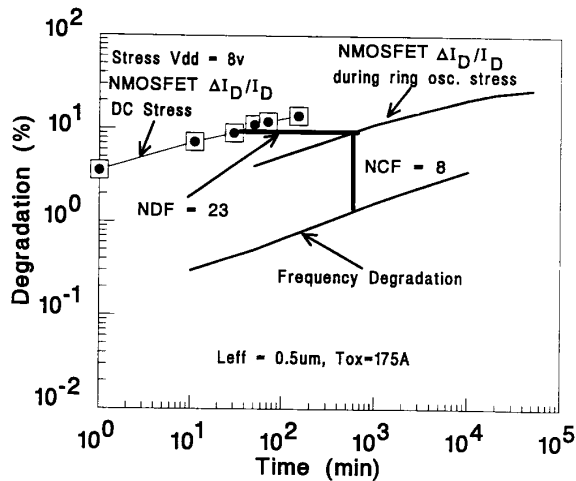


Fig. 8. BERT-simulation showing NMOSFET contribution to lifetime guideline. Ring oscillator degradation simulation is due to only NMOSFET degradation. Also shown is the internal ring oscillator NMOSFET linear $\Delta I_D/I_D$ during AC stress.

understood from fig. 8. The horizontal shift, called the NMOSFET duty factor (NDF), represents the time required for the internal ring oscillator NMOSFET device to reach an

equivalent DC linear $\Delta I_D/I_D$ and the vertical shift, called the NMOSFET speed factor (NSF), represents the factor required to translate a given linear $\Delta I_D/I_D$ to circuit speed degradation. Fig. 9 is same as fig. 8, except it is for PMOSFET with PDF and PSF representing the PMOSFET duty and speed factors respectively. From figs. 8-9, we obtain NDF = 23, PDF = 330, NSF = 8 and PSF = 3. In general NSF and PSF are independent of technologies; however NDF and PDF, the NMOSFET and PMOSFET duty factors will be a

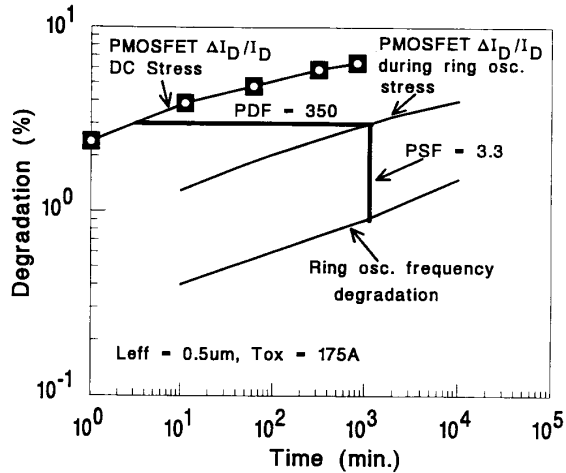


Fig. 9. BERT-simulation showing PMOSFET contribution to lifetime guideline. Ring oscillator degradation simulation is due to only PMOSFET degradation. Also shown is the internal ring oscillator PMOSFET linear $\Delta I_D/I_D$ during AC stress.

function of technology, circuit loading conditions and operating frequency. Fig. 10 shows the percent change in frequency when both NMOSFET and PMOSFET drain current change is taken into account. Compared with fig. 8 (NMOSFET only case), the speed factor has increased to 13 and at the same frequency degradation level, the circuit lifetime has increased by a factor of 3. Both of these are due to PMOSFET drain current enhancement. We believe other CMOS circuits could exhibit even greater sensitivity to PMOSFET drift. Thus to accurately predict circuit lifetime, PMOSFET effect has to be included in the simple rules of thumb.

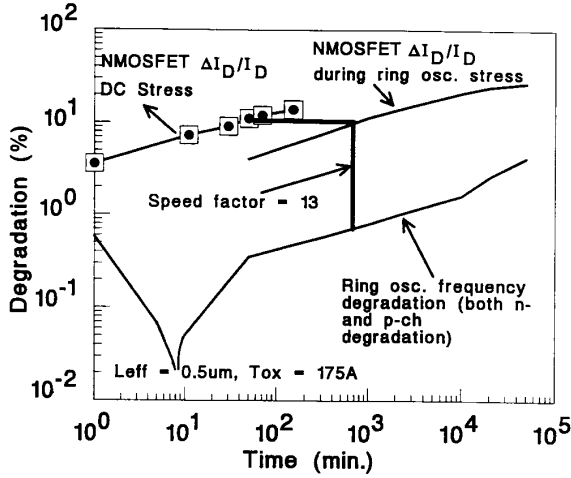


Fig. 10. Combined effect of NMOSFET and PMOSFET on circuit lifetime. PMOSFET drift causes both the speed and lifetime factors to increase.

Speed Rule

Consider an inverter with output load capacitance C . The time to charge or discharge C is given by

$$t = \frac{C\Delta V}{I} \quad (7)$$

where I is the charging/discharging current and t is the time required to change the output by voltage, ΔV . The total propagation delay, t_p , of an inverter is then given by,

$$t_p = \frac{C\Delta V}{I_n} + \frac{C\Delta V}{I_p} \quad (8)$$

Here I_n and I_p are the discharging and charging drain current respectively. The change in the propagation delay due to hot carrier effects can then be expressed as

$$\Delta t_p = \frac{C\Delta V\Delta I_n}{I_n^2} + \frac{C\Delta V\Delta I_p}{I_p^2} \quad (9)$$

and,

$$\frac{\Delta t_p}{t_p} = \frac{\Delta I_n}{I_n^2(1/I_n + 1/I_p)} + \frac{\Delta I_p}{I_p^2(1/I_n + 1/I_p)} \quad (10)$$

Assuming equal rise and fall time, so that $I_n = I_p$, we get,

$$\frac{\Delta t_p}{t_p} = \frac{1}{2} \left[\frac{\Delta I_n}{I_n} \right] + \frac{1}{2} \left[\frac{\Delta I_p}{I_p} \right] \quad (11)$$

I_n and I_p are some average of the linear and saturation currents. Representing the PMOSFET linear drain current by ΔI_{Dp} and NMOSFET linear drain current by ΔI_{Dn} , respectively, we obtain,

$$\frac{\Delta t_p}{t_p} = \alpha \frac{\Delta I_{Dn}}{I_{Dn}} + \beta \frac{\Delta I_{Dp}}{I_{Dp}} \quad (12)$$

Here $\Delta I_{Dn}/I_{Dn}$ and $\Delta I_{Dp}/I_{Dp}$ are the linear percentage drain current change of NMOSFET and PMOSFET respectively. α and β are the factors relating linear drain current change and the circuit speed. In [16] and fig. 8, it was shown that for NMOSFET the factor α is 8 and our PMOSFET study shows that the factor β should be 4, although for the specific case in fig. 9 β was found to 3.3. Thus the percentage change in the inverter propagation delay can be represented by

$$\frac{\Delta t_p}{t_p} = \frac{1}{8} \frac{\Delta I_{Dn}}{I_{Dn}} + \frac{1}{4} \frac{\Delta I_{Dp}}{I_{Dp}} \quad (13)$$

Duty Factor Rule

Fig. 11 shows the gate (V_G) and drain (V_D) voltage waveforms of an inverter subjected to the ring oscillator stress. The duty factor is defined as,

$$DF = \frac{\text{A.C. Age per Cycle}}{\text{D.C. Age per Cycle}} \quad (14)$$

where Age has been defined earlier in equs.(4-5). Equ. (14) should be used whenever feasible but for the purpose of approximate and quick estimation of duty factor from voltage waveforms, we propose the following first order duty factor approximation:

$$DF = \frac{\text{Effective A.C. stress time}}{\text{Cycle time}} \quad (15)$$

$$\text{NDF} = 8 \times [\text{time } (V_{DS} > 0.9V_{DD} \text{ and } V_{GS} > V_{tn} + 0.3)] / \text{Cycle Time} \quad (16)$$

$$\text{PDF} = [\text{time } (V_{SD} > 0.9V_{DD} \text{ and } V_{tp} < V_{GS} < V_{tp} + 1.5v)] / \text{Cycle Time} \quad (17)$$

where NDF and PDF are the NMOSFET and

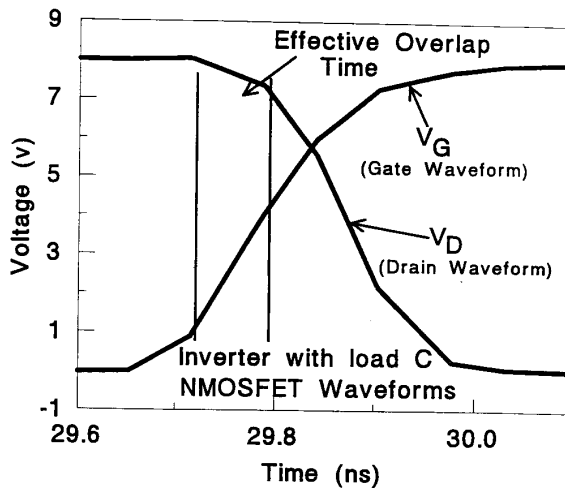


Fig. 11a. Gate and drain voltage waveforms affecting NMOSFET device degradation. Effective overlap time which approximates the duration of the degradation is used in NMOSFET duty factor calculation.

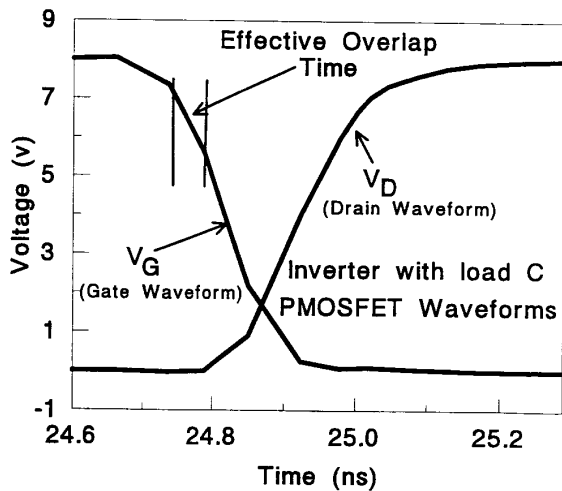


Fig. 11b. Gate and drain voltage waveforms affecting PMOSFET device degradation. Effective overlap time which approximates the duration of the degradation is used in PMOSFET duty factor calculation.

PMOSFET duty factors and $V_{th(p)}$ are the NMOSFET (PMOSFET) threshold voltages. The factor 8 has been included in NDF to account for lower drain current during A.C. stress compared to the D.C. stress drain current. Recall, $Age \propto I_D^{-(m-1)}$. From fig.11a and equ.(16) we obtain $NDF = 28$ and from fig.11b and equ.(17) we obtain $PDF = 350$.

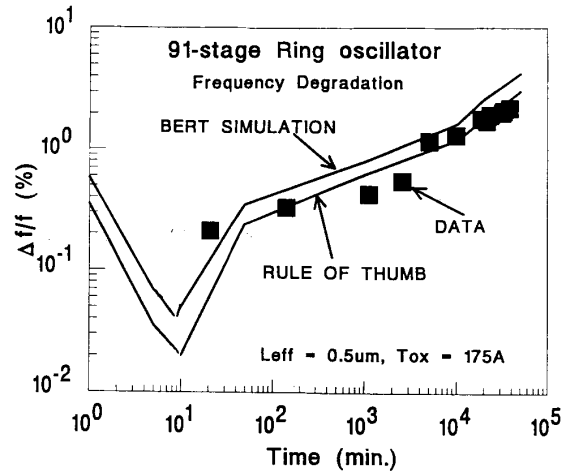


Fig. 12. Experimental, BERT simulated, and rule of thumb calculated frequency change as a function of time.

This agrees quite well with the simulation results (figs. 8-9). Fig. 12 shows the experimental, simulated and rule of thumb calculated $\Delta f/f$ as a function of time. The figure demonstrates that the simple rules of thumb can be used to roughly predict CMOS VLSI circuit hot-carrier induced circuit speed change from simple NMOSFET and PMOSFET D.C. stress data. More exact prediction of course requires circuit simulations such as those performed by BERT.

VI. CONCLUSION

BERT, a public-domain hot-carrier simulator, was successfully used to predict the long term hot-carrier degradation behaviour of ring-oscillators. Thus, this work supports the validity of the quasi-static approach in predicting the hot-carrier degradation of CMOS VLSI circuits. Large initial PMOSFET drain current enhancement can result in initial frequency enhancement followed by an initial fast degradation due to the "zero crossing" effect. Simulation results of good and trappy oxides were compared to show that the initial fast degradation gets further enhanced in trappy oxides. Simple rules of thumb that translate device-level degradation to CMOS circuit lifetime have been presented. The rules of thumb, which consists of two factors, speed and duty, and which includes

both PMOSFET and NMOSFET models, can roughly predict CMOS VLSI circuit degradation. For the test case in this study, the NMOSFET speed and duty factors were 8 and 28 respectively and the PMOSFET speed and duty factors were 4 and 350 respectively.

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REFERENCES:

- [1] C. Hu, et al, IEEE Tran. Elec. Dev., Vol.32, p.375, 1985.
- [2] E. Takeda, et al., IEDM Tech. Dig., P.60, 1985.
- [3] P. Heremans, et al., IEEE Tran. Elec. Dev., Vol. 35, P.2194, 1980
- [4] J. Choi, et al., J. Appl. Phys., Vol.65, P.354, 1989
- [5] K. Mistry et al, IEEE Elec. Dev. Letts., Vol. 11, P.267, June 1990.
- [6] M. Brox et al., IEEE Tran. Elec. Dev., Vol. 38, P.1852, Aug. 1991.
- [7] W. Weber et al, IEEE Trans. Elec. Dev., Vol. 38, P.1859, Aug. 1991.
- [8] E. Takeda et al, IRPS Proceedings, P. 1118, 1991.
- [9] P. Lee et al., IEDM Technical Digest, P.134, 1988.
- [10] UCB Memorandum No. UCB/ERL M91/07, Dec. 1991.
- [11] P. Lee et al, Int. Symp. on VLSI Tech., Systems, and Appl., P.191, 1991.
- [12] Ong. et al., Proc. IEEE Rel. Phys. Symp., P.178, March 1989.
- [13] M. Kuo et al., IEEE Tran. Elec. Dev., Vol. 35, P.1004, 1988.
- [14] K. Mistry et al., IEDM Tech. Dig., P.91, 1991.
- [15] P. Heremans et al., IEEE Tran. Elec. Dev., Vol. 39, P.458, 1992.
- [16] P. Lee et. al., IEEE Elec. Dev. Letts, Vol.11, No.1, P.39, Jan. 1990.