

THE EFFECTS OF OFF-AXIS SUBSTRATE ORIENTATION ON MOSFET CHARACTERISTICS

James Chung, Jian Chen, Mark Levi*, Ping-Keung Ko, and Chenming Hu

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA 94720

* Rome Air Development Center, Griffiss AFB, NY 13441.

ABSTRACT

In this paper, the effects of off-axis substrate orientation on MOSFET performance and reliability are examined. As the $\langle 100 \rangle$ wafer is tilted off-axis around the $\langle 011 \rangle$ axis, two principal effects are observed. First, for current flow normal to the axis of rotation, inversion-layer mobility is lower than for current flow in the parallel direction. This mobility difference is due to anisotropy in the inversion-layer effective mass as well as increased surface roughness in the normal direction. Second, because surface roughness enhances non-uniform oxidation, thin spots in the gate oxide are generated which increase the susceptibility of the gate oxide to defect-related failure.

INTRODUCTION

For future VLSI technologies, the use of silicon substrates that have been rotated a few degrees off-axis offers several advantages. Because high quality GaAs films can be grown on such slightly-tilted off-axis surfaces [1], it is possible to integrate gallium-arsenide and silicon devices. In addition, off-axis wafers can retard ion channeling without resorting to off-axis implantation which introduces undesirable shadowing asymmetry [2]. Previous studies have examined MOSFET characteristics fabricated on different primary silicon crystal planes [3-4] or on substrates rotated through a range of large angles [5-7]. This paper examines the impact that rotating the substrate a small amount off-axis has on MOSFET performance and reliability.

DEVICE FABRICATION

The transistors and capacitors used in this study were fabricated using a NMOS technology on p-type $\langle 100 \rangle$ substrates which were rotated from 0° to 8° around the $\langle 011 \rangle$ axis. Wafers were cut from the same silicon ingot and polished identically. Each wafer received an identical boron implant for a surface substrate doping of 10^{17} cm^{-3} . Crystal orientation and the off-axis angle (θ) were determined by x-ray diffraction. Figs. 1a and 1b illustrate the wafer rotation and the approximate orientation of the expected tilt-induced steps on the surface. Note that two directions for the current flow and channel length are defined: "normal" and "parallel" to the $\langle 011 \rangle$ axis of rotation (and the tilt-induced atomic steps on the surface).

Wet and dry gate oxides from 15.6nm to 18.8nm were grown at 850°C . The wet oxidation time was 8 minutes; the dry oxidation time was 100 minutes. All gate oxides were annealed in nitrogen at 850°C for 20 minutes. After metalization, all wafers were annealed in forming gas at 400°C for 20 minutes. Table I. summarizes various oxide properties: the gate oxide type (wet vs. dry), the approximate crystallographic orientation, the oxide thickness, the mean interface-state density, the flat-band voltage, the

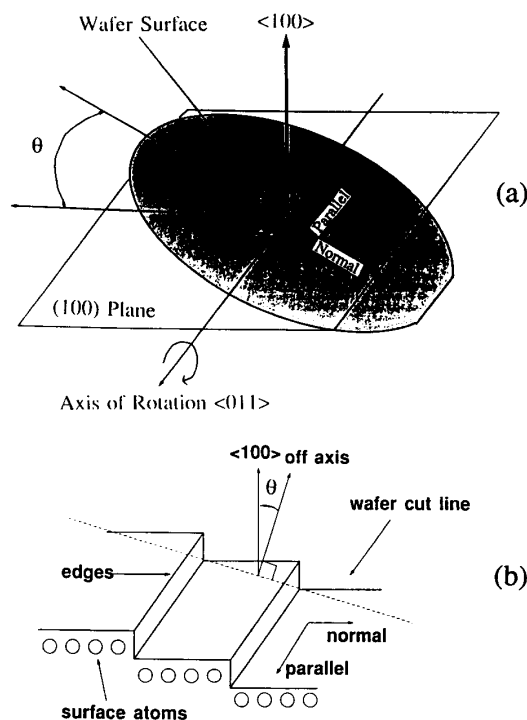


Figure 1. (a) Illustration of the wafer rotated around the $\langle 011 \rangle$ axis; the wafer has been tilted by θ° with respect to the $\langle 100 \rangle$ plane. (b) Illustration of the atomic steps on the off-axis wafer surface. Two directions of current flow (and channel length) are defined: "normal" and "parallel" to the surface steps and the $\langle 011 \rangle$ axis of rotation.

Table I

Sample	$T_{ox}(\text{nm})$	$\bar{D}_i(\text{cm}^{-2})$	$V_{FB}(\text{V})$	$\bar{Q}_{DD}(\text{C}/\text{cm}^2)$
0° wet $\langle 1,0,0 \rangle$	17.0	3×10^{10}	- 0.73	33.3
2° wet $\langle 40,1,1 \rangle$	17.0	5×10^{10}	- 0.73	33.1
4° wet $\langle 20,1,1 \rangle$	17.5	4×10^{10}	- 0.72	33.1
6° wet $\langle 16,1,1 \rangle$	18.2	4×10^{10}	- 0.71	25.9
8° wet $\langle 10,1,1 \rangle$	18.8	4×10^{10}	- 0.75	25.8
0° dry $\langle 1,0,0 \rangle$	15.6	5×10^{10}	- 0.77	24.9
5° dry $\langle 13,1,1 \rangle$	15.7	4×10^{10}	- 0.79	22.8
7° dry $\langle 23,2,2 \rangle$	16.0	3×10^{10}	- 0.77	25.0

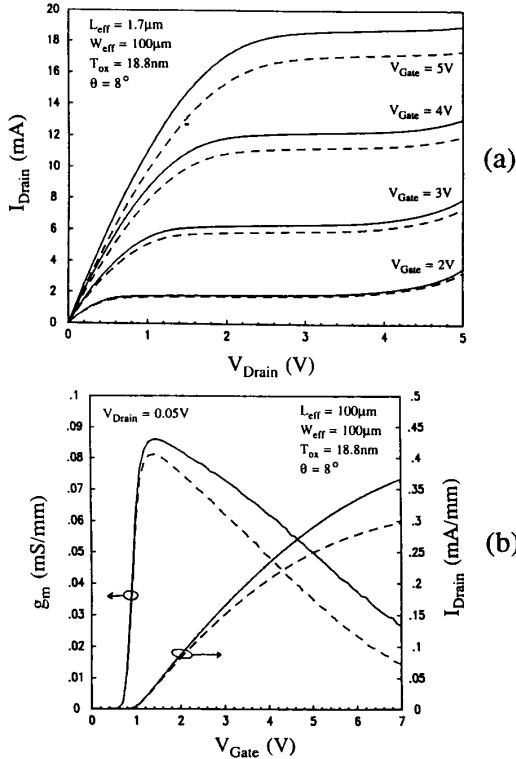


Figure 2. I-V characteristics for MOSFETs with $\theta = 8^\circ$ for (a) $L_{\text{eff}} = 1.7\mu\text{m}$ and (b) $L_{\text{eff}} = 100\mu\text{m}$. The dotted/solid line is for L_{eff} normal/parallel to the $\langle 011 \rangle$ axis of rotation (and to the surface steps).

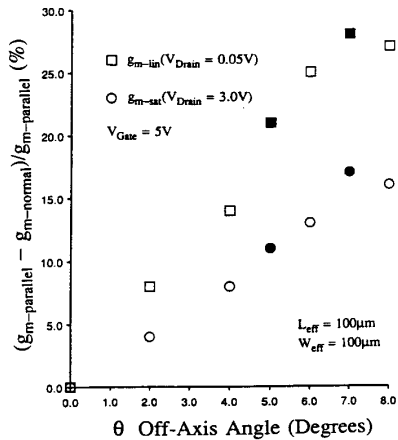


Figure 3. The percent difference between the parallel and normal current-flow directions for $g_{m\text{-in}}$ and $g_{m\text{-sat}}$ as a function of θ , the off-axis angle. The open symbols indicate wet oxide; closed symbols, dry oxide.

mean intrinsic charge-to-breakdown. It is apparent that, except for enhancing the oxidation rate due to the increased number of exposed silicon bonds [8], increasing θ has little significant effect on intrinsic oxide properties.

IMPACT ON MOSFET PERFORMANCE

I-V Characteristics: Figs. 2a and 2b show that, when devices with identical L_{eff} are compared, a considerable reduction in current drive and transconductance exists in the normal compared with the parallel direction. Fig. 3 displays the percent difference in g_m as a function of θ ; note that $g_{m\text{-sat}}$ is a less sensitive function of θ than $g_{m\text{-in}}$. This suggests that the saturation velocity is less sensitive to θ compared with the mobility.

As L_{eff} is reduced, the difference in device performance between the normal and parallel directions diminishes only slightly: a device with $L_{\text{eff}} = 0.8\mu\text{m}$ was observed to exhibit approximately 80% of the linear g_m anisotropy as a device with $L_{\text{eff}} = 100\mu\text{m}$. This behavior is due to non-scalability of the parasitic source/drain series resistance. As L_{eff} decreases, the channel resistance becomes a smaller component of the total device resistance; thus, any variation in the intrinsic channel mobility has less effect on the extrinsic measured linear g_m .

Inversion-Layer Mobility Measurements: The results in Figs. 2 and 3 can be explained by reduced surface mobility in the normal compared with the parallel direction. Inversion-layer mobility (μ_{eff}) was measured as a function of the effective electric field (E_{eff}) [9]. In Fig. 4, μ_{eff} in the normal and parallel directions for $\theta = 8^\circ$ is plotted as a function of E_{eff} for temperatures from 77 °K to 360 °K.

Various experimental and theoretical studies [10-12] generally agree that at higher temperatures and lower E_{eff} , μ_{eff} is determined primarily by coulomb and phonon scattering, whereas at lower temperatures and higher E_{eff} , surface roughness becomes the dominant scattering mechanism. From Fig. 4, it is apparent that, at $T > 298^\circ\text{K}$ and $0.2\text{MV/cm} < E_{\text{eff}} < 0.6\text{MV/cm}$, $\mu_{\text{eff}} \propto E_{\text{eff}}^{-1/3}$; this agrees with behavior predicted by phonon-scattering models [13]. Likewise from Fig. 4, it is also apparent that, at $T = 77^\circ\text{K}$ and $E_{\text{eff}} > 0.4\text{MV/cm}$, $\mu_{\text{eff}} \propto E_{\text{eff}}^{-2}$; this agrees with behavior predicted by surface-roughness scattering models [14]. Note that both $\mu_{\text{eff-normal}}$ and $\mu_{\text{eff-parallel}}$ exhibit similar dependences on temperature and E_{eff} . Thus, the same scattering mechanisms probably determine the mobility in the normal and parallel directions.

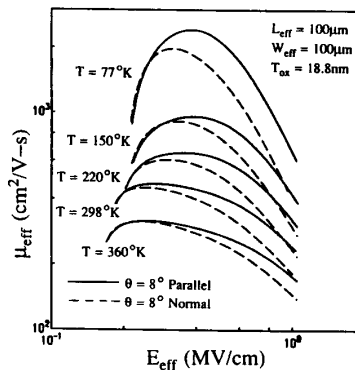


Figure 4. The effective surface mobility (μ_{eff}) in the normal and parallel directions as a function of the effective electric field (E_{eff}) for $\theta = 8^\circ$.

Inversion-Layer Mobility Anisotropy: Fig. 5 displays the intraplanar mobility ratio ($\mu_{\text{eff-normal}}/\mu_{\text{eff-parallel}}$), the ratio between the normal and parallel mobilities for fixed θ , as a function of E_{eff} . It is observed that $\mu_{\text{eff-normal}}/\mu_{\text{eff-parallel}}$ is a monotonically decreasing function of both θ and E_{eff} . Fig. 6 displays the intraplanar mobility ratio ($\mu_{\text{eff}}/\mu_{\text{eff}}(\theta = 0^\circ)$), mobility normalized to its value at $\theta = 0^\circ$, as a function of the off-axis angle. Whereas $\mu_{\text{eff-normal}}$ is almost linearly dependent on θ , $\mu_{\text{eff-parallel}}$ is almost independent of θ until the amount of rotation is greater than 6° . Also, as the temperature decreases, the degree of mobility anisotropy increases. In Figs. 5 and 6, no significant difference appears to exist between the wet and dry gate oxides.

The difference between $\mu_{\text{eff-normal}}$ and $\mu_{\text{eff-parallel}}$ can be explained by two different physical mechanisms.

1. Because of the structure of the silicon conduction bands, the inversion-layer effective mass (m_{eff}) is a tensor whose value depends on the particular current-flow direction [3,5]. For the $\langle 100 \rangle$ plane, the effective mass happens to be isotropic. However, when the wafer is rotated off-axis around the $\langle 011 \rangle$ axis, various theoretical studies [3,5] have shown that the inversion-layer effective mass in the normal direction becomes heavier than in the parallel direction. Since $\mu_{\text{eff}} = q\tau/m_{\text{eff}}$, an anisotropic mobility results.
2. As the wafer is rotated off-axis, surface steps are expected to appear in the normal direction (see Fig. 1b). Assuming the steps are diatomic in height [15], the step spacing should be less than 10 nm for $\theta = 8^\circ$. This distance is on the order of the surface mean-free path [14]. One expects that, since electrons must travel over the steps rather than along side them, the effects of surface roughness in the normal direction should be greater than in the parallel direction.

Qualitatively, both of the above mechanisms can explain the experimental results in Figs. 5 and 6. When E_{eff} increases or when the temperature decreases, the effective mass tensor changes [3,5] such that the effective-mass anisotropy increases. Likewise, surface roughness also becomes a more dominant scattering mechanism when E_{eff} increases or when the temperature decreases [14]; this too results in increased mobility anisotropy. It is likely that some combination of both mechanisms is responsible for the experimental results.

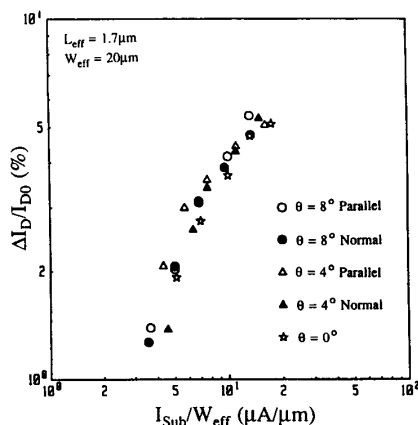


Figure 7. Hot-electron current degradation ($\Delta I_D/I_{D0}$) as a function of $I_{\text{Sub}}/W_{\text{eff}}$. Stressing was performed at peak I_{Sub} .

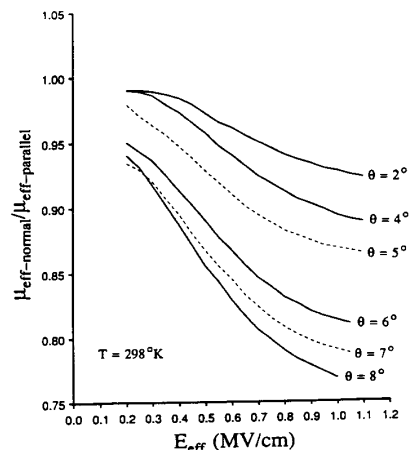


Figure 5. Anisotropic effective surface mobility ratio ($\mu_{\text{eff-normal}}/\mu_{\text{eff-parallel}}$) as a function of E_{eff} . The solid line indicates wet oxide; the dashed line, dry oxide.

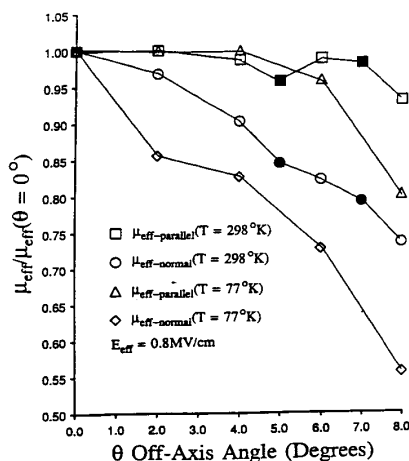


Figure 6. Normalized effective surface mobility ratio ($\mu_{\text{eff}}/\mu_{\text{eff}}(\theta = 0^\circ)$) at $E_{\text{eff}} = 0.8 \text{ MV/cm}$ as a function of θ for the normal and parallel directions. The open symbols indicate wet oxide; closed symbols, dry oxide.

IMPACT ON MOSFET RELIABILITY

Hot-Electron Degradation: For devices in the normal direction, substrate current was observed to be a weak decreasing function of θ . This decrease in I_{Sub} can be explained by the reduction in drain current which is a consequence of the lowered mobility. In Fig. 7, hot-electron degradation (the percent forward-linear current degradation measured at $V_G = 5\text{V}$) is plotted versus the stress substrate current. Changing θ or the direction of current flow (normal vs. parallel) is observed to have little influence on the amount of degradation.

Gate Oxide Quality: In Fig. 8 a significant reduction in the oxide breakdown field for wet oxides is observed as θ is increased; similar behavior is observed for dry oxides. However, from Fig. 9 it appears that changing the off-axis angle has little effect on oxide trapping behavior. Thus, from Table I., Fig. 7, and Fig. 9, one can conclude that changing θ appears to have

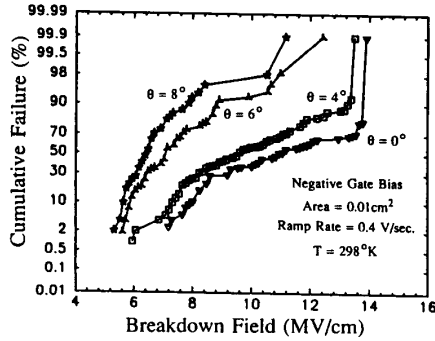


Figure 8. Cumulative failure ramp breakdown data for gate oxide grown on substrates with differing θ .

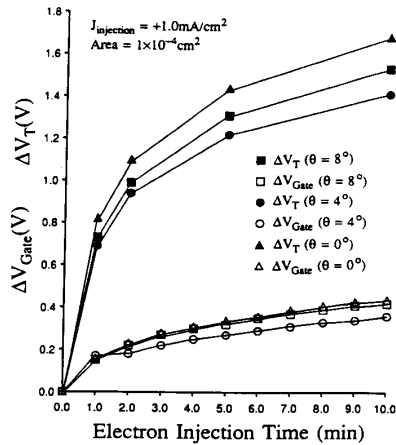


Figure 9. Trapping characteristics for oxides on $\theta = 0^\circ$, 4° , and 8° wafers. Threshold voltage shift (closed symbols) and the gate bias necessary for a constant electron injection (open symbols) as a function of electron injection time.

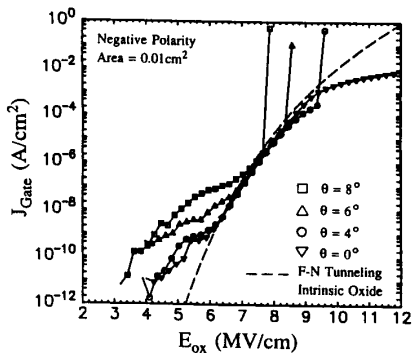


Figure 10. Gate current density as a function of oxide electric field for different θ . The dotted line indicates the Fowler-Nordheim tunneling characteristic for intrinsic oxide.

minimal effect on such intrinsic oxide properties as fixed charge, trapping behavior and hot-electron degradation.

Surface roughness has been shown to enhance non-uniform oxidation [16] as well as correlate with defect-related oxide reliability degradation [17]. A likely explanation for the decrease in breakdown field in Fig. 8 is the creation of thin regions in the oxide, due to the roughness-induced non-uniform oxidation, which appear as defects. For small values of θ where the wafer is smooth, the breakdown distribution is likely determined by various different mechanisms [18]: oxide thin spots, surface asperities, localized barrier height lowering, an increased oxide trap generation rate. However, as θ increases, the surface roughness increases; this enhances non-uniform oxidation and the creation of oxide thin spots.

The presence of thin-oxide regions is supported by Fig. 10 which plots gate current density as a function of oxide field. As θ increases, gate current is observed at E_{ox} values well below what is expected for intrinsic Fowler-Nordheim tunneling. It is possible that this current is due to tunneling through existing thin-oxide regions.

CONCLUSION

Rotating the $\langle 100 \rangle$ substrate around the $\langle 011 \rangle$ axis has been shown to have two major consequences: the introduction of orientation-dependent device performance due to mobility anisotropy, and an increase in defect-related oxide breakdown. The performance anisotropy may possibly be alleviated by rotating substrates in the $\langle 001 \rangle$ direction, such that the normal and parallel directions possess equivalent inversion-layer effective mass [5] and degrees of surface roughness. The oxide quality may possibly be improved by using a two-step oxidation procedure [19], where an intermediate high-temperature anneal is used to smooth the oxide. However, unless the above two issues are satisfactorily addressed, future VLSI technologies using off-axis substrates may face potential performance and reliability problems.

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