

# A NEW APPROACH FOR SIMULATION OF CIRCUIT DEGRADATION DUE TO HOT-ELECTRON DAMAGE IN NMOSFETS

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## ABSTRACT

In this paper, we present a new approach for modeling hot-electron induced change in drain current for both forward and reverse modes of operation. The change in drain current,  $\Delta I_D$  is implemented as an asymmetrical voltage controlled current source. We will first present the physical basis of the model and derive the analytical model equations. This will be followed by the implementation scheme for the analytical  $\Delta I_D$  model in BERT (BERkeley Reliability Tool) simulator and a detailed evaluation of the model as a function of different device and circuit parameters. Finally simulation results of uni-directional and bi-directional circuits based on the new model will be presented.

## I. INTRODUCTION

Hot-electron induced MOSFET degradation is becoming an increasing concern for constant voltage scaling. Although physical mechanisms for hot-electron damage have been extensively studied [1-5], a clear understanding of hot-carrier effects in an actual circuit environment [6-7] is essential to ensure product reliability and to the evaluation of hot-carrier reliability in the early stages of process optimization. Hot-carrier reliability programs which can predict circuit reliability can form an integral part of this process. Simulation tools, such as CAS [8], HOTRON [9], and RELY [10] have been developed to predict circuit reliability. Accurate modeling of fresh and degraded drain current in these simulation tools require the tedious and often difficult task of generating stressed process files.

In this paper, we present a new approach for modeling the hot-electron induced change in the drain current ( $\Delta I_D$ ) for forward and reverse operation and for uni-directional and bi-directional stress. The new  $\Delta I_D$  model is adaptable to any SPICE model and does not require any stressed process files. This can simplify the process of predicting circuit degradation. Conventional NMOSFET's with  $T_{ox} = 17.0\text{nm}$  and  $L_{eff} = 0.6 - 5.0\mu\text{m}$  are used for this study.

## II. PHYSICAL BASIS OF $\Delta I_D$ MODEL

Fig.1 shows the fresh  $I_D$ , degraded  $I_D$ , and  $\Delta I_D$  due to hot-electron stressing. In Fig.2,  $\Delta I_D/I_D$  and  $\Delta I_D$  are shown as function of  $V_{DS}$ . The forward  $\Delta I_D/I_D$  initially increases with  $V_{DS}$ , peaks at a voltage lower than  $V_{DSAT}$ , and eventually decreases. Studies [1-5] have shown that NMOS hot-electron damage is dominated by acceptor type interface states. For low  $V_{DS}$ , the interface states are occupied and negatively charged thus resulting in the flat  $\Delta I_D/I_D$  region (I). In region I as  $I_D$  increases with  $V_{DS}$ ,  $\Delta I_D$  also increases. As  $V_{DS}$  is further increased the lowering of the quasi fermi level decreases the number of charged states. This results in the  $\Delta I_D/I_D$  roll-off in region II. As shown in fig.2, the slope of this region is a function of  $V_{GS}$ . We now have two

competing mechanisms: 1) the deviation of  $I_D$  from its linear  $V_{DS}$  dependence due to velocity saturation effects, and 2) the decreasing  $\Delta I_D/I_D$  due to the reduction of charged interface states. These two mechanisms causes  $\Delta I_D$  to peak at a voltage lower than  $V_{DSAT}$  and then linearly decrease with  $V_{DS}$  (region II). Beyond  $V_{DSAT}$ , the channel pinchoff region ( $\Delta L$ ), partially screens the damage, causing  $\Delta I_D/I_D$  to deviate from its linear  $V_{DS}$  dependence (region III). In the reverse mode (source and drain switched after hot-electron stressing), the damage is located near the source and no reduction in occupied states occurs as  $V_{DS}$  is increased. Thus  $\Delta I_D/I_D$  remains constant and reverse  $\Delta I_D$  tracks the  $I_D$  behaviour as shown in Fig. 1.

## III. $\Delta I_D$ MODEL

Recent study [11] on dynamic degradation of MOSFETs has shown that in digital circuits interface traps is the dominant hot-carrier degradation mechanism of NMOSFETs. Fig.3a shows a NMOSFET cross-section with a damaged region of length  $\delta L$  and a uniform interface-state charge density,  $N_{it}$ . Interface-layer mobility,  $\mu$ , due to hot hot-carrier damage has been empirically modeled as [12],

$$\mu = \mu_{eff}(1 + KN_{it}) \quad (1)$$

where  $\mu_{eff}$  corresponds to inversion-layer mobility of a fresh device. Assuming that all the interface states are charged (which holds only for very small  $V_{DS}$ ), the percent degradation of drain current,  $I_{D0}$  has been modeled as [13],

$$\Delta I_D/I_{D0} = CK(\delta L/L_{eff})(t_{stress}I_D^n/I_D^{m-1}W_{eff})^n \quad (2)$$

where C is a technology constant, n is the time dependence of degradation and m is the slope of lifetime plot [10]. With  $E_{eff} = (V_G - V_T)/6T_{ox}$ , K is given by [13]

$$K = 3.2 \times 10^{-12} \text{cm}^2/[1 + (2.66 \times 10^6 E_{eff})^{2.25}] \quad (3)$$

However for circuit simulation a model for the entire  $V_{DS}$  range is needed.

**Forward Mode  $\Delta I_D$ :** In the previous section, we showed that the forward mode has three distinct regions: two in the linear region and one in the saturation region.

**Linear Region:** We first define  $\text{Age}(t)_{for}$  and the fresh drain current  $I_{D0}$  [14] as

$$\text{Age}(t)_{for} = C f(t_{stress}I_D^n/I_D^{m-1}W_{eff}) \quad (4)$$

$$I_{D0} = \frac{W}{L} C_{ox} \mu_{eff} (V_G - V_T) - \frac{1}{2} V_D |V_D| \left[ \frac{1}{(1 + V_D/E_{sat}L)} \right] \quad (5)$$

Using equs. 2-5 and defining  $V_{PK}$  as the voltage at which  $\Delta I_D$  peaks, we model region I (low  $V_{DS}$ ) as,

$$(\Delta I_D)_I = I_{D0} K \left( \frac{\delta L}{L_{eff}} \right) [\text{Age}(t)_{for}] \quad V_{DS} < V_{PK} \quad (7)$$

In region II,  $\Delta I_D/I_D$  was empirically determined to have a linear  $V_{DS}$  dependence and a  $1/(V_G - V_T)^{1.2}$  dependence.  $\Delta I_D$  in region II can then be expressed as,

$$(\Delta I_D)_D = (\Delta I_D)_1 \frac{(1 - A_1(V_D - V_{PK}))}{\sqrt{(V_G - V_T)}} \quad V_{PK} < V_{DS} < V_{DSAT} \quad (8)$$

From eqs. 7 and 8, we find that  $V_{PK} = A_2 V_{DSAT}$ , where  $A_2$  is a constant for a given technology and  $A_1$  is a fitting paramter.

**Saturation Region:** Fig.3b shows the cross-section of NMOS-FET in the saturation region with channel pinch-off region,  $\Delta L$ . Since the channel pinch-off region screens off part of the damage, only  $(\delta L - \Delta L)$  portion of the damaged region effects the inversion-layer mobility. The drain current and the channel voltage,  $V(y)$  is related by [14],

$$\frac{dV(Y)}{dy} = \frac{I_D}{[W\mu C_{ox}(V_G - V(y)) - I_D]/E_{sat}} \quad (9)$$

Integrating from  $y = 0$  to  $y = L_{eff} - \Delta L$  with  $V(0) = 0$ ,  $V(y) = V_{DSAT}$ , we obtain for  $V_D > V_{DSAT}$ ,

$$\Delta I_D = I_{DSAT} \frac{1 - A_1(V_{DSAT} - V_{PK})}{\sqrt{V_G - V_T}} K \frac{\delta L - \Delta L}{L_{eff} - \Delta L} Age(t)_{for} \quad (10)$$

where the saturation voltage of the fresh device is given by

$$I_{DSAT} = \frac{W V_{sat} C_{ox} (V_G - V_T)^2}{(V_G - V_T) + E_{sat} L} \frac{V_{DSAT} + E_{sat} L}{V_{DSAT} + E_{sat} (L - \Delta L)} \quad (11)$$

**Reverse Mode  $\Delta I_D$ :** In the reverse mode (drain and source switched after stress) the damage is located near the source and not the drain. With the  $(Age)_{rev}$  as the reverse age the reverse mode  $\Delta I_D$  can be expressed as,

$$\Delta I_D = I_{D0} K \frac{\delta L}{L_{eff}} Age(t)_{rev} \quad V_{DS} < V_{DSAT} \quad (12)$$

$$\Delta I_D = I_{DSAT} K \frac{\delta L}{L_{eff}} Age(t)_{rev} \quad V_{DS} > V_{DSAT} \quad (13)$$

The  $\Delta I_D$  model equations presented above require only six parameters:  $m$ ,  $n$ ,  $C$ ,  $A_1$ ,  $A_2$ ,  $\delta L$ . All these six parameters can be extracted from simple stress experiments.

#### IV. MODEL IMPLEMENTATION

In this section we will discuss the implementation scheme of the  $\Delta I_D$  model in BERT (BERkeley Reliability Tool). The hot-electron induced asymmetrical change in drain current is implemented as a voltage controlled current source as shown in Fig.4. By including the sign of  $V_{DS}$  in the  $\Delta I_D$  model, the asymmetrical drain current can easily be simulated. Bi-directional hot-electron stress proceeds independently of each junction [15]. Fig.4c shows that after a bi-directional stress, both source and drain have a damaged region. We include the effect of bi-directional stress by a linear superposition of the contributions from the forward mode  $\Delta I_D$  and the reverse mode  $\Delta I_D$ .

Fig.5 shows the two different implementation schemes we have developed. In method I,  $\Delta I_D$  equations are implemented outside SPICE and the second pre-BERT step adds a voltage controlled current source to the SPICE input file. This scheme thus requires no modification of the existing SPICE source codes. In the second method, the second pre-BERT step adds the forward and the reverse Ages to each transistor card in the SPICE input file. The original  $I_D$  of NMOSFET in SPICE is multiplied by the hot-carrier degradation factor based on the forward and the reverse Ages calculated by BERT. Thus if  $I_{D0}$  is the fresh drain current, then in the forward operating mode ( $V_{DS} > 0$ ), the SPICE drain current equation is modified to the following

$$I_D = I_{D0} [1 - ((\Delta I_D)_{for}/I_{D0}) + ((\Delta I_D)_{rev}/I_{D0})] \quad (14)$$

where  $(\Delta I_D)_{for}$  and  $(\Delta I_D)_{rev}$  are the  $\Delta I_D$  equations due to forward and reverse ages given above. In the reverse operating mode ( $V_{DS} < 0$ ), the  $I_D$  equation is same as eq. 14, except that  $Age_{for}$  and  $Age_{rev}$  are swapped and  $\delta L_F$  and  $\delta L_R$  are swapped. Since the hot-carrier drain current degradation is implemented as an adjustment factor to the original  $I_D$  equation in SPICE, both implementation schemes are adaptable to any SPICE MOS level.

#### V. EXPERIMENTAL AND SIMULATION RESULTS

**Model Verification:** Fig.6. demonstrates the  $(V_{GS} - V_T)$  dependence of the model in the three regions discussed in sections II and III. Figs. 7 and 8 show very good agreement between the modeled and measured values of  $\Delta I_D$  for different  $V_{GS}$ , and  $L_{eff}$  respectively. In order to evaluate the accuracy of the bi-directional model, we stressed each junction of a NMOSFET independently for 20 minutes. Fig. 9 shows that the model can accurately predict the degradation of both source and drain due to bi-directional stress.

**Circuit Simulation:** We simulated a ring oscillator and a dynamic latch as illustrations of uni-directional stress and bi-directional stresses respectively. Fig. 10 shows the simulated fresh and degraded waveform of the ring oscillator after 10 years of aging. Fig. 11a is the schematic of the dynamic latch and fig.11b is the stressing waveform. Fig 12 shows the simulated fresh and degraded waveform of the dynamic latch. Curve a is the fresh waveform, curve b is the degraded waveform with only uni-directional model and curve c is the degraded waveform when the bi-directional model is included. We can clearly see that the uni-directional model underestimates the degradation.

#### VI. CONCLUSION

A new approach for simulation of circuit degradation due to hot-electron damage in NMOSFETs is presented. Hot-electron damage is modeled as a bi-directional voltage controlled current source ( $\Delta I_D$ ) which does not require any stressed process files. The new  $\Delta I_D$  hot-electron model is adaptable to any SPICE model and requires only six parameters which can be extracted from simple stress experiments. Good agreement has been obtained between the modeled and experimental data for different  $V_{GS}$ ,  $L_{eff}$ , stressing time and stressing drain voltage. Simulation results show that the new approach can be extremely useful in accurately predicting both uni-directional and bi-directional circuit degradation.

#### ACKNOWLEDGEMENT

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#### REFERENCES

- [1] C. Hu, et al, IEEE Tran. Elec. Dev., Vol. 32, p. 375, 1985.
- [2] E. Takeda, et al, IEDM Technical Digest, p. 60, 1985.
- [3] P. Heremans, et al, IEEE Tran. Elec. Dev., Vol. 35, p. 2194, 1988.
- [4] J. Choi, et al, J. Appl. Phys., Vol. 65, p. 354, 1989.
- [5] B. Doyle, et al, IEEE Tran. Elec. Dev., Vol. 37, p. 744, 1990.
- [6] S. Aur, IEDM Technical Digest, p.498, 1987.
- [7] Wang et al., EDL-12, No. 5, p. 238, 1991.
- [8] P. Lee, et al, IEDM Technical Digest, p. 134, 1988.
- [9] S. Aur, IEDM Technical Digest, p.498, 1987.
- [10] W. Hsu, et al., Proc. of the IEEE 1988 CICC, p. 27.4.1, 1988.
- [11] W. Weber, et al., IEEE Trans. Elec. Dev., Vol. 38, p. 1859, 1991.
- [12] S. Sun et al., IEEE Trans. Elec. Dev., Vol. 27, p. 1497, 1980.
- [13] J. Chung, et al., IEEE Trans. Elec. Dev., vol. 38, p. 1362, 1991.
- [14] P. Ko, VLSI Elec: Microstructure Sci., Vol. 18, Ch.1, 1989.
- [15] K. Mistry, et al., EDL-11, No. 37, p. 2415, 1990.

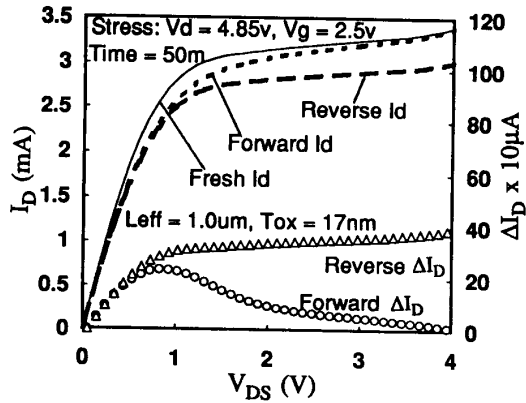


Fig.1 NMOS drain current  $I_D$  and change in drain current,  $\Delta I_D$ , as a function of drain voltage,  $V_{DS}$  after hot-electron stressing.

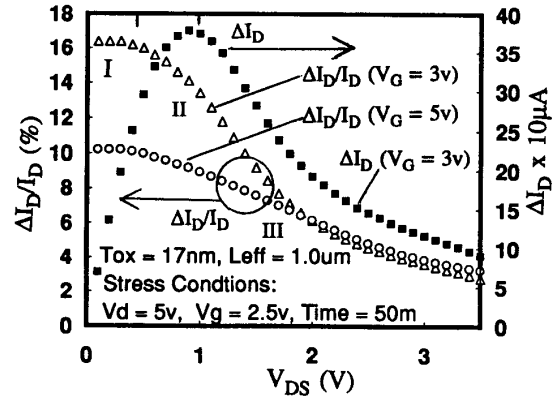


Fig.2 Percent change in drain current  $I_D$ , and change in drain current,  $\Delta I_D$  in forward mode as a function of drain voltage. I = linear 1, II = linear 2, and III = saturation.

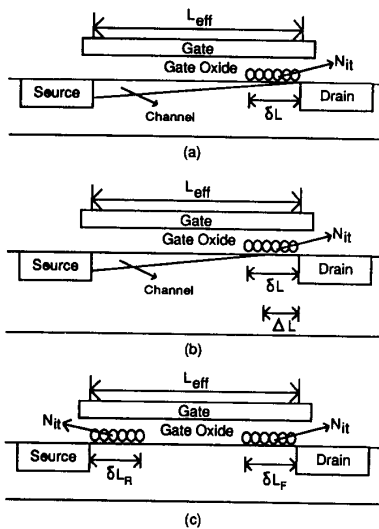


Fig.3 Interface trap dominated  $\Delta I_D$  model: a) Linear region, b) Saturation region, and c) bi-directional mode.  $\delta L$  is hot-electron damage region,  $\Delta L$  is pinch off region,  $\delta L_F$  and  $\delta L_R$  are the forward and reverse damage region.

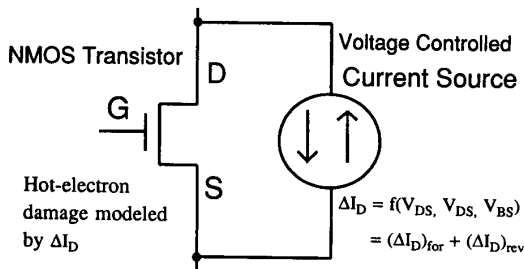


Fig.4 Change in drain current  $\Delta I_D$  stressing, modeled as a bi-directional voltage controlled current source.

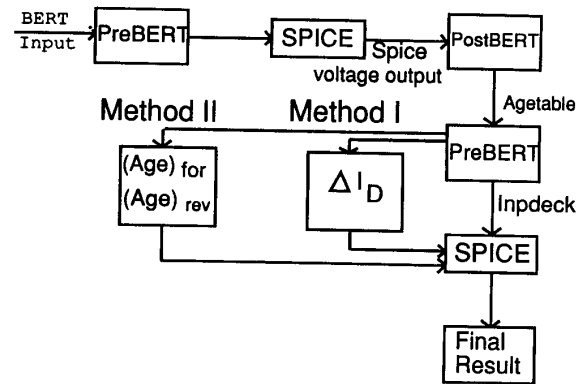


Fig.5 Flowchart for  $\Delta I_D$  model implementation in BERT. Method I requires no SPICE modification. Method II requires simple multiplicative change to  $I_D$  in SPICE.

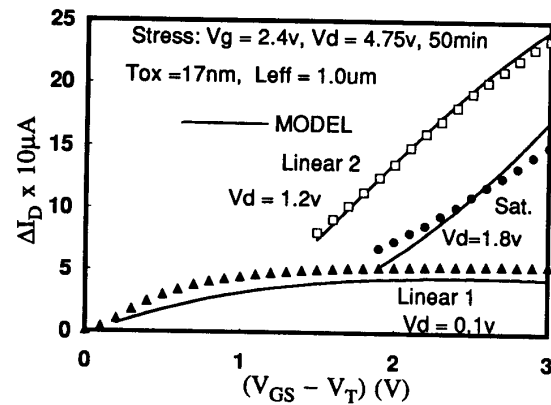


Fig.6 Dependence of the change in drain current  $\Delta I_D$  on  $(V_{GS} - V_T)$  in the three regions: linear I, linear II, and saturation.

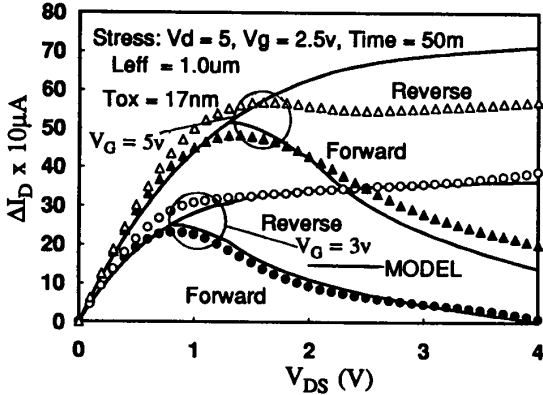


Fig. 7 Change in drain current  $\Delta I_D$  in forward and reverse modes as a function of  $V_{DS}$  for  $V_{GS} = 3v$  and  $V_G = 5v$ .

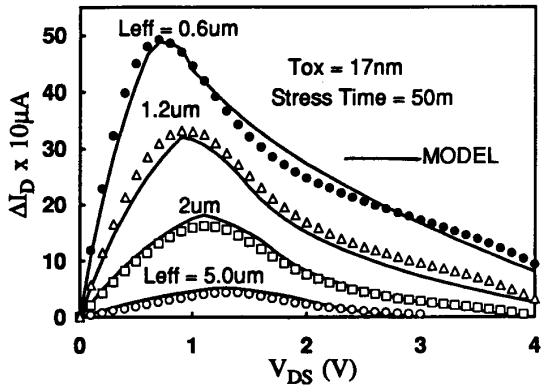


Fig.8 Change in drain current  $\Delta I_D$  in forward mode as a function of  $V_{DS}$  for different  $L_{eff}$ .

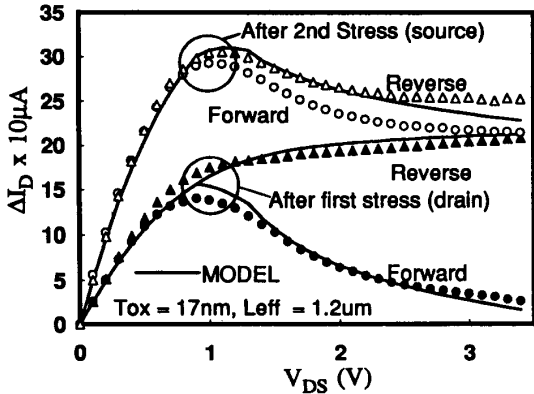


Fig.9 Change in drain current  $\Delta I_D$  in forward and reverse modes as a function of  $V_{DS}$  after bi-directional stress. Each junction independently stressed for 20min.  $\Delta I_D$  modeled as a linear sum of drain and source stresses.

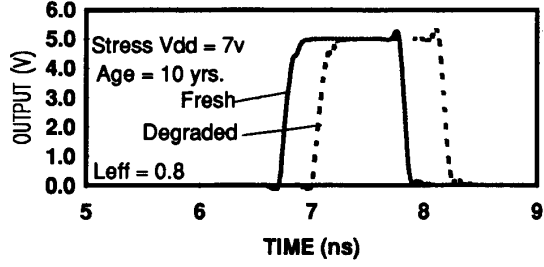


Fig.10 Hot-carrier degradation simulation of a 17-stage ring oscillator using the new  $\Delta I_D$  model in BERT.

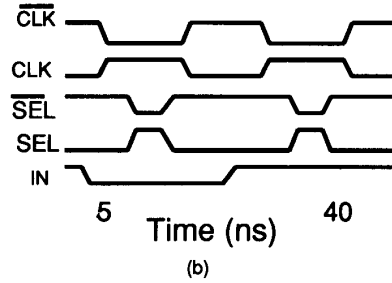
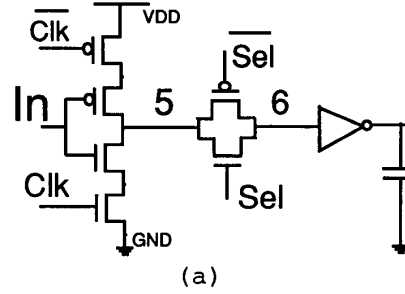


Fig.11 a) Schematic of a dynamic latch, and b) Waveform used in simulating the bi-directional degradation of the dynamic latch.

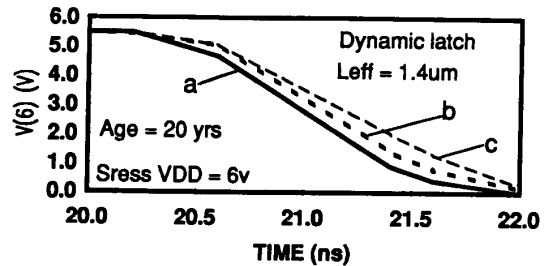


Fig.12 Hot-carrier degradation simulation of a dynamic latch using the new  $\Delta I_D$  model in BERT. a, b and c are the fresh, degraded(uni-directional model only), and degraded (bi-directional model) waveforms respectively.