INTERFACE QUALITY OF SOI MOSFET'S REFLECTED IN NOISE AND MOBILITY

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It is desirable to measure SOI MOSFET interface trap density for front and back interfaces. However, since SOI MOSFET's substrate is floating, normal quasi static CV and charge pumping methods cannot be used. In this paper, we estimate the trap density of both front and back interfaces of SOI devices using low frequency noise measurement. To date there is no systematic comparison between the mobility μ_{eff} of the front and back interfaces. Here we present the complete set of effective mobilities for both N- and and P-channel SOI MOSFET's at both the front and back channels and relate them to the trap densities.

The SOI devices used in this study were fabricated using a modified sub-micron CMOS technology on SIMOX wafers. A computer-controlled test system was used to conduct the I-V and noise measurements automatically[1]. The N- and P-channel MOSFET's used are all fully depleted and therefore do not have drain current kink and do not exhibit drain current noise overshoot[2]. From [1] and [3], in the strong inversion region, the relative spectral density of drain current fluctuations can be expressed as: $S_{Id}/I_D^2 = KN_t/f^{\gamma}\beta^2Q_n^2$ where γ=0.8 to 1.2, $K=q^4\lambda/LWkT$, L and W are device channel length and width, respectively. $\lambda=\hbar\,(8m^*\phi)^{-1/2}$ is the tunneling constant for electrons, and ϕ the energy barrier for tunneling electrons. $N_t(eV^{-1}.cm^{-3})$ is the oxide trap density near the conduction band, $\beta=q/kT$, and Q_n is the inversion layer charge. $Q_n\,S_{Id}/I_D^2$ is therefore independent of drain voltage and simply proportional to trap density as plotted in Fig.1. The mean interface-state densities were calculated as below using that the noise originates from a small region within oxide of about 10Å. The D_{it} for bulk MOSFET was calibrated with high frequency and quasi-static CV method.

Device	N SOI Front	N SOI Back	N Bulk	P SOI Front	P SOI Back
$D_{it}\,(eV^{-1}.cm^{-2})$	4×10^{11}	2.4×10^{11}	3×10^{10}	9×10^{9}	8×10^{9}

It can be seen that the front and back D_{it} are similar. In addition, the SOI device exhibit about 10 times higher D_{it} than bulk device. The D_{it} for PMOS are much lower than in NMOS as expected. Fig.2 shows that S_{ID}/I_D^2 vary from weak to strong inversion which are in agreement with theory, thus truly originated form the MOSFET channel.

The trap density results from noise was reflected in the low-field mobility study as well. Low-field effective mobility μ_{eff} was determined by measuring the I_D-V_G at V_D=50mV. The drain current is given by $I_D=\mu_{eff}(W/L)V_DQ_n$, where Q_n is the inversion charge density. For the front gate, Q_n is calculated by integrating C_{GDS} vs. V_G. For the back gate, since C-V data is difficult to interpret, Q_n was calculated using $Q_n=C_{BOX}(V_{BG}-V_{BT})$. The front and back channel μ_{eff} for both N and P SOI MOS are presented in Fig.3. The expected μ_{eff} for bulk N and P MOS are also shown for comparison [4]. It can be seen that there is very little difference between the μ_{eff} for the front and back sides of both the N- and P- SOI devices. This agrees with the trap density results shown above, suggesting that the interface quality of the front and back sides are similar. It is interesting to note that the very low field μ_{eff} for the N-SOI devices are lower than that of the bulk devices. This is due to the much higher interface trap density in SOI devices as effect of interface traps on μ_{eff} is most pronounced at low field [5]. As for SOI PMOS, the interface trap density is also higher than that of the bulk devices. However, the actual density is low enough that no significant effect can be seen on the μ_{eff}. Based on μ_{eff} of N-SOI and bulk device at 0.3MV/cm, it is calculated that the relative increase in the interface trap density to be around $2\times10^{11}cm^{-2}$, which agrees with trap density results from noise measurements.

Fig.4 shows the dependence of μ_{eff} on the thickness of the silicon film for both N and PMOS. It can be seen that as the thickness of the silicon film decreases, there is a slight increase in the μ_{eff} for both device types as predicted by theory [6]. The μ_{eff} for narrow width, i.e., the field-edge transistor was also investigated. The silicon film is much thinner at the edge due to the LOCOS process [7]. It is shown in Fig.5 that the μ_{eff} of those devices were considerably lower than those of wider devices. This is also confirmed by the smaller slope in the narrow width region as shown in Fig.6. The lower mobility of the narrow transistors is probably caused by the higher stress and/or higher D_{it} at the film edge.

In conclusion, it is found that the interface quality of the front and back sides are similar in SIMOX SOI MOSFET's from the noise and mobility standpoint. The very low field μ_{eff} of SOI NMOS is lower than that of bulk NMOS due to increased interface trap densities for SOI devices and the μ_{eff} of the edge transistor is lower.

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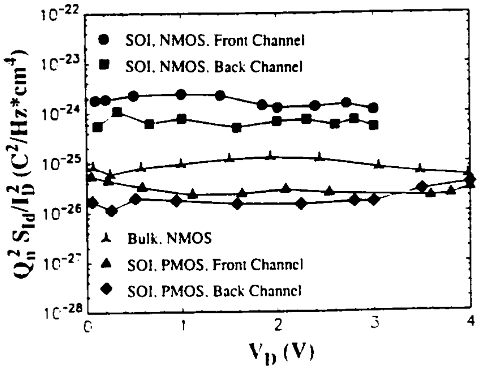

Fig.1 Low frequency drain current noise spectrum intensity for SOI and bulk devices. $Q_n^2\ S_{Id}/I_D^2$ is proportional to oxide trap density N_t.

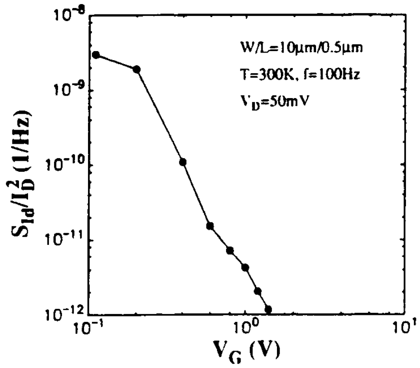

Fig.2 S_{Id}/I_D^2 in the whole range from weak to strong inversion regime.

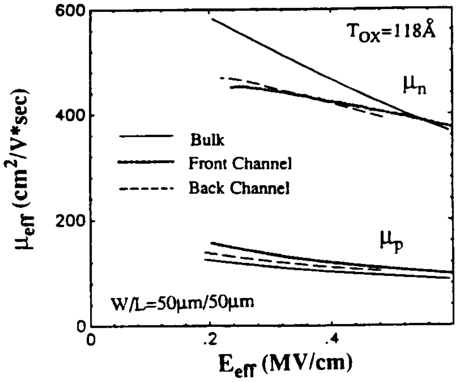

Fig.3 Low-field mobility of SOI devices compared with bulk mobility.

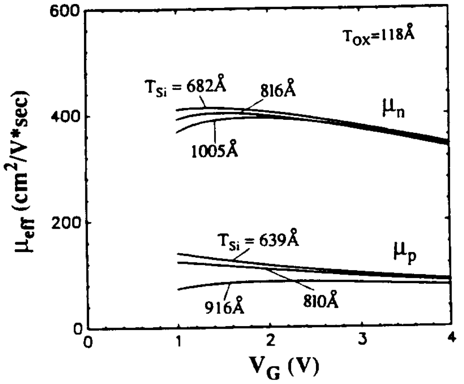

Fig.4 SOI silicon film thickness dependence of effective mobility.

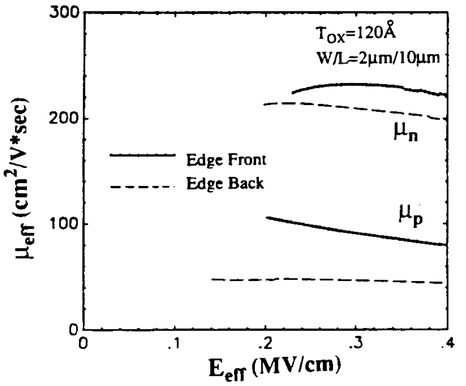

Fig.5 Low-field mobility of edge transistor in SOI devices.

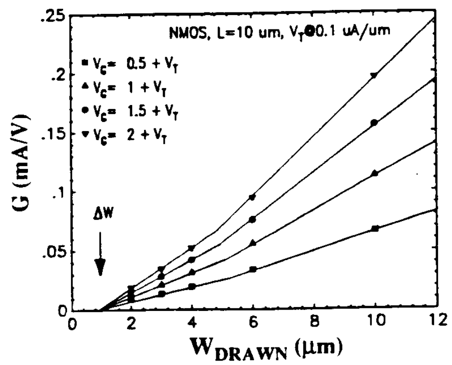

Fig.6 Conductance vs. drawn channel width showing the change in μ_{eff} due to change in width.