

# A *CV* Technique for Measuring Thin SOI Film Thickness

Jian Chen, *Student Member, IEEE*, Ray Solomon, Tung-Yi Chan, Ping-Keung Ko, *Member, IEEE*, and Chenming Hu, *Fellow, IEEE*

**Abstract**—A technique is developed to measure silicon-on-insulator (SOI) silicon device film thickness using a MOSFET. The method is based on *CV* measurements between gate and source/drain at two different back-gate voltages. This method is simple, nondestructive, and no special test structure is needed. Using this technique, SOI film thickness mapping was made on a finished wafer and a thickness variation of  $\pm 150 \text{ \AA}$  was found.

## I. INTRODUCTION

SILICON-on-insulator (SOI) technology is becoming a promising candidate for future VLSI, as the quality of SOI material continues to improve. Thin SOI film thickness (less than  $1000 \text{ \AA}$ ) is important for improvements in short-channel effects and elimination of the current kinks in SOI MOSFET's [1]. Nonuniformity in the SOI film thickness can result in nonuniformities in those characteristics and in threshold voltage. Normally TEM and ellipsometry are used to measure the SOI film thickness, but these methods are either inconvenient, destructive, or can only be performed on starting wafers. It is helpful to have an electrical technique that can measure SOI wafer thickness across the finished wafers.

Most electrical methods for measuring SOI film thickness require special structures [2], [3]. Others deduce silicon film thickness from the dependence of threshold voltage on back-gate voltages [2], [4]. However, threshold voltage also dependent on the doping concentration and transient phenomena in SOI MOSFET can cause  $V_T$  measurement inaccuracies [5]. This paper presents a *CV* measurement technique that is simple and direct.

## II. *CV* METHOD FOR MEASURING SOI FILM THICKNESS

The SOI devices used in this study were  $n^+$  polysilicon gate  $n$ -channel MOSFET's fabricated with modified submicrometer CMOS technology on SIMOX (Separation by Implanted OXYgen) wafers. The SIMOX wafers were implanted with a high dose of oxygen ions ( $10^{18} \text{ cm}^{-2}$ ) at 200 keV and subsequently annealed at  $1230^\circ\text{C}$ . The NMOS threshold boron implant dose is  $2 \times 10^{12} \text{ cm}^{-2}$ . Lateral isolation is obtained by LOCOS. The polysilicon gate thickness, gate

oxide thickness, and buried-oxide thickness are 2500, 118, and  $3600 \text{ \AA}$ , respectively. Large-area transistors with  $W/L = 50/50 \text{ \mu m}$  were used to measure SOI film thickness.

Fig. 1 shows the basic idea of this *CV* technique for measuring SOI film thickness using a fully depleted MOSFET. The area of the MOSFET is large so it can be described with a one-dimensional model and two-dimensional effects can be ignored. Drain and source are tied together and high-frequency capacitance is measured between the gate and the source/drain with different back-gate voltages  $V_{BG}$  applied. With back-gate voltage  $V_{BG} = 0 \text{ V}$  and high positive front-gate voltage  $V_{GDS}$ , an inversion layer is formed at the front channel, and gate oxide capacitance  $C_{OX}$  plus parasitic capacitance  $C_{PARA}$  such as gate-to-source/drain overlap capacitance is measured as  $C_{MAX}$  in Fig. 2. When  $V_{GDS}$  is much smaller than front-channel threshold voltage, there is no inversion layer in the channel region; the only capacitance measured is the parasitic capacitance  $C_{PARA}$  as shown in Fig. 2. From  $C_{MAX} - C_{PARA}$ , gate oxide thickness  $T_{OX}$  can be found. Buried oxide thickness can be found in a similar way by measuring the back-gate capacitance.

With back-gate voltage  $V_{BG}$  (e.g., 75 V) much higher than the back threshold voltage ( $\sim 30 \text{ V}$ ), an inversion layer is formed at the back channel. At high positive front-gate voltage  $V_{GDS}$ , an inversion layer exists on the front channel. The capacitance is  $C_{MAX}$  as shown in Fig. 2. However, when  $V_{GDS}$  is more negative than the back-gate threshold voltage, the whole thin silicon film is depleted, and an  $n^+$  inversion layer exists at the back channel, i.e., the bottom of the thin silicon film. The depleted silicon film behaves as dielectric. The measured capacitance is between the front-gate electrode and the back-channel inversion layer, which is shorted to the source/drain. The measured capacitance  $C_{MIN}$  is a series combination of the gate oxide capacitance and the depleted Si film capacitance  $C_{Si}$ . From  $C_{OX}$  and  $C_{MIN}$ , we can calculate  $C_{Si}$  and hence the Si film thickness  $T_{Si}$ :

$$C_{OX} = C_{MAX} - C_{PARA} \quad (1)$$

$$\frac{1}{C_{MIN} - C_{PARA}} = \frac{1}{C_{OX}} + \frac{1}{C_{Si}} \quad (2)$$

$$C_{Si} = \frac{\epsilon_{Si}}{T_{Si}} WL \quad (3)$$

$$T_{Si} = \epsilon_{Si} WL \frac{C_{MAX} - C_{MIN}}{(C_{MAX} - C_{PARA})(C_{MIN} - C_{PARA})} \quad (4)$$

where  $\epsilon_{Si}$  is the dielectric constant for silicon, and  $W$  and  $L$

Manuscript received March 20, 1991; revised June 4, 1991. This work was supported by SRC and AFOSR/JSEP under Contract F49620-87-C-0041. J. Chen, P.-K. Ko, and C. Hu are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720.

R. Solomon is with Intel Corporation, Santa Clara, CA 94050.

T.-Y. Chan is with Cypress Semiconductor, San Jose, CA 95134.

IEEE Log Number 9102249.

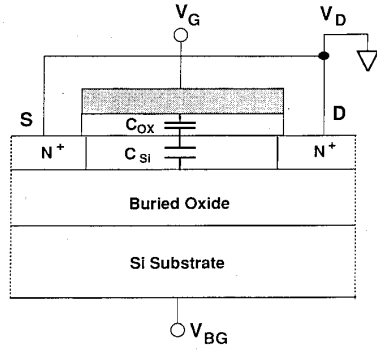


Fig. 1. Schematic of the HF  $CV$  measurement setup for SOI MOSFET. Capacitance is measured between gate and source/drain at two different back-gate biases. From the difference of those two, SOI film thickness  $T_{Si}$  can be found.

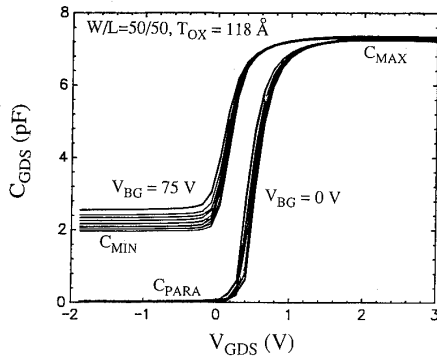


Fig. 2.  $CV$  measurement results at 12 locations across a SIMOX wafer. The spread in  $C_{MIN}$  reflects the thickness nonuniformity of the silicon film thickness.

are the device channel width and length, respectively. This technique is limited to silicon film thickness less than  $2X_{D_{MAX}}$ , where  $X_{D_{MAX}}$  is the maximum depletion layer width in the silicon. This is because the film has to be fully depleted. The limitation should be acceptable as the  $T_{Si}$  of the greatest interest is less than  $X_{D_{MAX}}$ , i.e., the "fully depleted" SOI devices [1]. Because it is high-frequency  $CV$ , interface states do not respond and hence do not affect the accuracy of this technique. The inversion-layer capacitance is not considered, but it has insignificant effects at strong inversion condition as shown by Liang *et al.* in [6]. Also, the correction is consistent for all the measurements, therefore the measured relative thicknesses among devices are the same.

### III. RESULTS AND DISCUSSIONS

In order to verify this method, cross-sectional transmission electron microscopy (XTEM) pictures were taken. One of these is shown in Fig. 3. From the cross section of a MOSFET on SIMOX wafer, 830 Å for the silicon film and 3600 Å for the buried oxide were measured. Table I shows the SOI film thickness measurement results using the  $CV$  technique compared with TEM results on three SOI wafers. The TEM thicknesses are for one spot on the wafer, while the  $CV$  thicknesses are average values of a few points on that

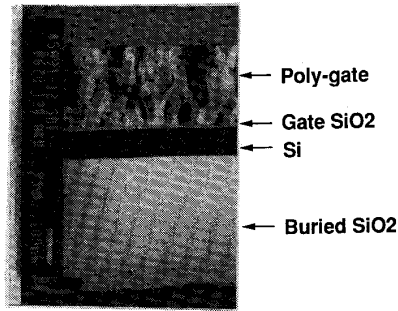


Fig. 3. Cross-sectional TEM picture of a MOSFET on SIMOX wafer. The gate oxide and the silicon film thicknesses are 118 and 800 Å.

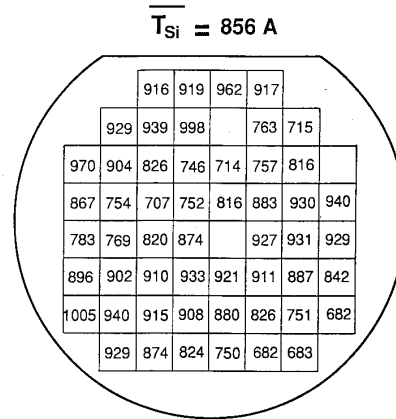


Fig. 4. SIMOX wafer silicon film thickness mapping obtained by using the  $CV$  technique on finished wafer.

TABLE I  
SILICON THICKNESS: TEM VERSUS  $CV$

Wafer	TEM	$CV$
SOI #9	1290 Å	1240 Å
SOI #12	830 Å	740 Å
SOI #16	830 Å	750 Å

part of the wafer. Higher TEM thicknesses are expected because the cross section may not be exactly normal to the wafer.

SOI film thickness uniformity across a wafer has been a major concern to manufacturers as well as to users of SIMOX wafers. Fig. 2 shows the high-frequency  $CV$  measurement result at 12 different locations across a SIMOX wafer using the above technique. The spread in  $C_{MIN}$  reflects the thickness nonuniformity of the Si film. The fact that the  $C_{MAX}$  are the same indicates that the gate oxide thickness is uniform across the wafer. Also it can be seen in the group of  $CV$  curves that the threshold voltage spreads where the capacitance value falls due to Si film thickness variation. The larger  $C_{MIN}$  corresponds to thinner Si film thickness, which also leads to lower threshold voltage as confirmed by Fig. 3.

Fig. 4 shows the SOI film thickness across the same SIMOX wafer with 50 points. The measurement time required for each point is less than 1 min. The silicon film

thickness varies from 680 to 1005 Å. This agrees with the  $\pm 150$ -Å specification provided by IBIS, the manufacturer of those SIMOX wafers, quite well. The same measurement was also performed on the p-channel SOI MOSFET and the same thickness and thickness variation were obtained. This further supports the validity of this method.

#### IV. SUMMARY

Thinner SOI film thickness is required for improvements in short-channel effects and elimination of the current kinks in SOI MOSFET's. Nonuniformity in SOI film thickness can result in nonuniformities in those characteristics and the threshold voltage. In this paper, a simple *CV* technique for measuring SOI film thickness across the finished wafers was developed. Using this technique, SOI film thickness mapping

was done on a SIMOX wafer which shows a thickness variation of  $\pm 150$  Å.

#### REFERENCES

- [1] J.-P. Colinge, "Reduction of kink effect in thin-film SOI MOSFET's," *IEEE Electron Device Lett.*, vol. 9, no. 2, p. 97, 1988.
- [2] J. Whitfield and S. Thomas, "An electrical method to measure SOI film thickness," *IEEE Electron Device Lett.*, vol. EDL-7, no. 6, p. 347, 1986.
- [3] D.-P. Vu, private communication.
- [4] M. Hoand and M. Tack, "Rapid electrical measurements of back oxide and silicon film thickness in an SOI CMOS process," *IEEE Trans. Electron Devices*, vol. 38, no. 3, p. 647, 1991.
- [5] F. Assaderahhi *et al.*, "Transient behavior of subthreshold characteristics of fully depleted SOI MOSFET's," submitted to *IEEE Electron Device Lett.*
- [6] M.-S. Liang, J. Y. Choi, P.-K. Ko, and C. Hu, "Inversion-layer capacitance and mobility of very thin gate-oxide MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-33, no. 3, p. 409, 1984.