The Effects of Furnace N2O Annealing on MOSFETs

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***Abstract*—MOSFETs with 70-110Å thick furnace N2O-annealed gate oxides are examined at both room and liquid nitrogen temperatures. The N2O anneal not only improves device performance, e.g. by increasing the high normal field mobility and current drivability, but it also suppresses degradation induced by Fowler-Nordheim and channel hot-carrier injection. Random telegraph noise measurements reveal a possible correlation between the interface properties and the mobility.**

I. INTRODUCTION

Thermal nitridation of conventional oxides in a nitrogen rich ambient, most notably NH_3 and N_2O, has been shown to improve many properties of the oxide films [1]-[3]. N_2O nitridation, in particular, is appealing because of the absence of deleterious hydrogen which has been correlated with electron trapping and because the films requires no reoxidation [2]-[4]. It has been reported previously [2]-[4] that a post-oxidation N_2O anneal (two-step process) is more promising than direct oxynitride growth in N_2O (one-step process) because the self-limiting nature of the direct oxynitride growth limits the film thicknesses to about 40Å unless rapid thermal processing (RTP) techniques are used [5]. The two-step process, however, allows the fabrication of much thicker nitrided oxide films. In this work, we report the characteristics of nMOSFETs with 70-110 Å N_2O-annealed gate oxides.

II. DEVICE PREPARATION

The nMOSFETs used in this work were fabricated on 15-30 Ω·cm p-Si (100) wafers using a four mask self-aligned poly-Si process. A boron channel implant was used to adjust the threshold voltage to around 0.7 V. The initial gate oxides were grown at 850°C in dry O_2 and then annealed at atmospheric pressure in N_2O at 900 or 950°C for 5-40 minutes. To achieve better uniformity than that allowed by RTP, both the oxidation and anneal steps were performed in a conventional furnace. The control oxides received a 20 minute N_2 anneal at the oxidation temperature. Following the gate oxidation, in situ phosphorous doped poly-Si was deposited and patterned using a photoresist ashing technique by which deep submicron dimensions could be acheived. After the contact pad definition, a 20 min forming gas anneal at 400°C completed the fabrication process.

III. RESULTS AND DISCUSSION

a. Composition and Kinetics

Typical compositional profiles of N, O, and Si in the gate oxides determined by Auger electron spectroscopy (AES) are shown in Fig. 1. A nitrogen pile-up at the oxide-substrate interface can be seen for all the N_2O-annealed oxides. Depending on the annealing time, temperature and initial oxide thickness, the interfacial nitrogen concentration varies from 0.8 to 4 at%. No nitrogen pile up is observed at the oxide surface.

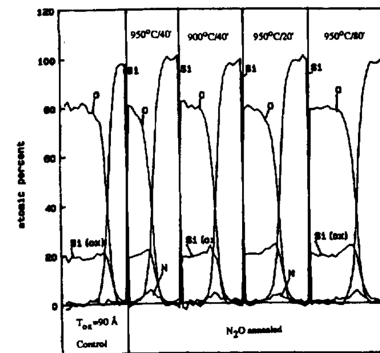

Fig. 1 Typical depth compositional profiles for control and N_2O-annealed oxides. Note that for all 4 N_2O-annealed oxides, nitrogen pile up can be observed at the oxide-Si interface where the oxygen concentration is about half of their bulk value.

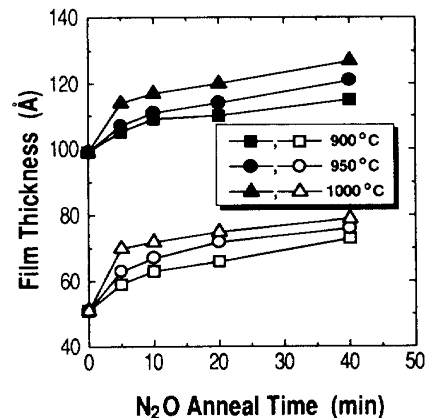

Fig. 2 Film thickness increase versus anneal time for 50Å (open markers) and 100Å (solid markers) oxides annealed in N_2O at different temperatures.

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The growth kinetics of the one-step N_2O oxynitride film growth have been shown to be self limiting [5]. Similarly, the thickness increase of conventional oxides induced by N_2O annealing is relatively insensitive to the anneal time (Fig. 2). Comparing the growth rate at different temperatures, one finds that increasing the anneal temperature only increases the initial growth rate; the subsequent growth rate for all temperatures studied is hardly changed. In addition, the thickness increase induced by annealing is only a weak function of the initial oxide thickness. These findings suggest that the kinetics of the N_2O-anneal, while initially reaction controlled, are dominated by the oxidant diffusion through the nitrogen rich layer at the interface.

b. Device Performance

The normalized linear transconductance G_m/C_{ox} of devices with different anneal conditions is shown in Fig. 3 as a function of the gate drive V_G-V_{TH}. At larger gate drives, e.g., V_G-V_{TH} = 4V, most of the N_2O-annealed devices show a 45 % increase in G_m, though their peak G_m is degraded by 5-10 %. This G_m cross-over is directly correlated with similar characteristics of the channel effective electron mobility μ_{eff} which is plotted as a function of the effective field in Fig. 4. The improvement in the high-field μ_{eff} for N_2O-annealed devices is enhanced at low temperatures while the field dependencies of μ_{eff} are hardly changed. It is also important to notice that the low field mobility degradation observed in the N_2O-annealed devices is substantially reduced at low temperatures. This is unlike NH_3-nitrided devices in which *enhanced* peak low field mobility degradation is observed at low temperatures [1]. For the anneal conditions examined here, the high-field mobility enhancement is only a weak function of the anneal time and temperature while the peak mobility degradation increases with increasing anneal time and temperature.

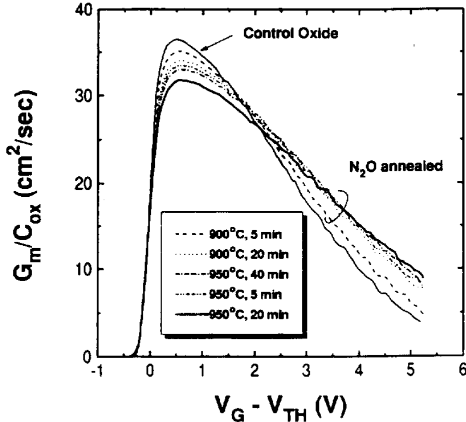

Fig. 3 The effects of N_2O annealing on the linear transconductance. The channel doping concentration is about $2x10^{17}cm^{-3}$ ($V_{TH} \approx 0.75$ V) and the oxide thickness is about 110Å. V_{DS} in this measurement is 50 mV and W_{eff}/L_{eff} = 29.5 μm/19.4 μm.

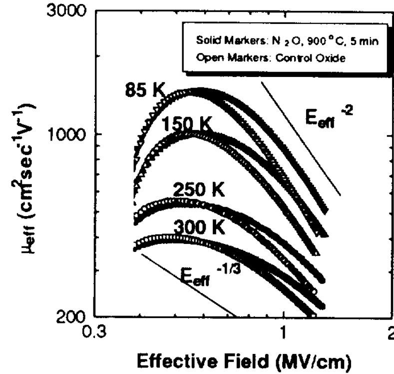

Fig. 4 The effective electron mobility versus effective field E_{eff} for MOSFETs with control and N_2O-annealed gate oxides. E_{eff} is calculated from $E_{eff}=(0.5Q_n+Q_B)/\varepsilon_{si}$ where the mobile charge Q_n is obtained by integrating the gate to channel capacitance against the gate voltage. The device parameters are $N_{sub}=3.3x10^{17}cm^{-3}$, T_{ox}=70 Å, and W_{eff}/L_{eff}=29.5 μm/19.4 μm.

Due to the increase in high-field mobility, N_2O-annealed devices show an increased current drivability (Fig. 5). Typically, the saturation drain current will increase by 15% at 300 K to 30% at 85 K when E_{eff} > 0.8 MV/cm.

The high-field mobility increase induced by thermal nitridation has long been thought to be due to the nitrogen incorporation at the oxide-silicon interface which modifies such interface properties as the surface potential roughness and interface trap density [1], or the interfacial strain [7]. However, under the condition of strong inversion at which the mobility increase occurs, most available techniques (*C-V*, charge pumping, etc.) are not applicable. In this work, we use Random Telegraph Signal (RTS) measurements [8] to study the interface property modification induced by the N_2O anneal. RTS fluctuations in the drain current of small-area MOSFETs arise due to the charge influence of single oxide interface traps. Typical RTS drain current fluctuations observed for devices with W_{eff}/L_{eff} = 0.5μm/0.4μm are

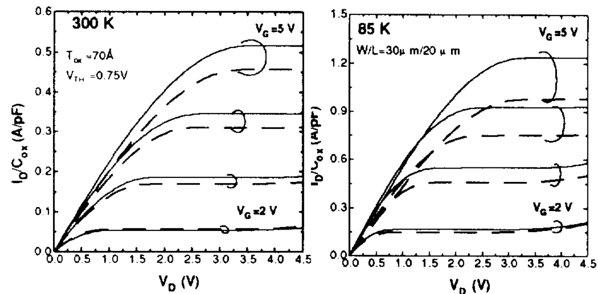

Fig. 5 Comparison of the output characteristics for control (dashed lines) and N_2O-annealed (solid lines) devices operated at 300K and 85K. To eliminate the minor difference in thickness, I_D has been normalized by the oxide capacitance.

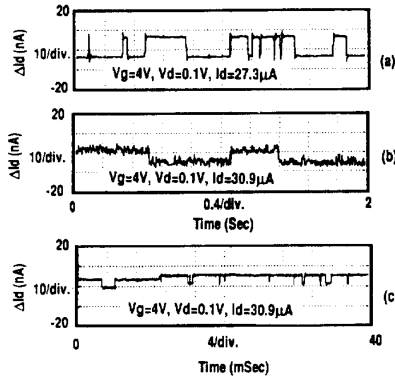

Fig.6 Typical random telegraph signals measured in deep-submicrometer MOSFETs with (a) control and (b) N2O-annealed gate oxides. Shown in (c) are the small RTS fluctuations of (b) measured on a finer time scale.

shown in Fig. 6. For n-channel devices these drain current fluctuations have been shown to be the result of single empty (current high) or filled (current low) interface traps [8]. It can be seen that an N_2O anneal significantly changes the ratio of trap-empty time to trap-filled time. Also, a weaker RTS with a much shorter time constant is induced by the anneal and superimposed on the stronger RTS. This suggests that an N_2O anneal not only affects the capture and emission times of the interface traps but also introduces new interface traps which have little effect on μ_{eff} because of their large empty to fill time ratio (Fig. 6c).

The scattering coefficient α extracted from RTS measurements is shown in Fig. 7. Interestingly, as the gate voltage increases, α of N_2O-annealed devices crosses over that of the control oxide. This observation is qualitatively in agreement with the mobility measurements. We therefore attribute the increase in the high-field mobility to less efficient interface trap scattering resulting from the increased trapping distance from the interface (Fig. 8).

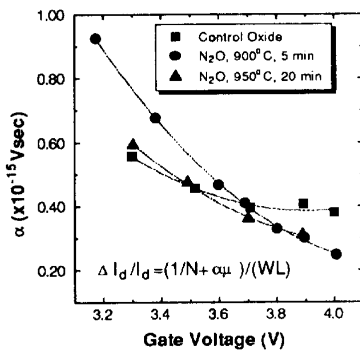

Fig. 7 The extracted scattering coefficient α $[=(1/\mu - 1/\mu_o)/N_t]$ versus gate voltage for control and N2O-annealed devices. The drain current fluctuation ΔId is correlated with α through the formulation shown in the inset [8].

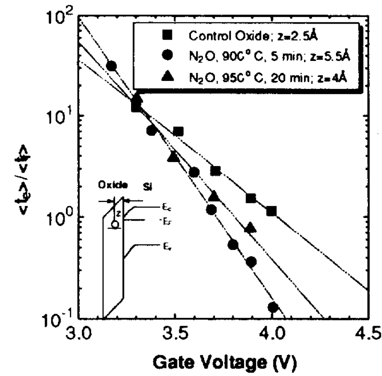

Fig. 8 The ratio of the average interfacial "trap-empty" time <te> to the average interfacial "trap-filled" time <tf> versus gate voltage,. The slope of the plot log[<te>/<tf>] versus gate voltage is proportional to the distance of the trap from the interface, z, as illustrated in the inset.

c. Device Reliability

Device reliability was examined under FN and channel hot-carrier injections. As shown in Fig. 9, although the lifetime under FN injection increases with N_2O anneal, the field acceleration factor (impact ionization coefficient) remains unchanged. The lifetime increase is further enhanced at high stress frequencies. The lifetime increase induced by N_2O annealing shown in Fig. 10 is a factor of ten at the stress frequency of 1 MHz while under DC stressing it is only a factor of 2-3. This lifetime increase can be explained by a reduction in the hole trapping and hole mobility in the annealed oxide [9].

DC channel hot-carrier injection was performed at the two worst-case stress conditions of peak I_{SUB} ($V_G = 0.425V_D$) and peak I_G ($V_G = 1.25V_D$) stressing. Shown in Fig. 11 is the linear transconductance degradation ΔG_m under peak I_{SUB} injection. A reduction in device degradation is

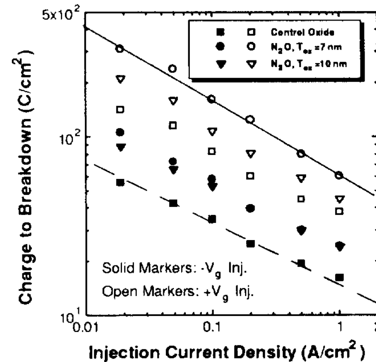

Fig. 9 Charge to breakdown versus injection current density for control and N2O-annealed oxides. The similar slope indicates that the anneal does not change the field acceleration factor, or the impact ionization coefficient, though the lifetime of the N2O-annealed oxides is longer.

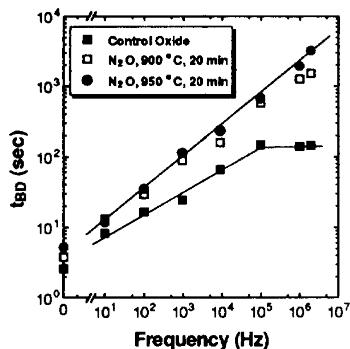

Fig. 10 Time-to-breakdown (tBD) under bipolar square-wave voltage stressing plotted against the stressing frequency. T_{ox}=70Å, E_{ox}≈12.5 MV/cm.

observed for all N_2O-annealed devices. Charge pumping measurements (not shown) indicate that this suppressed G_m degradation is due to an improvement in the interfacial hardness. The interface hardness improves with increasing anneal time and temperature.

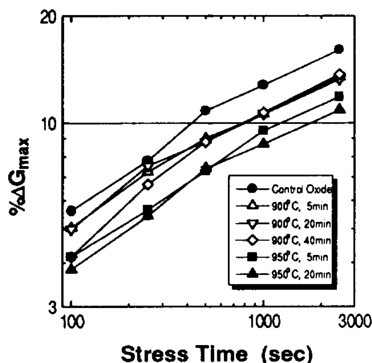

Fig. 11 The degradation in the maximum linear transconductance resulting from channel hot electron stressing. The stress condition is V_G ≈V_D/2 with the stress drain voltages chosen to match an initial substrate current level. The oxide thicknesses are ≈70Å and W_{eff}/L_{eff} = 6.5 µm/0.3 µm.

It has been shown that N_2O annealing reduces both electron and hole trapping under F-N injection [4]. Thus, the threshold voltage shift ΔV_t for MOSFETs stressed at peak I_G as shown as a function of the stress time in Fig. 12 is reduced for the N_2O devices. Although enhanced electron trapping is frequently observed for NH_3 annealed devices [1], [7], no enhanced electron trapping is observed for the N_2O annealed devices examined here. Furthermore, F-N injection results indicate that electron trapping monotonically decreases with increasing anneal time and temperature while subsequent re-oxidation does not further reduce electron trapping [4]. We therefore conclude that the incorporation of nitrogen alone does not introduce new bulk electron traps.

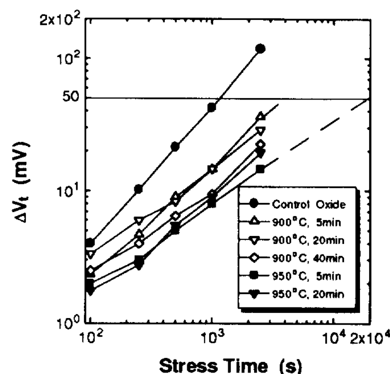

Fig. 12 Shifts in the extrapolated threshold voltage versus stress time under high V_G channel hot electron injection (V_G=1.25V_D). The stress drain voltages were chosen to match initial stress gate current levels. The device dimensions were the same as those in Fig.11.

The hydrogen present in NH_3-nitrided oxides should be responsible for the inherent high trap density in these films.

IV. Summary

Though a simple and flexible process, N_2O annealing has been shown to improve device performance and hot carrier immunity. RTS measurements indicate that the anneal-induced interface modification is responsible for the increase in high-field mobility.

Acknowledgment

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