DESIGN GUIDELINES FOR DEEP-SUBMICROMETER MOSFETS

M.-C. Jeng, J. Chung, J.E. Moon, G. May, P.K. Ko, and C. Hu

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA 94720

ABSTRACT

A comprehensive study of the performance and reliability constraints on the dimensions and power supply of deep-submicrometer non-LDD n-channel MOSFETs is presented. Design guidelines, extracted from experimental results, are presented based on the following considerations: short-channel and drain-induced-barrier-lowering effects, off-state leakage currents, hot-electron reliability, time-dependent dielectric breakdown, current-driving capability, voltage gain, and switching speed. The relative importance of each mechanism for a given technology and design criteria is compared. As an example, a set of design curves, using a set of typical performance and reliability criteria, is provided for n-channel deep-submicrometer devices. With slight modifications, these design curves can also be extended to other technologies, including p-channel and LDD devices.

INTRODUCTION

Although it is well known that circuit performance can be enhanced by scaling down device dimensions, in the deep submicrometer regime the different trade-offs between reducing oxide thickness, channel length, and power supply are still not clear. For longer-channel devices, previous studies [1-3] have proposed design guidelines based mainly on the threshold voltage shift due to short-channel effects, subthreshold current, and hot-electron reliability considerations. This paper attempts to provide comprehensive design guidelines for MOSFETs in the deep-submicrometer regime by investigating a wide range of performance and reliability constraints on device dimensions and power supply. The mechanisms examined in this study are: short-channel and drain-induced-barrier-lowering (DIBL) effects, the punchthrough and gate-induced drain leakage (GIDL) [4] currents, hot-electron reliability, time-dependent dielectric breakdown, current-driving capability, voltage gain, and switching speed. Using this set of performance and reliability constraints, design curves are developed based on measurements of n-channel deep-submicrometer devices. The relative importance of each mechanism is compared.

The deep-submicrometer devices used in this study were fabricated using a photoresist-ashing technique [5]. The oxide thicknesses range from 3.6nm to 15.6nm. Substrate doping concentrations have been adjusted such that threshold voltages for long-channel devices are around 0.65V. In this study, the junction depth is fixed to about 0.2μm.

DEVICE LIMITATIONS

Threshold Voltage Shift: Fig. 1a and 1b show the threshold voltage shift due to short-channel and DIBL effects as a function of the channel length. The threshold voltage shift is defined as the difference between the measured threshold voltage at a given drain voltage and its corresponding long-channel value at a drain voltage of 50mV (V_{T0}). The straight lines of the data reveal that the functional form of the experimental results agrees with existing threshold-voltage models [6]. The dashed lines in Fig. 1-6 demarcate the performance and reliability (Table 1) criteria used in this paper to obtain the design curves (Fig. 7-9); the arrows indicate the acceptable regions.

Off-State Leakage Current: As shown in the insert of Fig. 2, off-state leakage current is composed of two main components: punchthrough current (I_{PT}) and gate-induced drain leakage current (I_{GIDL}). In Fig. 2, the off-state leakage current is measured at V_{T0} - 0.6V for various device dimensions and drain voltages. A gate bias of V_{T0} - 0.6V is used to eliminate any effect caused by the variations in threshold voltage between different oxide thicknesses. The punchthrough current dominated regions are indicated by open symbols; the GIDL current dominated regions are indicated by closed symbols. The current level of the experimental data is clamped at a lower bound of 0.5pA/μm due to limits in the measurement resolution.

Hot-Electron Reliability: Fig. 3 displays the extrapolated maximum allowable power supply voltage to ensure a 10-year device lifetime [7] (corresponding to a 10% reduction of the drain current in the triode region) as a function of channel length for different oxide thicknesses. For a given substrate current, thinner oxide devices exhibit less degradation than those with thicker oxides [8]. However, for a given drain bias, thinner gate oxide devices also exhibit greater peak substrate current than those with thicker oxides [9]. These two counteracting trends explain why 8.6nm gate oxide devices show a slightly smaller minimum channel length than those of 5.6nm and 15.6nm gate oxides devices at a power supply of 3V.

Time-Dependent Dielectric Breakdown Based on a defect-density model, a technique to predict oxide breakdown statistics has been developed [11]. Because oxide quality is a sensitive function of the device fabrication process, the oxide reliability results used in this study should be viewed as a rough approximation only. Other fabrication technologies can yield a higher quality oxide with a lower defect-density than is observed in this study (1.0 cm^{-2}). Listed in Table 1 is the oxide reliability criterion used in Fig. 7-9.

PERFORMANCE CONSTRAINTS

Current-Driving Capability: In Fig. 4, the drain saturation current measured at V_{GS} = 3V is plotted versus channel length for different oxide thicknesses. As expected, the current-driving capability for a given gate oxide increases as the channel length decreases. However, because of mobility degradation due to high vertical fields, the current-driving capability tends to saturate at very thin gate oxides. The high channel doping concentration required to achieve the required threshold voltage for thin oxide devices also degrades carrier mobility.

Voltage Gain: In Fig. 5, the peak voltage gain (solid lines)

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and the gain measured at $V_{GS} - V_T$ = 0.3V (alternated lines) is plotted for various device dimensions. The voltage gain is defined as $g_m R_{out}$, where g_m is the measured transconductance and R_{out} is the output resistance. Since both g_m and R_{out} are higher for thinner gate oxide devices, the gain increases as oxide thickness decreases. The sharp decrease of the gain at very short channel lengths is caused by bulk punchthrough which significantly reduces R_{out}.

Switching Speed: In Fig. 6, the simulated delay time [11] of an 11-stage CMOS ring oscillator with a 0.1pF load capacitor on each stage is presented for different oxide thicknesses, channel lengths, and power supplies. The channel width is 15μm for n-channel and 30μm for p-channel devices. As oxide thickness decreases, the gate capacitance eventually becomes larger than the load capacitance. However, the capacitance charging rate (proportional to the current-driving capability) does not increase as rapidly as the gate capacitance due to mobility degradation (Fig. 4). These two mechanisms explain why the delay time does not continue to decrease with diminishing oxide thickness.

DESIGN GUIDELINES

Based on the experimental results presented in the last section, various design curves can be developed. Since oxide thickness, channel length, and supply voltage are the main design parameters, three types of design curves are provided for maximum flexibility (Fig. 7-9). Each curve fixes one parameter while varying the other two. The intersection of these performance and reliability curves (shaded area) indicates the region of allowable device dimensions and/or power supply for both digital and analog applications. Table 1. summarizes the meanings of the symbols and lists the performance and reliability criteria used.

DISCUSSION

Oxide Thickness vs. Channel Length: Fig. 7 shows design curves where oxide thickness is plotted versus channel length for a power supply of 3V. At this supply voltage, the lower bound of the oxide thickness is limited to 5.6nm by GIDL current rather than by oxide breakdown. For digital applications, depending upon the oxide thickness, the minimum channel length is determined by either the threshold voltage shift or by the hot-electron reliability criterion; the minimum device size is found to be T_{ox} = 7.8nm and L_{eff} = 0.26μm. For analog applications, the minimum channel length is limited by the voltage gain; the minimum device size is about T_{ox} = 6.3nm and L_{eff} = 0.31μm. The upper bound on device dimensions is determined by the speed (delay time) and current driving capability requirements.

Power Supply vs. Channel Length: Fig. 8 shows design curves where power supply is plotted versus channel length for an oxide thickness of 8.6nm. The maximum power supply voltage is limited by the hot-electron reliability while the minimum power supply voltage is limited by the current driving capability requirement. At a power supply of 3.3V, hot-electron reliability does not pose a problem to devices with channel length longer than 0.4 μm which implies that LDD devices may not be necessary. The minimum allowable channel lengths are 0.28μm and 0.36μm for digital and analog applications, respectively; these values are roughly independent of the power supply voltage.

Power Supply vs. Oxide Thickness: Fig. 9 shows design curves where power supply is plotted versus oxide thickness for an effective channel length of 0.3μm. For gate oxide thicknesses less than 5.6nm, the maximum supply voltage is determined by GIDL current; for gate oxide thicknesses greater than 5.6nm, hot-electron reliability is the limiting mechanism. The minimum power supply is determined by the speed requirement. For L_{eff} = 0.3μm, the minimum oxide thickness is about 4.0nm at a supply voltage of 2V.

Junction Depth: Although the junction depth has been fixed at 0.2μm in this study, with slight modifications, the design curves in Fig. 7-9 can be extended to other junction depths. For example, if the junction depth is decreased, short-channel and DIBL effects and punchthrough currents would diminish. However, hot-electron reliability would degrade due to the increase in the lateral electric field.

Other Technologies: The design curves in Fig. 7-9 can also be extended to any technology, including p−channel and LDD devices. For example, with LDD devices, short channel, DIBL, and GIDL effects would be less severe and the hot-electron lifetime would be longer. However, current-driving capability and gain would decrease due to the increase in source/drain resistance.

CONCLUSION

Design guidelines for deep-submicron MOSFETs are presented based on various performance and reliability constraints. Three types of design curves are constructed to obtain a design window for a given set of design requirements. For next generation ULSI systems, the device dimensions and power supply can be determined and the relative importance of each mechanism affecting the device design can be identified.

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TABLE I

Symbol	Description	Criterion
ΔV_T	Threshold voltage shift	≤ 0.1V
I_{PT}	Punchthrough current at V_{T0} - 0.6V	≤ 10pA/μm
G	Voltage Gain at $V_{GS} - V_T$ = 0.3V	≥ 80
I_{GIDL}	Gate-induced-drain-leakage current	≤ 10pA/μm
τ_l	Lifetime (10% I_{DS} degradation)	≥ 10 years
τ_d	delay time	≤ 120ps/stage
I_{DSAT}	Drain saturation current at V_{GS} = 3V	≥ 0.5mA/μm
TDDB	Time Dependent Dielectric Breakdown on $5mm^2$ area for 10 years	≤ 5%

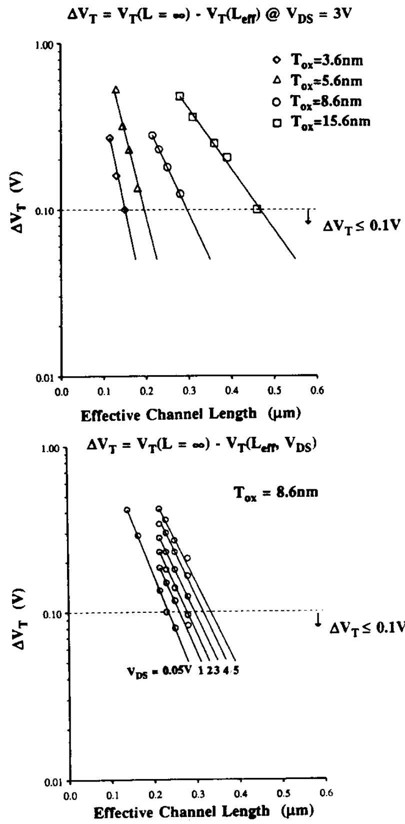


Fig. 1 The threshold voltage shift as a function of the channel length. (a) measured at V_{DS} = 3V for different oxide thicknesses, (b) measured at different drain voltages for T_{ox} = 8.6nm. The dashed lines are used to obtain the design curves.

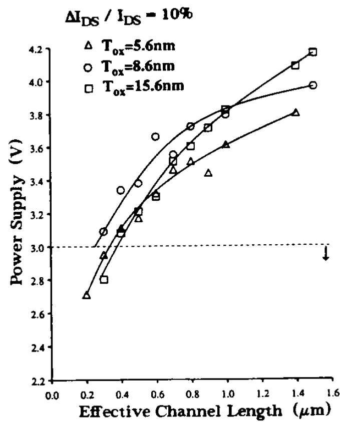


Fig. 3 The maximum allowable power supply to ensure 10 years device lifetime.

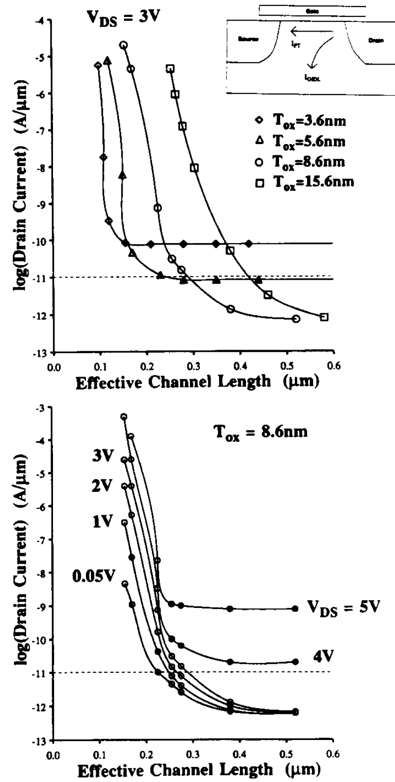


Fig. 2 The drain current at $V_{GS}=V_{T0}-0.6V$. Punchthrough current dominated regions are indicated by open symbols and gate-induced drain leakage current dominated regions are indicated by closed symbols. (a) measured at V_{DS} = 3V for different oxide thicknesses, the insert shows the current paths of the two current components, (b) measured at different drain voltages for T_{ox} = 8.6nm.

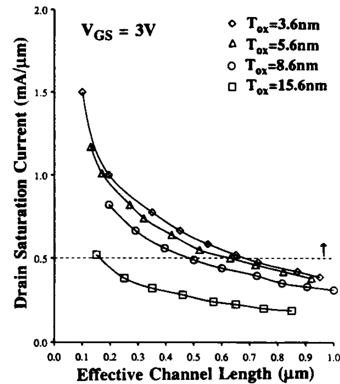


Fig. 4 The drain saturation current measured at V_{GS} = 3V.

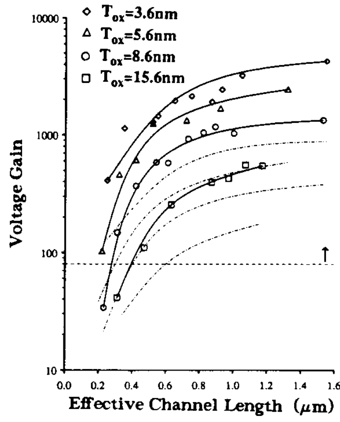
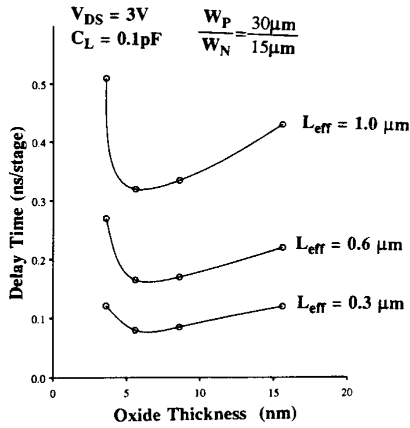


Fig. 5 The voltage gain as a function of the channel length for different oxide thicknesses. The solid lines are the peak voltage gain. The alternated lines are the gain measured at $V_{GS}-V_T$ = 0.3V. Only the data for the peak gain are shown.



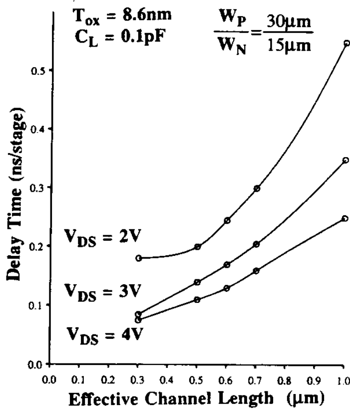


Fig. 6 The simulated delay time of 11-stage ring oscillators. The load capacitance is 0.1pF for each stage. (a) V_{DS} = 3V for different oxide thicknesses and channel lengths, (b) T_{ox} = 8.6nm for different power supply and channel lengths.

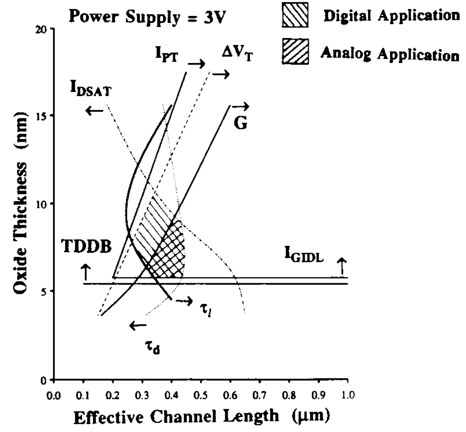


Fig. 7 The design curves for power supply of 3V. The arrows indicate acceptable regions. Each line is the contour of different criterion listed in Table1.

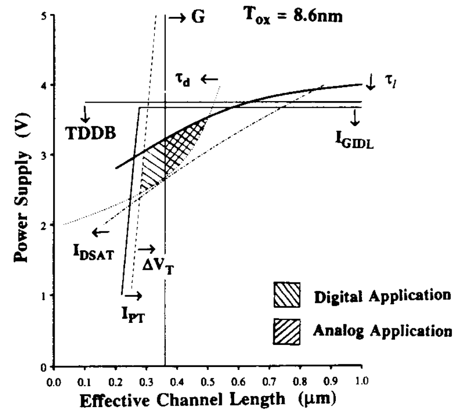


Fig. 8 The design curves for 8.6nm gate oxide devices. The arrows indicate acceptable regions. Each line is the contour of different criterion listed in Table1.

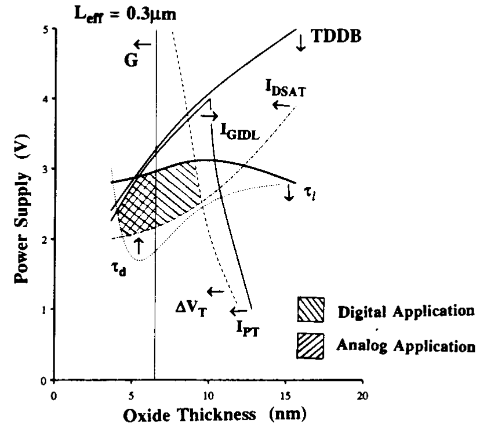


Fig. 9 The design curves for L = 0.3μm devices. The arrows indicate acceptable regions. Each line is the contour of different criterion listed in Table1.