Stress-Induced Oxide Leakage

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Abstract—**Voltage-stress-induced leakage in 5-nm thermal oxides was studied. A correlation between the leakage current and the charge-pumping current was evident in a series of voltage stress, annealing, and restress tests. The close correlation suggests that the leakage may be a result of the oxide-trap-assisted tunneling.**

I. Introduction

The integrity and reliability of the dielectrics are of great importance in the ULSI technologies. It has been shown [1], [2] that the high field stress on thin gate oxides produces a leakage current (observable at low fields) which currently limits the scaling of EEPROM's [3], [4] and may limit oxide scaling in future VLSI technologies. The mechanism of this leakage current has been attributed to the generation of localized defects or weak spots [1], localized positive charges [2], and trap states near the injecting interface [5], [6]. In this study data supporting a model involving trap states are presented.

II. Experiments

NMOS transistors with 5.5-nm gate oxide and $W/L = 10$ μm/10 μm, fabricated using standard NMOS fabrication process [7], were used in this study. Transistors were subjected to systematic voltage ramp stress controlled by HP4140 and HP9836. The maximum voltage of the voltage ramp was increased successively from 6 to 7.6 V at which breakdown occurred. The $I-V$ characteristics were recorded during each voltage ramp stress. Since the thin oxide samples were in the form of MOSFET's rather than capacitors, we were able to use the sensitive charge-pump technique [8] to study the behavior of the $Si-SiO_2$ interface traps before and after stress. The source and drain of the transistor were grounded. The frequency of the pulse applied on the gate was 100 kHz, with 50-ns rise and fall times and 2-V peak-to-peak amplitude. The charge-pump current I_{cp} was measured at the substrate as a function of the dc offset voltage ($V_{g\text{-low}}$) of the pulse. The maximum charge-pump current I_{cp} is equal to $I_{cp(\max)} \propto qfD_{it}$, where q is the electron charge, f is the frequency of the applied pulse, and D_{it} is the number of interface traps [8]. Since only D_{it} is expected to be changed by voltage stress and low-temperature annealing, I_{cp} is a direct indicator of the interface trap density. This technique is well proven in the study of hot-carrier induced traps [9]. The annealing behavior and CV characteristics, the charge-pump current, and the oxide leakage current of the samples were also measured.

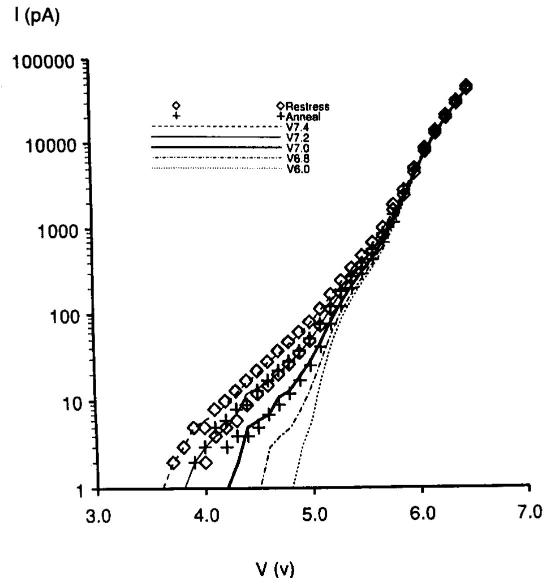

Fig. 1. I_g versus V_g in a series of successive voltage ramp stress, anneal, and restress.

III. Results and Discussion

Fig. 1 illustrates the $I-V$ characteristics following each voltage ramp stress and anneal. The waving nature of the curve is a consequence of the interference of tunneling electron waves [2] and is an indication of the high quality (flatness) of the interfaces. The first ramp ends at 6 V, the second ramp ends at 6.8 V, etc. The increase in the leakage current (at low fields) after each ramp stress is clearly visible. Fig. 2 shows the charge-pump current I_{cp} increasing after each voltage ramp indicating the increased interface trap density D_{it}. So far, the observation described is the same as previously reported. After the fifth ramp stress (to 7.4 V), the device was baked at 270°C for 30 min and for 1 h, and the $I-V$ and I_{cp} measurements were repeated. It was observed that the leakage current and I_{cp} decreased to their respective levels measured after the 7.2- and 7-V ramp steps. The device was then stressed to the maximum ramp voltages of 7.2 and 7.4 V and the $I-V$ and I_{cp} curves were again recorded. The results indicated that both I_{cp} and leakage current were identical to the data taken prior to the bake, as shown in Figs. 1 and 2.

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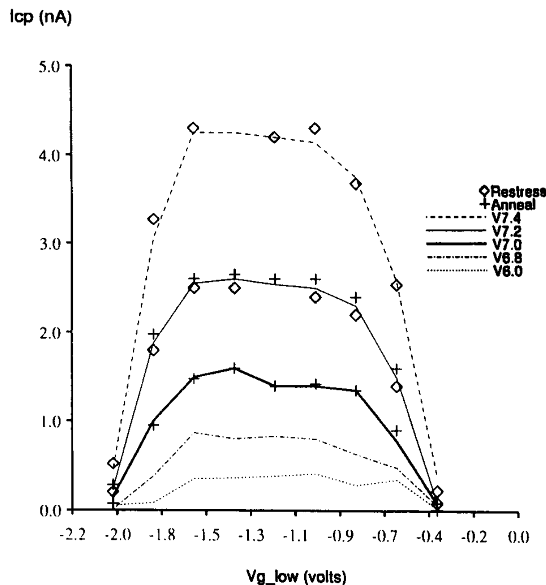

Fig. 2. Charge-pump current versus low gate voltage $V_{g\text{-low}}$. Lines indicate the charge-pump characteristics measured after the initial voltage ramp stresses to increasingly higher voltages. Measurements after anneal are shown with plus (+) marks. The charge-pump currents after restress are shown with diamond marks (△).

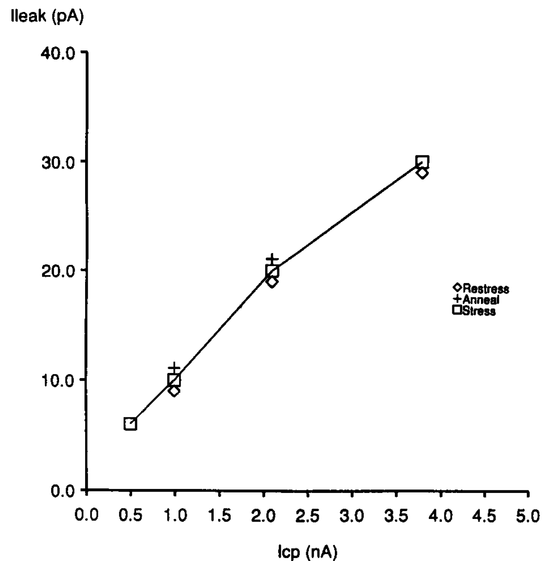

Fig. 3. Increase in the leakage current versus increase in the charge-pump current, after initial voltage ramp stress. Measurements after anneal and restress are shown with plus (+) and diamond marks (△), respectively.

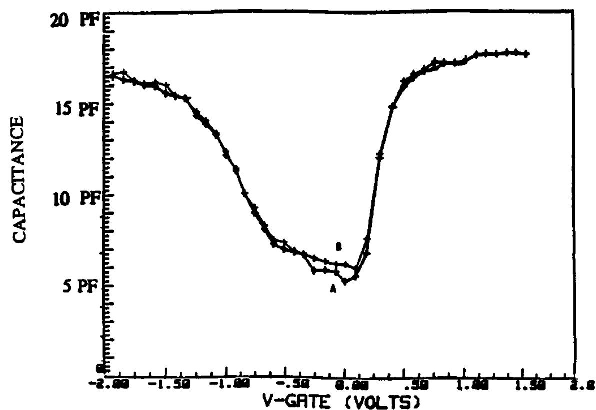

Fig. 4. Low-frequency CV measurements. A: before stress; B: after stress.

An apparent correlation between the leakage current and I_{cp} is quite evident, i.e., whenever the same I_{cp} was observed the same leakage current was also observed, no matter whether the leakage current (and I_{cp}) is the result of voltage stress or stress plus annealing or stress plus annealing plus restress. This correlation was quite reproducible from device to device. One may note that when different stress/annealing conditions produce the "same" leakage current, the "sameness" is observed at all voltages, i.e., the I-V curves are the same. Similarly, the I_{cp} versus $V_{g\text{-low}}$ characteristics (Fig. 2) are the same, suggesting the same energy distribution of D_{it} [8]. One may also note that 270°C anneal apparently annealed out interface states without leaving latent damages, in the sense that a subsequent 7.4-V ramp stress did not produce larger leakage and I_{cp} than the first 7.4-V ramp stress.

Fig. 3 shows that the increase in the leakage current versus the increase in the charge-pump current I_{cp} is roughly a linear function with a hint of sublinearity and that the measurements after the anneal and repeated voltage stress coincide on the same line. The decrease in the leakage current by bake and increase by voltage stress can be explained by the decrease and increase in the interface trap density due to annealing and stress. Although this correlation is not a proof of causality, it does strongly suggest a link between the leakage current and the traps. The mechanism linking the two may be trap-assisted direct tunneling [5]. Trap-assisted direct tunneling effectively decreases the barrier height for tunnel electrons. This fact can explain the observed apparent lower barrier height [1]. The thickness sensitivity of tunneling can also explain why leakage current is not observable in thicker oxide even with the same trap density—perhaps the most striking characteristic of the stress-induced leakage.

In principle, localized positive charges on the interface can also lower the tunneling barrier for electron injection and result in the leakage current [2], [10]. This alone, however, cannot explain the extremely strong thickness sensitivity of the stress-induced leakage current [4]. The quasi-static CV plot of Fig. 4 also shows the presence of interface states after voltage ramp stress to 7.2 V, and the absence of any uniform trapped charge which would have produced a lateral shift in addition to the shape change in the CV curve. The transistor I-V characteristics of the transistor before and after the stress (to 7.2 V) are shown in Fig. 5. From the subthreshold slopes the increase in the interface states can be seen, while the decrease in the mobility can be observed from the reduction in the drain current.

IV. Summary

The results may be summarized by noting that $I_{\text{leak}}(\text{V}) = A \cdot f(\text{V})$ and $D_{it}(\text{E}) = A \cdot g(\text{E})$, where A is determined by

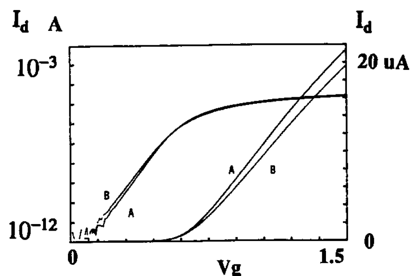

Fig. 5. Drain current versus gate voltage characteristics. *A*: before stress; *B*: after stress (to 7.2 V).

the stress and anneal history. The suggestion is that I_{leak} results from trap-assisted tunneling. Although I_{cp} only reflects the fast interface traps located close to the interface, one may speculate that oxide trap density farther away from the interface may also be proportional to A and also contribute to the oxide leakage.

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