IMPACT OF INTER-METAL-OXIDE DEPOSITION CONDITION ON NMOS & PMOS TRANSISTOR HOT CARRIER EFFECT

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Abstract

The hot carrier effect of NMOSFETs and PMOSFETs has been investigated for different inter-metal-oxide (IMO) deposition condition. It is found that the hot carrier effect lifetime of NMOSFETs using silane-based oxide deposition can be more than two orders of magnitude longer than that of NMOSFETs using tetraethylorthosilicate (TEOS) based deposition, while PMOSFETs exhibit more net electron trapping. TEOS IMO apparently increases the rate of hole trapping and hole-induced generation of bulk and interface traps. Si-rich oxide deposition condition improves the hot carrier lifetime, but does not overcome the deleterious effect of an additional TEOS oxide layer. IMO only influences the charge trapping properties of gate oxide/interface in the vicinity of the source-drain gate edges and therefore affects short channel devices more strongly.

I. Introduction

MOS device instability induced by the hot carrier effect has been widely studied during the last decade. Recently there is a strong interest on issues of hot-carrier-induced degradation caused by backend processing and structures. Hydrogen-rich plasma-deposited silicon nitride encapsulation was found to enhance interface trap generation [1]. Spin-on glass layer as a component of the inter-metal-oxide (IMO) was also reported to accelerate the degradation of the MOS transistor [2]. Plasma enhanced tetraethylorthosilicate (TEOS) has been widely used as a component of the IMO structure. Trichloroethane oxidation has been found to degrade the charge retention characteristics of EPROM interpoly oxide due to the presence of carbon [3]. However, the effect of TEOS IMO on the degradation of the MOS transistor has not been reported.

In this work the effect of oxide deposition condition is studied. Results indicate that the hot-carrier-induced degradation using silane based plasma enhanced oxide (OX) layers is much superior to that using plasma enhanced TEOS oxide layers. TEOS process apparently enhances hole trapping and results in bulk and interface trap generation.

II. Experiment

The MOS devices used for this investigation were fabricated on p-type 10 Ω-cm Si substrates with a twin-tub CMOS technology, whose features included lightly-doped-drain with a 0.3μm TEOS spacer and double-level metalization. A spin-on-glass (SOG) layer sandwiched by four different combinations of IMO layers were fabricated. The four combinations are listed in Table 1. The refractive indices were 1.47 for OX layer and 1.46 for TEOS layer. The silicon rich oxides were obtained by increasing the ratio of silane to oxygen flow rates and the refractive indices became 1.54 for OX and 1.48 for TEOS. Final encapsulation contained a 500nm oxide layer and a 700nm nitride layer. The gate oxide thickness was 200Å. The effective channel lengths (L_{eff}) ranged from 0.55 to 0.8 μm

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and the channel width was 20μm.

Devices were stressed at DC conditions. The hot-carrier-induced degradation was monitored for two parameters: linear drain current I_{dl} and threshold voltage V_t, where I_{dl} is measured at V_d=0.1V and V_g=5V. V_t is extrapolated from the curve of I_{dl} vs. gate bias V_g with V_d=0.1V.

III. Results and discussion

Fig. 1 shows extrapolated device lifetime due to hot-carrier-induced degradation versus effective channel lengths of tested devices. The devices with different effective channel lengths for each group of four different IMO layers were stressed at the same conditions of V_d=6.5V and V_g=1.8V, i.e., at the maximum substrate current. Failure criterion was 10% shift in the linear drain current at V_g=5V. Fig.1 shows that lifetime for devices containing OX IMO layers were about two orders of magnitude longer than those for devices containing TEOS IMO layers with the same L_{eff}. Furthermore lifetime for devices with Si rich OX layers, is about one order of magnitude longer than that for devices with OX layers. The beneficial effect of Si-rich oxide has been attributed to the blocking effect against hydrogen diffusion by dangling bonds in Si-rich OX layers [4]. But devices with two layers of Si-rich TEOS layers have shorter lifetime than single-layer TEOS oxide devices as shown in Fig. 1. The benefit of Si-rich TEOS, if any, is insufficient to overcome the deleterious effect of the additional TEOS oxide layer. For a given L_{eff}, the four groups of devices in Fig. 1 have about

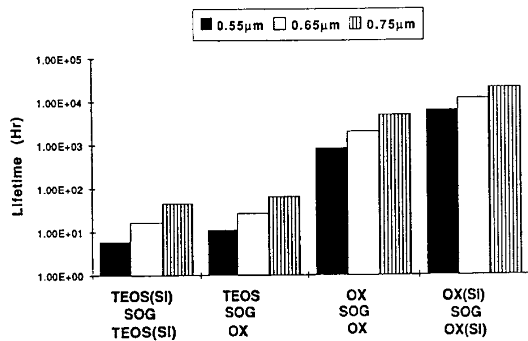

Fig.1 Lifetime versus effective channel lengths for four groups of NMOS devices with different IMO layers. Stressing biases V_d=6.5V and V_g=1.8V.

the same substrate current. All nominal values of lifetimes for 0.85μm devices extrapolated to V_d=5.5V and V_g=2.0V [5] are listed in the right column in Table 1. In this column, OX IMO clearly leads to longer lifetime than TEOS IMO. Also one layer of TEOS leads to longer lifetime than two layers of TEOS.

Fig. 2 shows examples of NMOSFETs degradation of linear current I_{dl} versus stressing time. All four NMOSFETs were stressed at V_d=7.5V and V_g=2.3V, i.e., at the maximum substrate current. Their effective channel lengths are 0.65μm. Fig.2 shows similar dynamics for all four samples and confirms the differences in lifetimes shown in Fig.1. Small but consistent differences in subthreshold swing were also observed in these samples.

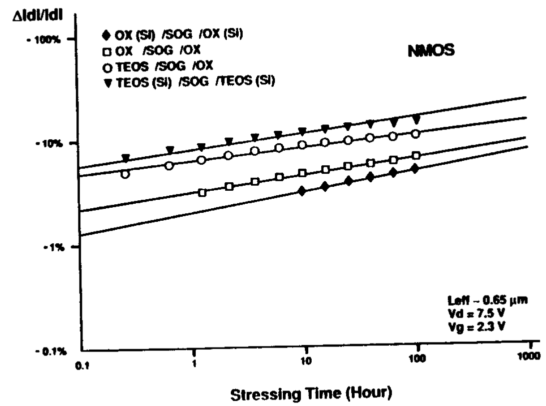

Fig.2 Linear drain current I_{dl} degradation versus stressing time for four NMOS devices with different IMO layers. Stressing biases V_d=7.5V and V_g=2.3V.

Fig. 3 shows V_t shift versus stressing time for the same four NMOSFETs. Here, significant differences are seen. Initially all V_t shifts are negative indicating that the hole trapping process dominates the V_t shift although interface traps are also being generated and are responsible for the decreases in I_{dl} shown in Fig. 2. After 10 hours of stressing a large positive V_t shift for devices containing TEOS oxide layer is observed suggesting the existence of a strong electron trapping process. Comparing Fig. 2 and Fig. 3, it is found that a device with a larger I_{dl} degradation also has a larger initial negative V_t shift rate, as well as a larger positive V_t shift later on. The correlation of the three suggests that the generation of interface traps, which is the main cause of the I_{dl} degradation, may be associated with the hole trapping process [6,7]. Bulk electron trap generation may also result from the presence of the hole traps [8].

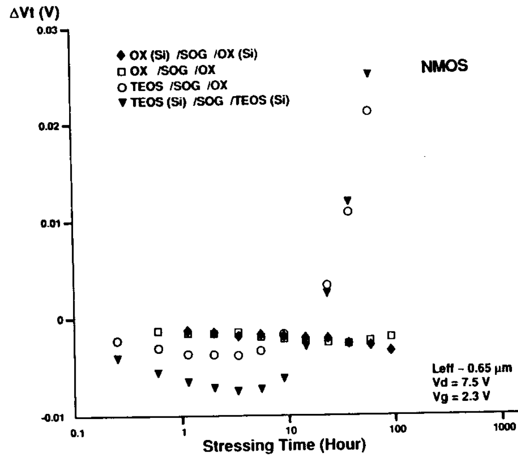

Fig.3 Threshold voltage V_t shift versus stressing time for four different NMOS devices with different IMO layers. Stressing biases V_d=7.5V and V_g=2.3V.

Fig.4 shows the change of I_{dl} vs. stressing time for four PMOSFETs of different IMO layers. All four devices were stressed at V_d=-9V and V_g=-2V. In this stressing condition the origin of the device degradation is mainly due to the avalanche hot electron injection from the drain. The increase of I_{dl} as shown in the Fig. 4, as well as the observed increased subthreshold swing, is due to electron trappings in the oxide and the resultant "channel shortening" [9]. Fig.4 shows that the device with two layers of TEOS has the lowest net rate of electron trapping in the oxide, while the device without TEOS layer has the highest net rate, probably due to hole trapping in TEOS devices.

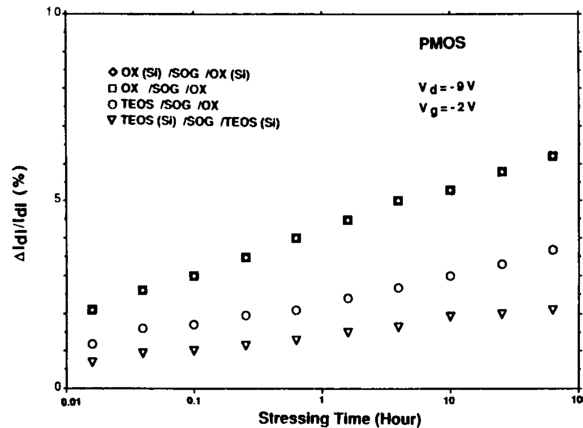

Fig.4 Linear drain current I_{dl} degradation versus stressing time for four PMOS devices with different IMO layers. Stressing bias V_g=-2V.

Fig.5 shows the change of I_{dl} vs. stressing time for PMOSFETs stressed at V_d=-9V and V_g=-10V. In this stressing condition, the gate oxide favors the channel hot hole injection [10,11]. Devices using TEOS layers show larger decreases in I_{dl} indicating the rate of hole trapping and/or hole-like donor-type interface trap generation is higher in TEOS devices. This is consistent with the behaviors of TEOS NMOSFETs.

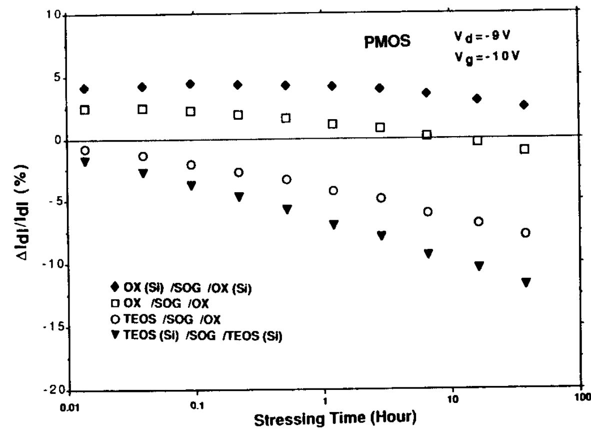

Fig.5 Linear drain current I_{dl} degradation versus stressing time for four PMOS devices with different IMO layers. Stressing bias V_g=-10V.

Fig. 6 shows the change of V_t vs. V_g after 10 hours' stressing for PMOSFETs with different IMO layers. At low $|V_g|$ (<5V) region, drain induced hot electron injection and trapping causes V_t to be less negative, i.e., $\Delta V_t > 0$. Devices with TEOS layers show less electron-trapping than devices with OX layers. While at high $|V_g|$ (>5V) region, some hot holes in the channel can surmount the gate oxide barrier, holes trapping in the oxide causes V_t to be more negative, i.e., $\Delta V_t < 0$. Devices with TEOS layers show more hole-trapping than devices with OX layers. The different behaviors of electron and hole trapping in different IMO layer devices agree with the discussion of Fig. 4 & 5 for PMOSFETs, and they are also consistent with the discussion of Fig. 1, 2 & 3 for NMOSFETs.

Fig. 7 shows the change of the threshold voltage V_t versus L_{eff} induced by Fowler-Nordheim stressing for NMOSFETs after 4.3 hours' stressing. The stressing condition is V_g=16.5V and V_d=V_s=V_{sub}=0V. Fig. 7 shows that NMOSFETs with TEOS oxide layer have higher rates of electron trapping than devices with OX layers. Notice that the difference between the two groups decreases with longer effective channel lengths. This phenomenon

suggests that the effect of TEOS layers on the gate oxide charge trapping characteristics may be located only near the source-drain edges of the channel. This is further supported by Fig. 8, where quasi-CV data of large (200x200 μm) capacitors with OX and TEOS IMO layers but without diffusion edges are compared. There is little difference in both stress-induced flatband shift and interface states generation (shape change in CV curves) between two capacitors. This confirms that the IMO layers have little influence on the interface property of gate oxide except near the source-drain edges.

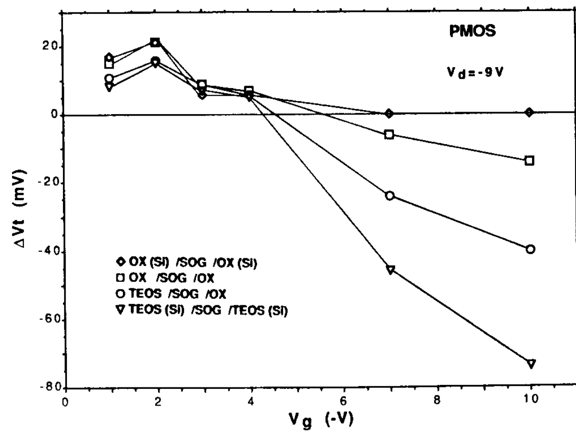

Fig.6 Threshold Voltage V_t degradation versus stressing gate bias V_g after 10 hours' stressing for four groups of PMOS devices with different IMO layers. Drain stressing bias V_d=-9V.

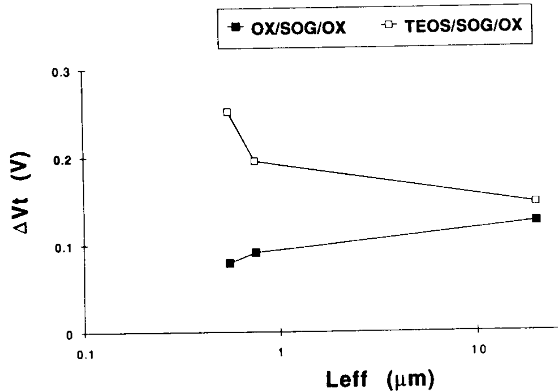

Fig.7 Fowler-Nordheim stressing induced threshold voltage shift versus effective channel length for two groups of NMOS devices with OX and TEOS oxide layers respectively. Stressing biases V_g=16.5V and V_d=V_s=V_{sub}=0V. Stressing time was 4.3 hours.

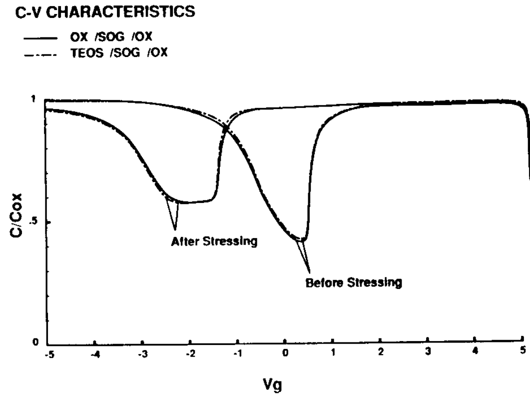

Fig.8 Quasi-CV measurements for two capacitors with OX and TEOS oxide layers before and after Fowler-Nordheim stressing. The dimension of the capacitor was 200x200 mm. Stressing time was 100s and constant gate current was -1E-6A.

In conclusion, we have found that the NMOSFETs under TEOS IMO layers have much worse hot-carrier-induced degradation than the devices under silane-based PECVD oxide layers, while PMOSFETs shows less net electron trapping. Si-rich oxide deposition can improve the hot carrier lifetime but do not overcome the deleterious effect of having additional TEOS oxide layers. The device degradation is apparently associated with hole trapping and enhanced trap generation process. The effect of the IMO layer is confined to the source-drain gate edges, therefore, it has a more serious effect on the shorter channel devices. Carbon base spin-on-glass [2,12] and carbon containing thermal oxides [3] were reported to lead to device instability. TEOS oxide effect reported here may stem from a similar carbon-related process.

Acknowledgment

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