

TIME DEPENDENCE OF FULLY-DEPLETED SOI MOSFET'S SUBTHRESHOLD CURRENT

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In this paper we show that the subthreshold current and the threshold voltage of fully-depleted SOI MOSFET's show a time dependent behavior under certain front-gate and back-gate voltage conditions. We provide an explanation for this behavior. The SOI devices used in the study were MOSFET's on SIMOX wafers. The gate oxide thickness (T_{fg}), silicon film thickness (T_{si}), and buried oxide thickness (T_{bg}) were approximately 118Å, 700Å, and 4000Å respectively. The doping concentration was $2 \times 10^{17} \text{cm}^{-3}$.

Figure 1 shows the front channel subthreshold current of a NMOS device as a function of front-gate voltage V_{fg} , while back-gate voltage is stepped from -10V to -60V. The theory in [1] predicts that since at $V_{bg} = -20\text{V}$ the back surface is accumulated, the curves for $V_{bg} = -20\text{V}, -30\text{V}, -40\text{V}$, and so on all should coincide. However, we see that the curves for $V_{bg} = -40\text{V}, -50\text{V}$, and -60V are distorted and are to the left of the curve for $V_{bg} = -30\text{V}$.

Figure 2 shows the subthreshold characteristics when $V_{bg} = -20\text{V}$ and V_{fg} is scanned from 0.2V to 1.2V with two different scan rates. Curve #1 corresponds to a very slow scan rate (3mv/sec), while curve #2 corresponds to a fast scan rate (100mv/sec). Both subthreshold slopes and threshold voltages differ significantly for these two curves. When $V_{bg} = -20\text{V}$, the back surface should be accumulated under steady-state conditions. However, the accumulation layer can not form immediately after the back gate voltage is applied. This implies that V_{tr} (front channel threshold voltage) still increases with decrease of V_{bg} [1]. Thus, V_{tr} is larger than its steady-state value. As time elapses, the generation of holes allows the accumulation layer to form. While the back surface becomes accumulated, V_{tr} gradually decreases toward its steady-state value.

This transient behavior is illustrated in figures 1 and 2. Curve #1 in figure 2, which is measured at a very slow scan rate, always allows enough time for the accumulation layer on the back side to form and represents the steady-state characteristics. In contrast, curve #2 in figure 2 is measured at a fast scan rate, so the accumulation layer is not formed, and V_{tr} is larger. This explains why curve #2 is shifted to the right with respect to curve #1. If the measurement for figure 1 were done very slowly, the curves for $V_{bg} = -20\text{V}, -30\text{V}, -40\text{V}, -50\text{V}$, and -60V would have coincided. Similar results are obtained if the measurements are repeated for PMOS devices. For example figure 3 shows the front channel current for two different scan rates, with V_{bg} set to 20V.

The above experiments can also be performed with the back surface inverted, and the front surface accumulated. Thus, the current is completely carried by the inversion layer at the lower silicon/oxide interface. A typical result for a NMOS device is shown in figure 4. All these transient behaviors could be further understood by observing the time response of the devices. If we define the value of V_{fg} where $I_D = 10\text{nA}$ as the threshold voltage (point #1 in figure 2), then $V_{tr} = 0.65\text{V}$ for curve #1 of figure 2. So if we set $V_{fg} = 0.65\text{V}$, $V_{bg} = -20\text{V}$, and measure I_D versus time, we expect the final steady-state value of I_D to be 10nA. This is shown in figure 5 (NMOS, front channel). Similar curves are shown for PMOS, and for the cases where current is carried by the back channel.

The difference between the subthreshold slopes in figure 2, (and similarly in figure 3) can be analytically evaluated. $S = (60\text{mv/dec}) \cdot n$, $n = (d\Phi_{fs}/dV_{fg})^{-1} = 1 + (C_{sub,eff}/C_{fg})$. Where, $C_{sub,eff}$ is the effective substrate capacitance, and C_{fg} is the front gate capacitance. When the silicon film is fully depleted, $C_{sub,eff}$ is the series combination of C_{si} (silicon film capacitance) and C_{bg} (buried oxide capacitance). Since C_{bg} is very small, $C_{sub,eff} \approx 0$, $n = 1$, and $S = 60\text{mv/dec}$, which agrees very well with the measured values in figures 2 and 3. On the other hand, if enough time has elapsed such that the accumulation layer forms, this layer becomes an AC ground plane in the voltage divider circuit and $C_{sub,eff} = C_{si} = \epsilon_{si}/T_{si}$. Using T_{si} , T_{fg} , and T_{bg} values for our devices, we obtain $S = 90.4 \text{mv/dec}$ which again agrees well with the measured values in figures 2 and 3.

Finally in figure 6, V_{fg} of a NMOS device is scanned from 0 to -8V for two scan rates (V_{bg} is set to 30V). The slow scan rate represents the steady-state condition. The rapid recovery seen for the fast scan at $V_{fg} = -4.5\text{V}$ is due to GIDL (gate-induced drain leakage), which provides the holes to accumulate the front surface. In summary, we have shown the time dependence of subthreshold current in fully-depleted SOI MOSFET's under certain front and back-gate voltage conditions. We have provided an explanation for this phenomena.

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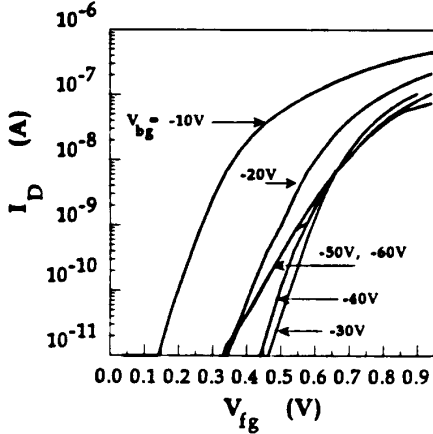


Fig. 1 Front channel subthreshold current of a NMOS, vs. front gate voltage.

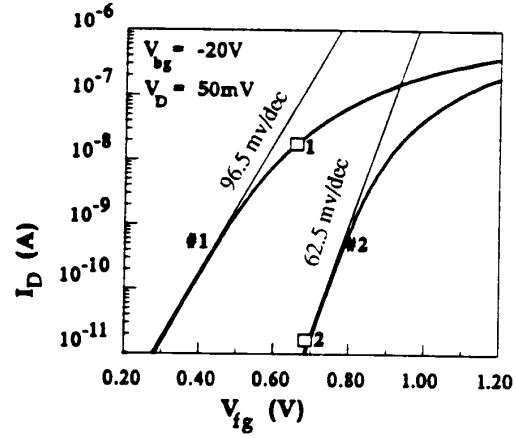


Fig. 2 Curve #1 represents slow scan of V_{fg} , curve #2 is for the fast scan of V_{fg} .

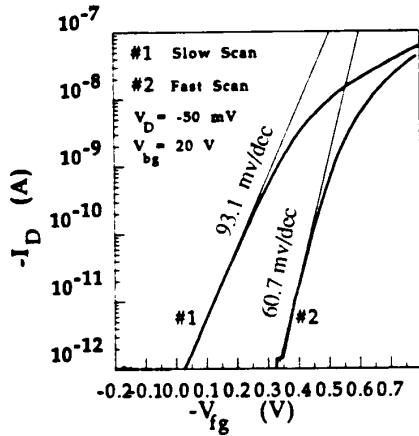


Fig. 3 Subthreshold current of a PMOS device for two different scan rates.

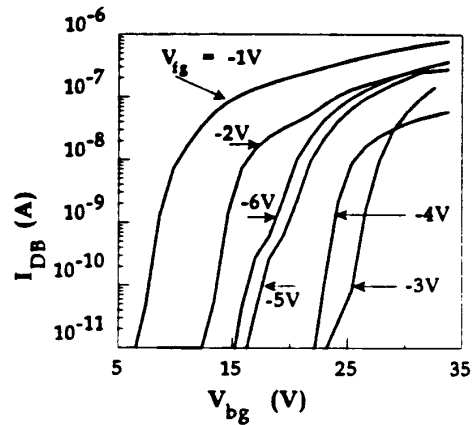


Fig. 4 Back channel subthreshold current of a NMOS, vs. back gate voltage.

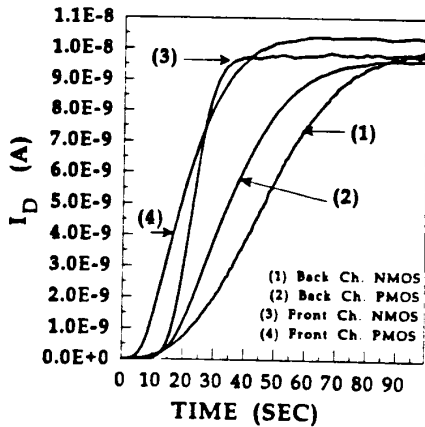


Fig. 5 Time response of the drain current.

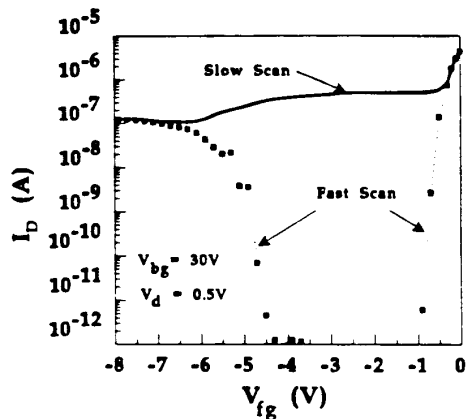


Fig. 6 V_{fg} is scanned from zero to -8V.