Antifuse Structure Comparison for Field Programmable Gate Arrays

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Abstract

Antifuse structure as a programming element has become increasingly popular in field programmable gate array devices. In this paper we will discuss the characteristics of various antifuse structures. Tradeoffs between performance and reliability will also be discussed.

Introduction

Field programmable gate arrays are becoming a major growth market in the ASIC sector, and antifuses are becoming a main programmable element for these products. n+ diffusion / ONO / polysilicon antifuses have been successfully used in field programmable gate array for many years[1]. TiW/Amorphous-Silicon(a-Si) / TiW antifuses have recently been used for the same application[2]. In this paper, the main characteristics of antifuses, which include leakage current and its dependence on temperature, antifuse resistance, breakdown voltage, time dependent dielectric breakdown, and resistance disturb during read of a programmed antifuse, are compared for the following antifuse structures: n+ diffusion / ONO / polysilicon, n+ diffusion / NO / polysilicon, metal / NON / metal, metal / a-Si / metal, metal / N / metal where O stands for oxide and N for nitride.

Leakage/Breakdown Voltage

Fig. 1 is a comparison of leakage current and breakdown voltage of several different antifuses. Data shows that in general metal to metal antifuses have higher leakage current while N+ diffusion to polysilicon antifuses have lower leakage current. The reason is that the quality and leakage of dielectrics grown at high temperature is better than those grown at low temperature which is the main constraint of metal to metal antifuses. Leakage current can be reduced by increasing antifuse film thickness. But thicker antifuse increases the breakdown voltage which limits the scaling. Choice of electrodes, antifuse material, cell structure, and process conditions allows further leakage current reduction. Fig. 1 shows that metal / dielectric / metal antifuse structure can have lower leakage current and lower breakdown voltage than the a - Si antifuse [3]. Lower antifuse breakdown voltage is required in order to integrate the antifuse in an advanced high speed technology. The effect of temperature on the antifuse leakage is shown in Fig. 2. N+ diffusion to polysilicon ONO antifuse again has the lowest leakage current density and temperature dependence among all antifuses surveyed.

Resistance

Fig. 3 shows the I - V plot of 5mA programmed antifuses. Programmed antifuse resistance for various antifuse structures(including polysilicon / NO / polysilicon[4]) is listed in Table 1. Programmed antifuse resistances are uniformly lower for metal to metal antifuses. It has been demonstrated that polysilicon links are formed in n+ diffusion / ONO / polysilicon programmed antifuses[5]. It is believed that metal or silicided links are formed in metal to metal antifuses. In addition, the parasitic resistance associated with the electrode resistance is lower for the metal to metal antifuse. For FPGA designs based on n+ diffusion / ONO / polysilicon antifuses, antifuses in critical delay paths can be programmed with larger currents to reduce their resistances. While lower resistances obtained for the metal to metal antifuse with lower programming currents are attractive, the read disturb phenomenon to be discussed later requires antifuses to be programmed with larger currents.

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TDDB

In FPGA applications, unprogrammed antifuses must withstand Vcc voltage without degradation. Fig. 4 shows the time dependent dielectric breakdown(TDDB) data. Except for one antifuse (metal / N / metal) which has a very low breakdown voltage, all other intrinsic antifuse lifetimes at 5.5V exceed 10 years. The intrinsic lifetime of metal / N / metal antifuse can be improved by simply increasing the nitride thickness. Defect failure lifetime is much less certain. While defect failure lifetime is longer than 10 years for n+ diffusion / dielectric / polysilicon antifuses[6], more work is required to characterize metal to metal antifuse defect failure lifetime. Amorphous silicon antifuse doesn't seem to exhibit TDDB like dielectric failures. This is attractive since it does not breakdown at 5.5V. One concern for a - Si is that it shows a time dependent leakage behavior[2]. This behavior should be taken care of during product design.

On-Resistance Stability

Circuit reliability requires the on-resistance of a programmed antifuse to remain unaltered during long term operation. Programmed metal to metal antifuses were found to exhibit a disturb phenomenon as shown in Fig. 5. The antifuse can be turned off when the DC read current is comparable to or larger than the programming current in a ramp voltage test. This turn-off behavior happens both in the forward and reverse read disturb direction with the reverse direction showing higher probability of disturb occurrence. The phenomenon is similar to electromigration. This read disturb phenomenon is not observed in n+ diffusion / ONO / polysilicon antifuses, shown in Fig. 6, since the link is made of single crystal silicon or poly crystalline silicon and not metals. The above data were obtained with a ramp voltage test. However, in FPGA products, antifuses are stressed by AC current without a DC component. AC stress generally results in longer lifetime than DC stress for electromigration[7]. Preliminary data supports the above theory. Operation current for metal to metal antifuses must be chosen such that it is well below programming current level to avoid this problem[2]. Such operation current limit is not required for n+ diffusion / ONO / polysilicon antifuse since it doesn't exhibit the read disturb problem.

Thickness Tradeoffs

Antifuse thickness also appears to affect metal to metal antifuse characteristics as shown schematically in Fig. 7. Increasing the antifuse thickness reduces the capacitance and reduces the leakage, but increases the programming voltage and increases the antifuse lifetime. Reducing antifuse thickness will also reduce the antifuse on resistance and the possibility of read disturb. Proper balance of each parameter is necessary.

Conclusions

N+ diffusion / ONO / polysilicon antifuses have been studied and used for years. Due to its low resistance and capacitance, metal to metal antifuse of either a-Si or dielectric will be an important interconnect device for future generation FPGAs. Its reliability and manufacturability require more work and characterization.

Acknowledgments

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Table 1. Antifuse Characteristics Comparison

Type	R(ohm) @5mA	BVG(V)	Leakage (pA/um2)	Leakage@125C/ Leakage@25C	TDDB(sec) @ 5.5V	I disturb DC / I program
N+ diffusion/ ONO / Poly	500	14	0.01	2X	1E+19	>10X
Poly / NO / Poly [4]	500	11	0.1	- *	1E+12	- *
Metal / NON / Metal[3]	65	11	1	2X	1E+10	2X
Metal / a-Si / Metal	180	13	100	50X	No TDDB **	1X
Metal / N / Metal	40	8	100	5X	30000	2X

*** data not available**

**** silicon antifuse doesn't exhibit TDDB like dielectric, but leakage current is time dependent[2].**

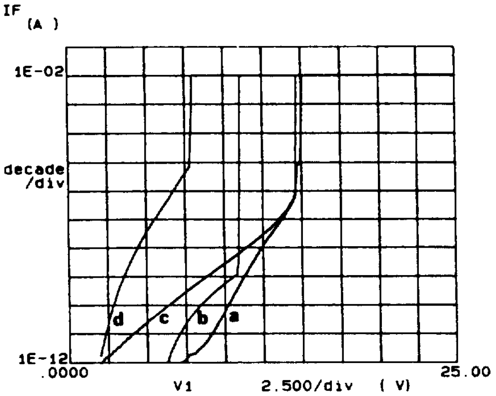

Fig. 1. Unprogrammed antifuse IVs : a) N+ diffusion / ONO / polysilicon, b) metal / NON / metal; c) metal / a-Si / metal; d) metal / N / metal.

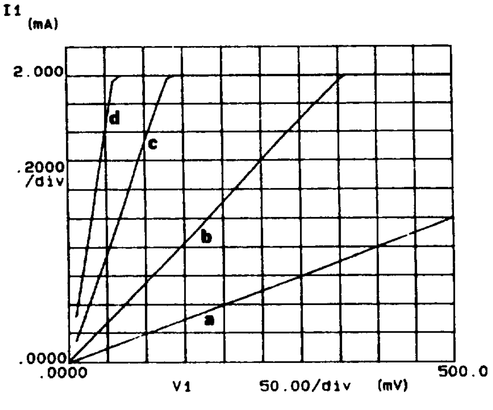

Fig. 3. IVs of antifuses programmed at 5mA current for: a) N+ / ONO / polysilicon; b) metal / a - Si / metal; c) metal / NON / metal ; d) metal / N / metal.

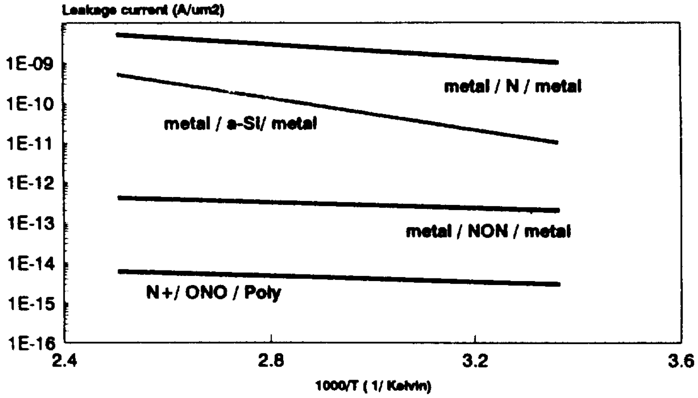

Fig. 2. Dielectric antifuse leakage has lower temperature sensitivity characteristics of tunneling conduction.

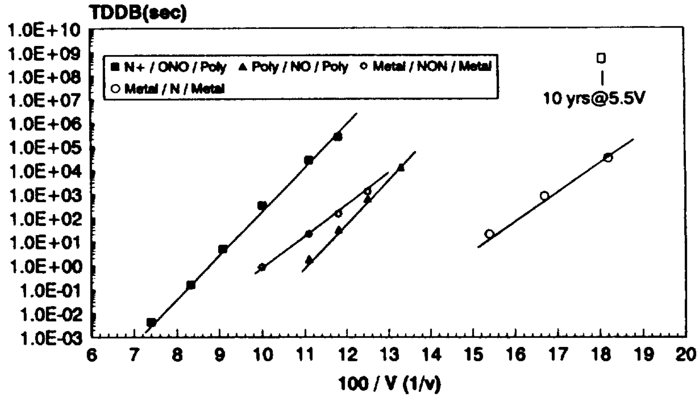

Fig. 4. Sensitivity of programming time to programming voltage and extrapolation of lifetime to 5.5V. (0.01 to 0.04mm2 area cap.) poly / NO / poly data is from [4].

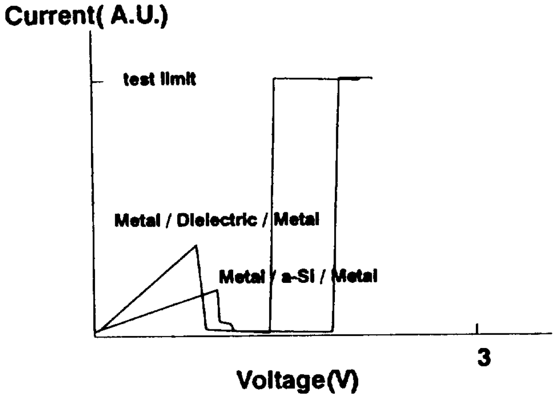

Fig. 5. Schematic showing that programmed metal to metal antifuse can be turned off when the reverse read current is larger than the programming current. The antifuse is programmed again at higher voltages (~ 1.5 to 2V).

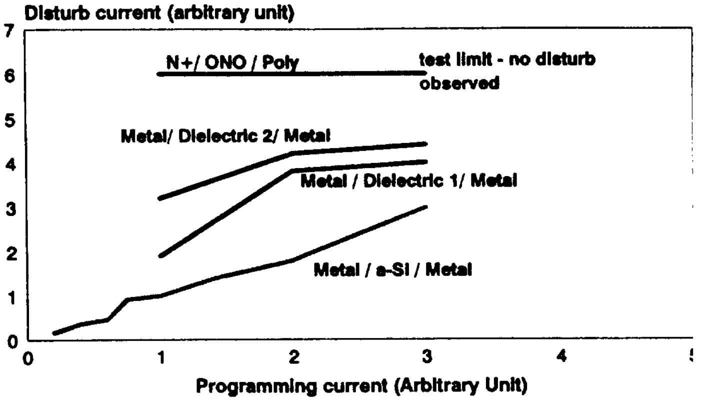

Fig. 6. Sensitivity of reverse DC read disturb current to programming current for different antifuse materials. Links made of poly silicon compounds is less sensitive to read disturb than links made of metallic compounds.

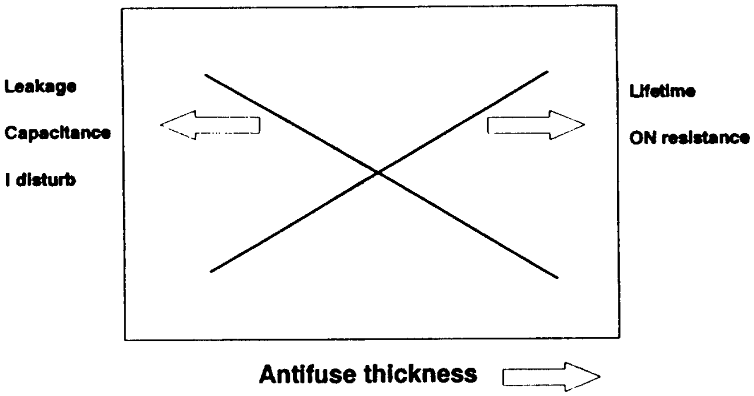

Fig. 7. Trends of metal to metal antifuse characteristics as a function of antifuse thickness. Increasing antifuse thickness lowers the capacitance, reduces the leakage, and improves the lifetime. Reducing antifuse thickness lowers the antifuse ON resistance and reduces the possibility of read disturb.