AC Hot-Carrier Degradation in a Voltage Controlled Oscillator

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ABSTRACT

A voltage controlled oscillator can be a useful supplement to ring oscillators for studying AC hot-carrier-induced degradation. AC stress is carried out with a fixed gate voltage while the drain voltage rises and falls. We found that device parameters degrade under AC stressing with the same time and voltage dependence as under DC stress, suggesting that the same mechanism(s) are at work. Oscillator frequency degradation is correlated with device degradation produced by AC or DC stressing.

I. INTRODUCTION

Hot-carrier-induced degradation is recognized as a scaling limit for CMOS submicron devices. Recent work has emphasized hot-carrier-induced degradation during dynamic (AC) stressing [1-5], which is closer to the real circuit operation. Despite many studies devoted to the study of AC hot carrier effect and its correlation with DC hot carrier effect, controversy regarding experimental results still exists. This controversy stems partly from the experimental errors induced in the high frequency AC test, the noise caused by the wiring inductance in VLSI circuits or/and measurement systems can enhance the hot carrier effect [3]. To date, the ring oscillator is the only circuit used for on-chip AC stress testing. Other circuits should also be used to obtain full picture of AC stress effect.

In this paper, we report the study of a Voltage-Controlled Oscillator (VCO) as a supplement for AC hot carrier-induced-degradation. A VCO circuit is widely used to implement phase-locked-loops, voltage-to-frequency converters and other practical circuits. VCO degradation is conveniently measured by the frequency drift. By applying DC and AC stressing to the n-channel MOSFET (labeled device under test, DUT), it offers an opportunity to correlate the DUT degradation under AC and DC stressing, as well as the VCO speed drift. This paper only reports the result of stress at 20 MHz.

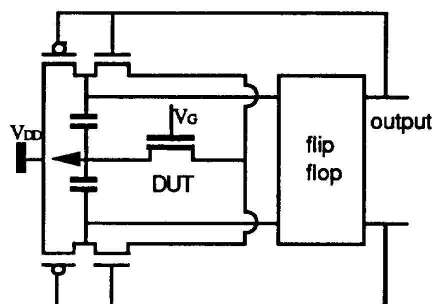

Figure 1a. Schematic of voltage controlled oscillator (VCO).

II. EXPERIMENTAL SET UP

Figure 1a is a schematic of a VCO. The oscillation frequency of this VCO is controlled by the DUT. When the VCO is operating, the DUT is stressed with the time varying wave forms. The two capacitors are alternatively charged through the PMOSFET and discharged through the DUT. Figure 1b shows a cycle of the SPICE simulated drain waveform of the DUT. The peak voltage of the AC waveform is smaller than the applied V_{DD} of 7V, due to the voltage drop in the pass transistor. The VCO frequency is mainly determined by the DUT impedance, the value of the capacitor, the gate bias and the trigger voltage of the flip flop circuit. Unlike in ring oscillators, V_G of the DUT is held constant and the stressing frequency, up to 100MHz, can be modified by changing V_G as shown in Figure 2.

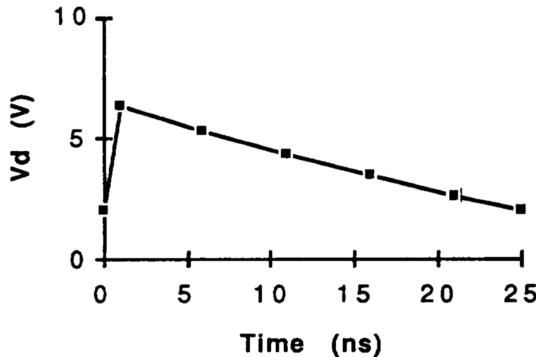

Figure 1b. SPICE simulated voltage waveform on the drain of the DUT with V_{DD}=7V and V_G=2V. AC frequency is 20 MHz. The waveform is repeated between 25 ns and 50 ns.

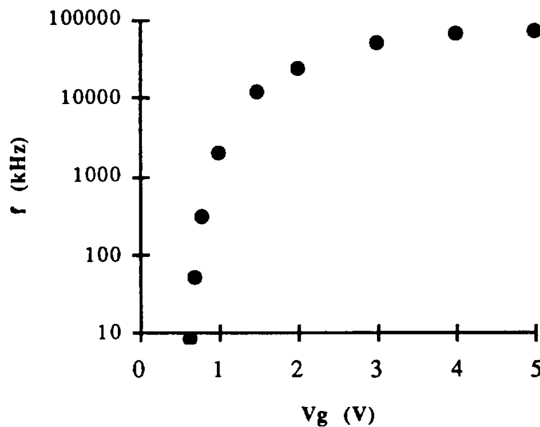

Figure 2. VCO frequency can be varied up to 100MHz by changing V_G.

Devices were fabricated using .6 μm CMOS technology. The NMOSFET used in this study has a gate length of .5 μm and a width of 20 μm. Its gate oxide thickness is 13.5nm. The gate material consists of a polycide/polysilicon stack. Both NMOS and PMOS devices received LDD implants prior to oxide spacer formation. Limited thermal cycles resulted in source-drain junction depths of about 0.2 μm. In the tested VCO circuit, the charging capacitor is 14.6 pf, the trigger voltage of the flip-flop circuit is 2V. Both DC and AC stressing were performed at maximum substrate current condition with V_{DD}=7V and V_G=2V. AC stressing frequency is around 20MHz.

III. RESULTS AND DISCUSSIONS

Figure 3 shows the degradation of the oscillator frequency f, transconductance G_m and threshold voltage V_T as a function of stress time for a typical sample. Where, G_m and V_T are obtained from the linear current measurement. Initially Δf follows the trend of ΔG_m with $\Delta f/f \approx 0.1 \Delta G_m/G_m$, which is similar to the relationship reported from the inverter ring-oscillator circuits [5]. However, when ΔV_T becomes larger, Δf follows the trend of ΔV_T.

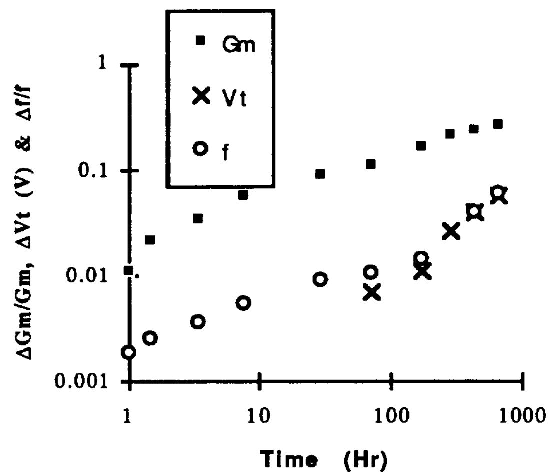

Figure 3. AC stressing induced degradation of frequency f (circle) of VCO correlates with degradation of threshold voltage V_T (cross) and transconductance G_m (square) of NMOSFET stressed at 20MHz. AC stressing biases are V_{DD}=7V and V_G=2V.

Figure 4 shows AC and DC stressing induced degradations of linear drain current I_D, transconductance G_m and threshold voltage V_T of the DUT as a function of stress time for two typical samples. These DC parameters show the same time dependence except for a shift in time scale of about 70 due to the "duty factor" of AC stressing. A quasi-static model [4,5] to estimate this "duty factor" was performed. SPICE model parameters for substrate currents were extracted from the electrical measurement of NMOSFETs. The drain voltage during AC and DC stressing were obtained from SPICE simulation. The AC waveform is shown in the Figure 1b. The calculated duty factor ratio of the DC and AC stress ages [5] was 1/30. Since the measured duty factor is smaller than the calculated quasi-static duty factor, we conclude that no "enhanced" AC stress degradation was observed in this AC stress test. The

difference between 30 and 70 is attributed to inaccuracies in waveform simulation and I_{sub} model parameters.

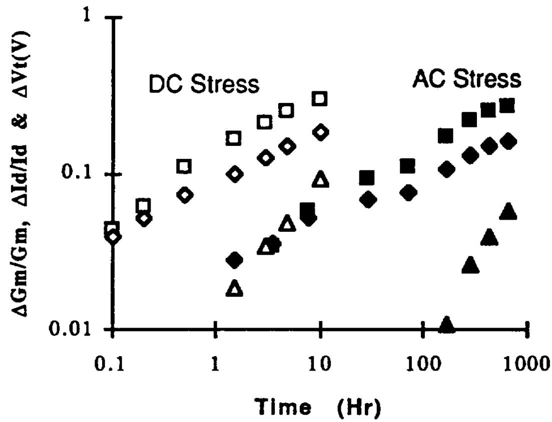

Figure 4. AC stressing-induced degradations of linear drain current I_D (diamond), transconductance G_m (square) and threshold voltage V_T (triangle) show the same time dependence as DC-stressing induced degradations of the DUT, where filled and empty symbols stand for AC and DC stressing, respectively. Stressing conditions are V_{DD}=7V and V_G=2V. AC stress frequency is 20 MHz.

Figure 5 shows that degradations of transconductance G_m (and subthreshold swing S and threshold voltage V_T) of the DUT are correlated to that of linear current I_D in the same manner whether the drifts are produced by AC or DC stressing. This suggests that the same physical mechanism(s), i.e., charge trapping or interface trap generation, are involved in AC and DC stressing.

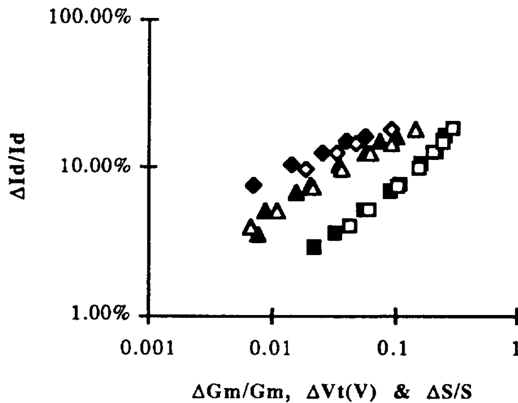

Figure 5. AC and DC stressing produces the same inter-parameter correlation for transconductance G_m (square), threshold voltage V_T (diamond), subthreshold swing S (triangle) and linear drain current I_D of the DUT, where filled and empty symbols stand for AC and DC stressing, respectively.

Figure 6 shows the device lifetime as a function of V_{DD} at V_G=2V. Device DC lifetime is defined as the DC stress time to produce $\Delta G_m/G_m$=10% and VCO AC lifetime is defined as the AC stress time to produce $\Delta f/f$=1% and $\Delta G_m/G_m$=10%, respectively. AC and DC stressing show the same V_{DD} dependence indicating the same mechanism(s) are involved and that device lifetime at working condition can be extrapolated from the accelerated DC stressing test. AC stressing lifetime is larger by about 70 times, consistent with Figure 4. Also, we note that that $\Delta f/f$ is slightly over 1% when ΔG_m has degraded by 10%.

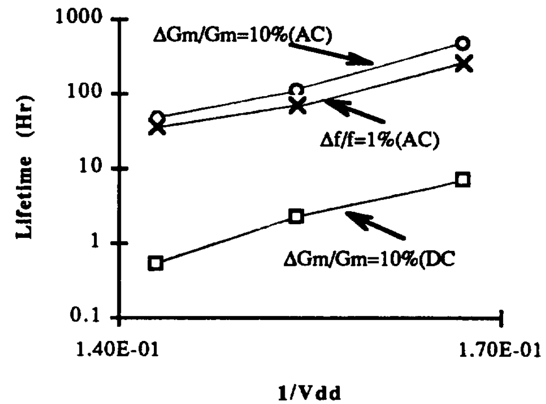

Figure 6. VCO circuit lifetime, AC and DC stressing induced device lifetime have all the same V_{DD} dependence. Device lifetime is defined as $\Delta G_m/G_m$=10% . VCO circuit lifetime is defined as $\Delta f/f$=1% at V_{DD}=V_G=5V.

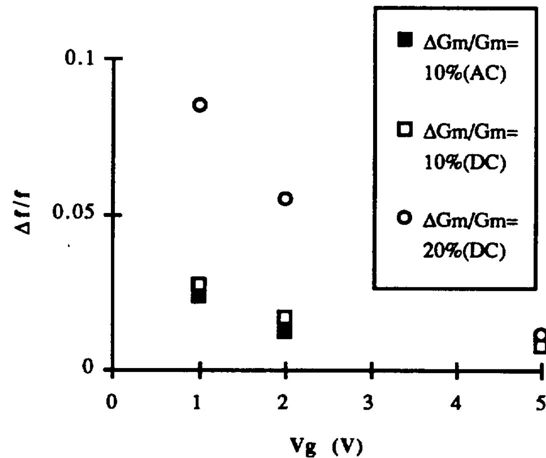

Figure 7. VCO frequency degradation increases with lower measurement V_G Stressing biases are V_{DD}=7V and V_G=2V.

Figure 7 shows that the degradation of circuit frequency Δf is a strong function of gate bias at which the frequency is measured. When $\Delta G_m/G_m$=10%, ΔV_T is smaller than 10mV as shown in Figure 4, $\Delta f/f$ is about 1-3% depending on V_G. But when $\Delta G_m/G_m$=20%, ΔV_T is 80mV as shown in the Figure 4, $\Delta f/f$ is very large at low V_G. This reflects the fact that V_T shift has a larger influence on the oscillator frequency at smaller V_G.

IV. CONCLUSION

Voltage controlled oscillator was used to generate 20 MHz stress signal and to detect device and circuit degradation due to AC stressing. AC stressing in general has the same effect on device and circuit as DC stress in terms of time dependence (except for duty factor difference), V_{DD} dependence, and correlation between ΔV_T and ΔI_D. The similarity suggests that the same mechanism are at work in both DC and AC stressing. The 20 MHz AC stress lifetime is 70 times larger than a DC stress. This ratio is less than the value calculated by quasi-static model indicating no evidence for enhanced AC degradation. The ratio between the degradations of oscillation frequency and device DC parameters depends on the circuit operating conditions.

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