

NOISE OVERSHOOT AT DRAIN CURRENT KINK IN SOI MOSFET

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Bias dependence of the drain current noise power of SOI MOSFET's were studied and low frequency noise overshoot at the drain current kink is observed for the first time in SOI MOSFET. The overshoot has a width of about 0.7 V and exhibits a peak noise power which is two orders of magnitude higher than the normal noise level. This newly found noise phenomena will affect the usefulness of SOI device in precision analogy circuits. It also provides a new way for studying traps related SOI film and device phenomena.

The SOI devices used in this study were N-channel polysilicon gate MOSFET's on SIMOX wafers fabricated with conventional sub-micron CMOS technology. The SOI film thickness, the buried-oxide thickness, and the gate oxide are 100nm, 300nm and 11.5 nm respectively. A computer-controlled test system was used to conduct the I-V and noise measurement automatically [1]. The substrates of the SOI wafers are grounded unless otherwise mentioned. The flicker noise of the device is much larger than the channel thermal noise as well as the background noise, and all the data reported here have been corrected for the background noise.

Figure 1(a) shows a typical I-V characteristic of an n-channel SOI MOSFET. Kinks in the drain current appear at moderate drain voltages. The corresponding drain current noise powers at 100 Hz (Figure 1(b)) for the same device overshoot around the kinks. The peaks of these overshoots are two orders of magnitude higher than the rest of the spectrum and their onsets appear to coincide with those of the kinks. The width of the overshoots is about 0.7 V.

In Fig. 2, Drain current noise power spectrums measured at different V_d 's are shown. For a V_d not in the overshoot region, the noise spectrum clearly exhibits a $1/f^k$ frequency dependence with the power factor k very close to unity, which is similar to that found in a conventional bulk MOSFET. However, for a V_d within the overshoot region, a Lorentzian is always clearly observed, as shown for $V_D=1.4$ V in Fig. 2.

In order to identify the origins of the overshoots, two experiments were conducted. In one experiment, a positive substrate bias $V_{SUB} = +25$ V was applied to the same n-channel SOI MOSFET used before. As shown in Fig. 3(a), the current kink disappears. This phenomenon is well understood [2]. Interestingly, however, the noise overshoots also disappears with the kink, as shown in Fig. 3(b). In another experiment, the kink and noise behaviors in a normal bulk n-channel MOSFET were studied. With the substrate floating, the I-V characteristic (Fig.3(a)) shows a current kink as expected[3]. However, no noise overshoot is observed around the kink region. These results suggest that in order for the noise overshoot to happen, both a current kink and a SOI film with a bottom Si-SiO₂ interface have to be present.

The occurrence of the noise overshoot and the noise peak can be explained by the following model. Figure 4 shows the schematic cross-section of a SOI device biased around the kink region. Hot electron hole pairs are generated due to impact ionization at high electric field near the drain junction. Electrons flow to the drain while holes flow to the floating body and accumulate near the bottom Si-SiO₂ interface of the silicon thin film. The source to body pn junction is slightly turned on in order to sink the hole current. This acquired body potential V_B decreases the threshold voltage V_T of the front-gate device thereby increases and causes a kink in the drain current. Due to trapping and detrapping which occur in the SIMOX material and at the bottom Si-SiO₂ interface, the body potential V_B fluctuates and consequently produces noise in the drain current. Since the drain current fluctuation dI_D equals $dI_D/dV_B * dV_B/dI_B * dI_B$, the drain current noise peak can be attribute to the dV_B/dI_B peak in the insert of Fig. 1(b) in which a qualitative I-V curve and the corresponding conductance dV_B/dI_B for the forward-biased body-to-source pn junction are shown. This model explains why both the kink (dI_D/dV_B) and the noise in V_B ($dV_B/dI_B * dI_B$) are required to produce the noise overshoot and the noise peak.

REFERENCES

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- [2] T. Elewa et al, *IEEE Tran. Electron Device*, vol. TED-37, no.4, p.1007, 1990
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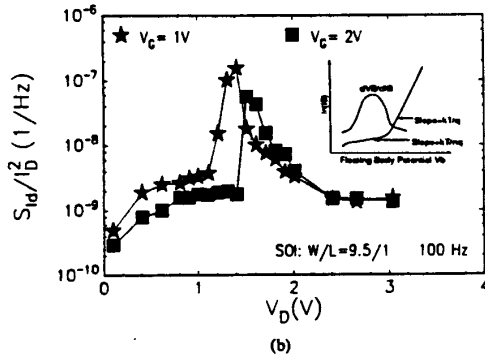
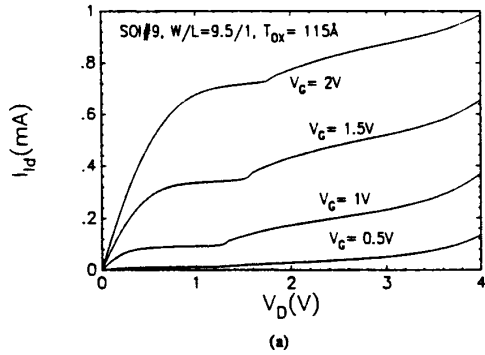


Fig.1 (a) Measured I-V characteristic for an n-channel SOI MOSFET. (b) Normalized drain current noise spectrum intensity vs. drain voltage V_D of the above device. The noise peaks coincides with the drain current kinks as in (a).

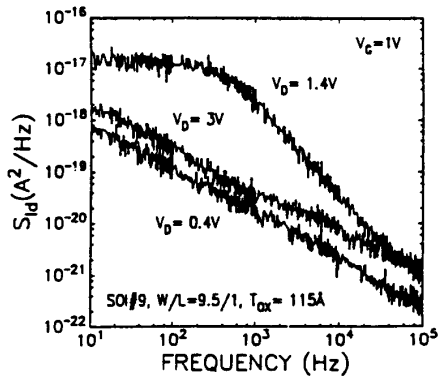


Fig.2 Drain current noise power spectrum for an SOI device biased at drain voltages before the kink ($V_D=0.4$ V), at the kink ($V_D=1.4$ V) and beyond the kink ($V_D=3$ V). For $V_D=1.4$ V case, a Lorentzian type spectrum is observed.

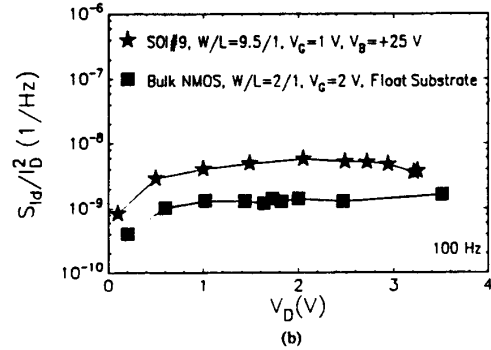
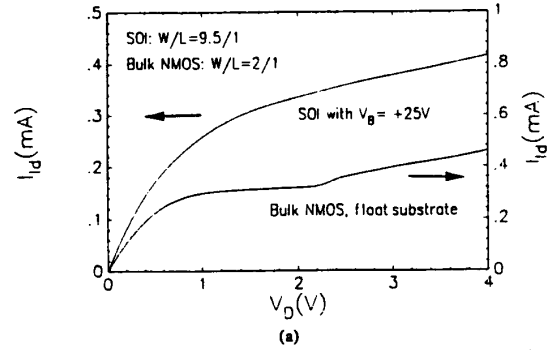


Fig.3 (a) Drain current kink disappears with a positive substrate voltage 25 V applied for SOI device. The lower curve shows a drain current kink is created for a conventional bulk n-channel device when the substrate floats. (b) No noise overshoot was observed in neither case suggesting that both a kink and back-interface are necessary for the noise peak to be generated.

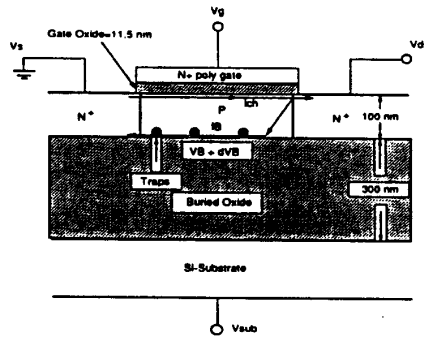


Fig.4 Schematic cross-section of an n-MOSFET on thin SOI film. The noise peak is attributed to the affect of back-side interface traps and the slightly forward-biased source body p-n junction.