

D5.

A DEEP-SUBMICROMETER RAISED SOURCE/DRAIN LDD STRUCTURE FABRICATED USING HOT-WALL EPITAXY

J.E. Moon, C. Galewski*, T. Garfinkel**, M. Wong†,
W.G. Oldham*, P.K. Ko*, and C. Hu*

Eastman Kodak Company
Rochester, New York 14650

Abstract

An elevated LDD (ELDD) structure has been designed, fabricated, and evaluated. A hot-wall reactor was used to selectively grow epitaxial silicon in the regions adjacent to the gate. The ELDD devices were equivalent to TOPS and LDD devices in current drive capability. The hot-electron reliability of the ELDD devices was superior to that of LDD devices. A general comparison among alternative LDD structures is given in terms of critical performance and reliability criteria. The ELDD structure is shown to be a promising candidate for deep-submicrometer applications.

Introduction

This paper presents a new LDD structure designed for deep-submicrometer VLSI circuits. The LDD structure¹ has been widely investigated as a means of reducing the lateral electric field and the associated hot carrier effects on reliability. As channel lengths are scaled toward 0.25 μm the area occupied by the lightly doped regions becomes significant^{2,3,4,5}. The elevated source/drain

LDD (ELDD) structure presented in this paper (Fig. 1) has been proposed as a way of controlling hot-carrier effects while still realizing the device and circuit density benefits inherent in

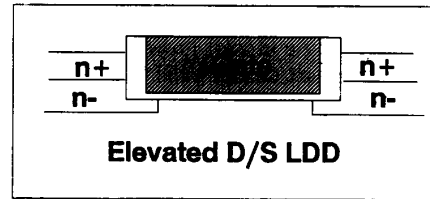


Figure 1

ELDD cross-section. Elevated junctions are formed in epitaxial silicon.

device scaling. Additionally, the ELDD structure will provide relief from short-channel effects such as drain-induced barrier lowering (DIBL) and punchthrough through ultra-shallow junctions while still maintaining low source/drain series resistance. A theoretical investigation of this and similar structures has recently been presented⁶.

Device Processing

The performance and reliability characteristics of ELDD devices are demonstrated in this paper and are compared to those of oxide-spacer LDD and fully-overlapped (TOPS)

* C. Galewski, W.G. Oldham, P.K.Ko, and C. Hu are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA;

** T. Garfinkel is with Intel Corporation, Santa Clara, CA;

† M. Wong is with Unisys, San Jose, CA.

Critical E-LDD Process Steps

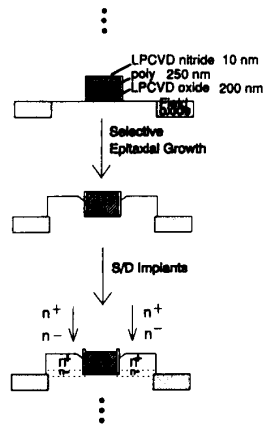


Figure 2

Epitaxial junction growth and implant steps. Gate isolation during epitaxial growth is ensured by a nitride cap and oxide sidewalls.

devices. The critical processing required to produce the ELDD structure is shown schematically in Fig. 2. All devices have a gate oxide of 11 nm and were fabricated using the deep submicrometer optical lithographic technique reported previously⁷. Another novel aspect of this work is that a hot-wall reactor with

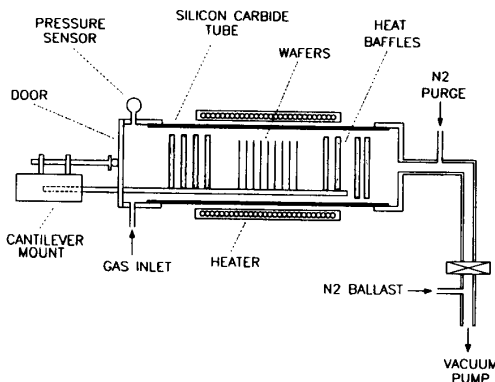


Figure 3

Schematic diagram of hot-wall silicon epitaxial reactor used to grow elevated source/drain regions.

the potential for low-cost applications was used to grow the selective epitaxial layer in the raised source/drain structure (Fig. 3). The reactor was built by modifying a tube in an LPCVD furnace bank⁸. In its present configuration it can accommodate up to 100 wafers of 100 mm diameter. Selective epitaxial deposition is achieved at 850°C by using a 0.6 torr mixture of dichlorosilane and hydrogen. The deposition rate is about 7 nm/min.



Figure 4

SEM cross-section of gate and epitaxial growth regions. LTO spacers are visible on both sides of the gate. Dark regions above the gate oxide plane are epitaxial silicon; below the plane are the junctions in the substrate. Gate length is about 0.3 μm .

Removal of the native oxide before deposition is accomplished by an HF vapor clean outside the reactor⁹, and a bake in hydrogen at 900°C inside the reactor. In this initial study the n-region was implanted before epi growth to ensure functionality. Subsequent thermal drive, however, reduced the anticipated short-channel benefits. In optimized devices the n-implant would be done after epi growth. Fig. 4 shows an SEM

cross-sectional view of the ELDD structure.

Performance

The drain current characteristics of ELDD and LDD devices are compared in Fig. 5 for $L_{eff} = 0.5 \mu\text{m}$. Saturation drain current and transconductance of

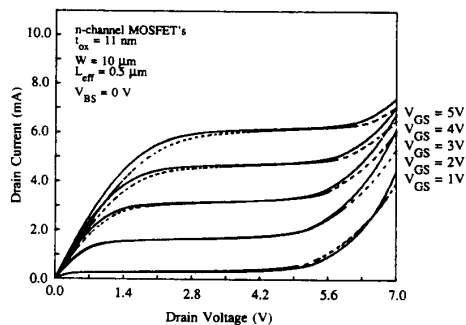


Figure 5

Drain current characteristics of ELDD and LDD devices with $L_{eff} = 0.5 \mu\text{m}$. n^- doses were $1.2 \times 10^{14} \text{ cm}^{-2}$ for both devices. Dashed lines (---) are ELDD; solid lines (—) are LDD.

the ELDD device are similar to those of the oxide spacer LDD. Breakdown voltage is slightly larger for the ELDD device. Series resistance is somewhat larger due to the non-optimal source/drain implant profile. An optimally-designed source/drain doping profile is expected to have less resistance due to the larger area available for current spreading into the drain n^- and n^+ regions while still maintaining the short-channel benefits of an ultra-shallow junction. Fig. 6 shows the saturation current for ELDD, LDD, and TOPS devices as a function of L_{eff} . The ELDD devices are equivalent to TOPS and LDD in current drive capability. The DIBL characteristics shown in Fig. 7 for ELDD and LDD devices are similar as well.

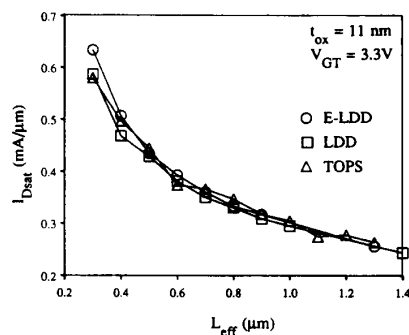


Figure 6

Drain saturation current of ELDD, LDD, and TOPS devices as a function of effective channel length. Implanted n^- doses are 1.2×10^{14} , 1.2×10^{14} , and $3 \times 10^{13} \text{ cm}^{-2}$.

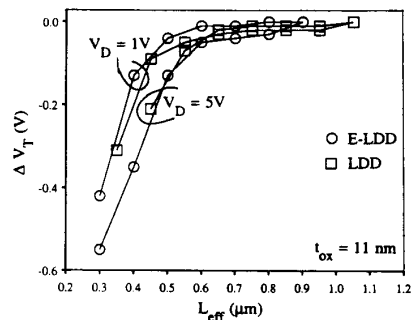


Figure 7

Drain-induced barrier lowering (DIBL) behavior of ELDD and LDD devices.

Reliability

It is expected that the reliability of the ELDD structure will be superior to that of conventional LDD. Fig. 8 compares the substrate current for ELDD and LDD devices with $L_{eff} = 0.5 \mu\text{m}$. The nearly identical shape of the curves is indicative of similar channel electric field patterns in the two structures. Gate current generated at large drain voltages (up to 10V) in the ELDD and LDD devices has a very similar relationship to I_{sub} indicating that the models of gate current as presently understood¹⁰ are applicable

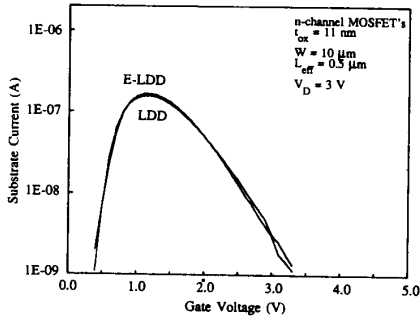


Figure 8
Substrate current characteristics of ELDD and LDD devices.

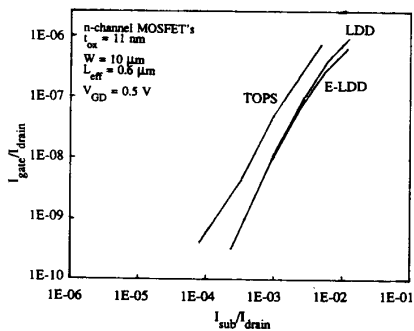


Figure 9
Gate current/substrate current relationship for ELDD, LDD, and TOPS devices.

to this new structure (Fig. 9). Hot carrier degradation under accelerated stressing conditions proceeds more slowly in the ELDD devices than in LDD because of the location of the peak electric field in the vertical drain, the thicker oxide between the gate and drain, and the flow of current away from the silicon surface at the point of maximum electric field. Fig. 10 shows the percentage degradation in forward-linear drain current as a function of stress time for $L_{eff} = 0.5 \mu\text{m}$. Fig. 11 presents a definitive comparison of performance and reliability among the ELDD, LDD, and TOPS devices evaluated. These data demonstrate a 50% improvement in degradation with

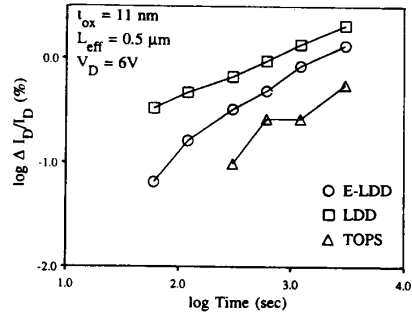


Figure 10
Time dependence of current degradation under stress. Devices were stressed at peak I_{sub} and $V_d = 6V$ up to 50 minutes. Current degradation values are for forward linear operation ($V_g = 4V$, $V_d = 50 mV$).

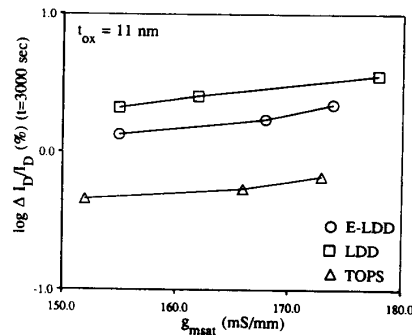


Figure 11
Overall performance comparison of ELDD, LDD, and TOPS technologies. Degradation values are for forward linear operation and g_{msat} values are measured at $V_d = 3.3V$.

ELDD over LDD at equivalent drive or, conversely, a 15% improvement in drive for comparable degradation. As before⁵, the TOPS devices have a drive/reliability advantage. However, higher overlap capacitance in the TOPS devices may make it desirable to trade off some reliability for device and circuit speed.


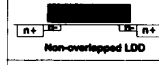



	DMBL	Drive	HE relab.	GRDL	Complexity	Cap	Density
 Conventional	-	++	-	-	+	0	+
 Non-overlapped LDD	+	0	+	+	0	++	-
 Fully-overlapped LDD	+	+	++	0	0/-	-	-
 Fully-overlapped Drain-only LDD	+	+	++	0	-	+	-
 Elevated D/S LDD	+	0	++	+	-	+	+

Figure 12
Comparison of ELDD, LDD, TOPS, and non-LDD technologies in terms of critical performance and reliability parameters.

Conclusions

We have successfully fabricated and tested a new LDD structure which has elevated source/drain regions. The ELDD structure's source/drain regions are grown by selective silicon epitaxy, seeding from the monocrystalline substrate in the areas immediately adjacent to the gate. Device performance is equivalent to that of oxide-spacer and TOPS LDD devices. The reliability of the ELDD devices was better than that of oxide-spacer LDD devices. In a general comparison of device performance and reliability, the ELDD devices are superior to LDD devices, giving 15% more drive at a comparable level of degradation or 50% less degradation for comparable current drive. Fig. 12 shows a qualitative comparison of ELDD to non-LDD and several other LDD technologies in terms of seven important performance and reliability criteria. It should be noted here that the ELDD structure occupies a favorable position in comparison to the

other technologies that we have evaluated. Its sole drawback appears to be the degree of process complexity that is encountered in its fabrication. The principal difficulty in the fabrication of the ELDD structure is the maintenance of gate isolation prior to and during epitaxial growth.

References:

- [1] S. Ogura *et al.*, *IEEE Trans. Electron Devices*, **ED-27**, 1359 (1980).
- [2] T. Huang *et al.*, *IEEE Electron Device Lett.*, **EDL-8**, 151 (1987).
- [3] R. Izawa *et al.*, *Tech. Dig. -- Int. Electron Devices Meet.*, pp. 38-41 (1987).
- [4] T. Hori *et al.*, *Symp. VLSI Technology*, p. 15 (1988).
- [5] J.E. Moon *et al.*, *IEEE Electron Device Lett.*, **EDL-11**, 221 (1990).
- [6] A.F. Tasch *et al.*, *Symp. VLSI Technology*, p. 43 (1990).
- [7] J. Chung *et al.*, *IEEE Electron Device Lett.*, **EDL-9**, 186 (1988).
- [8] C. Galewski *et al.*, *Symp. VLSI Technology*, p. 79 (1988).
- [9] C. Galewski *et al.*, *IEEE Trans. Semicon. Manuf.*, vol. 3, no. 3, p. 93 (1990).
- [10] C. Hu *et al.*, *IEEE Trans. Electron Devices*, **ED-32**, 375 (1985).