A High-Performance Lateral Bipolar Transistor Fabricated on SIMOX

Stephen A. Parke, Chenming Hu, *Fellow, IEEE*, and Ping K. Ko, *Member, IEEE*

***Abstract*—Double-diffused, lateral n-p-n bipolar transistors were fabricated in a simple CMOS-like process using SIMOX silicon-on-insulator (SOI) substrates. Excellent device characteristics were achieved, with peak h_{FE} = 120, BV_{CEO} = 10 V, and peak f_t = 4.5 GHz. The f_t versus BV_{CEO} trade-off was studied as a function of n^- collector width. $f_t > 25$ GHz is predicted for this structure with an improved device layout and optimized basewidth. This process may be easily extended in order to fabricate complementary BJT's in a C-BiCMOS thin-film SOI technology.**

I. Introduction

With the advent of deep-submicrometer photolithography, lateral bipolar transistors are being reinvestigated as potentially attractive devices for achieving medium-to-high performance in a simplified, CMOS-like, fully complementary BiCMOS technology [1]. However, if these lateral BJT's are implemented on bulk silicon wafers, several problems arise with both process integration and device performance, due to the parasitic vertical devices that coexist with the lateral transistors. Thin-film silicon-on-insulator (SOI) substrates permit much simpler device integration. In addition, the buried oxide eliminates the vertical parasitics, permitting high-performance operation. Early lateral n-p-n's were fabricated on poor-quality SOI films with 1.5–3.0-μm lithographically defined base-widths [2], [3]. These devices exhibited very low current gains. More recently, current gains of 75 and 40 were achieved for lateral n-p-n's and p-n-p's, respectively, using a 0.5-μm CMOS process on high-quality laser-recrystallized SOI [4]. Most recently, thin-base double-diffused lateral n-p-n's have been fabricated on bonded wafer [5] and epitaxial lateral overgrowth SOI [6], with current gains of about 20 and f_t as high as 20 GHz. This lateral double-diffused structure provides a lightly doped collector, and is only possible on thin-film SOI. In addition to yielding high-speed operation, the lateral double-diffused structure permits optimization of f_t versus BV_{ceo} for each individual device, by lithographically varying the collector width. However, these recently reported structures have used the polysilicon gate as either an extrinsic collector [5] or base [6] contact, which introduces added process complexity over the simple SOI CMOS process, and eliminates the possibility of independently biasing the polysilicon gate electrode.

In this paper, we describe a simpler, CMOS-compatible, double-diffused lateral n-p-n that can be used as either a three- or four-terminal device. Unlike previous work, these devices were fabricated using commercially available SIMOX substrates. The n-p-n devices exhibit a current gain of 120, with a peak cutoff frequency of 4.5 GHz. Higher performance ($f_t > 25$ GHz) is projected for an optimized device design and layout.

Manuscript received July 21, 1992; revised November 2, 1992.

The authors are with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720.

IEEE Log Number 9205992.

II. Device Structure and Fabrication

The n-p-n devices were fabricated in a double-diffused drain (DDD) CMOS process using a masked, vertical base implant on the emitter side of the gate only. This boron implant was subsequently driven laterally, under the gate edge, so that it is completely overlapped by the gate. The multiply-implanted and annealed SIMOX substrates were fabricated by IBIS Technology Corporation with SOI and buried oxide thicknesses of 180 and 390 nm, respectively. Oxidized-sidewall MESA isolation was performed, followed by a phosphorus collector implant with a dose of $2 \times 10^{12}/cm^2$. In an integrated process, polysilicon gates would be formed next. However, these devices utilized CVD oxide "gates" in order to study the ungated lateral BJT device behavior. "Gate" lengths as short as 0.2 μm were obtained by oxygen plasma photoresist "ashing" for 10 min at 50 W, prior to the gate etch. The boron base was then implanted vertically on the emitter side of the "gate" and driven laterally for 1 h at 950°C in N_2. Both low-energy (15 keV) and high-energy (45 keV) boron implants were performed in order to place the peak base concentrations near the front and back oxide interfaces. This prevents a low base punchthrough voltage along these interfaces. The total base dose was $3 \times 10^{14}/cm^2$, resulting in a base width of 0.16 μm, as measured by SEM and base transit-time extrapolation. Complementary high-dose arsenic and boron implants followed. These implants form the emitter, extrinsic collector, and extrinsic base contacts. The intrinsic base "finger" is contacted at the edges of the device by p^+ regions, as shown in Fig. 1(a). The intrinsic base resistance is strongly dependent on the device width. An SEM cross section of the completed device is shown in Fig. 1(b). Device processing was performed in the University of California, Berkeley Microfabrication Laboratory.

0741-3106/93$03.00 © 1993 IEEE

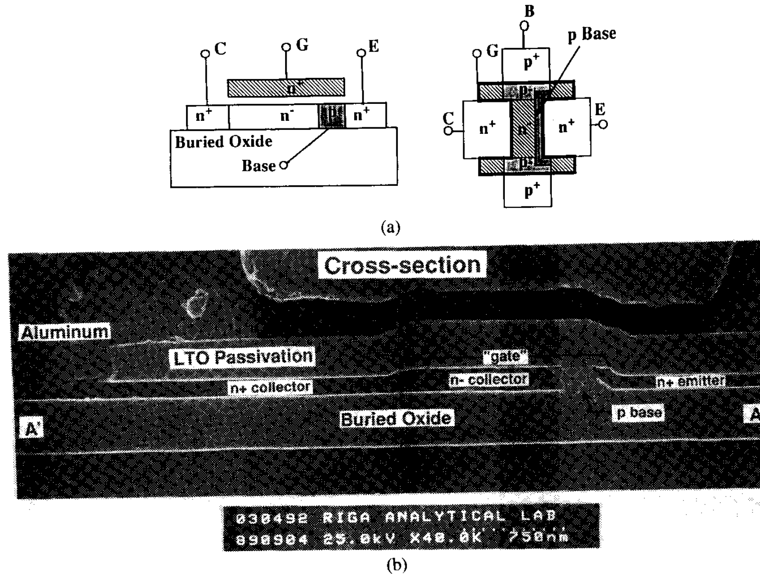

Fig. 1. (a) Lateral double-diffused n-p-n cross section and four-terminal layout. (b) Cross-sectional SEM of the completed lateral n-p-n device.

III. Device Characterization

I_c–V_{ce} characteristics for collector widths of 0.2 and 1.2 μm are shown in Fig. 2, demonstrating the strong sensitivity to the width of the lightly doped collector. The devices exhibit breakdown voltages of 2.5 and 10 V, respectively. No front- or back-gate biases were needed in order to accumulate the SOI/oxide interfaces, due to the dual-energy base implant. The Gummel plot is shown in Fig. 3. A peak current gain of 120 was obtained for this device. This is the highest value reported thus far for pure lateral BJT action, excluding gated-BJT behavior [7]. Ideal base current is observed down to the picoampere range, indicating a defect-free SIMOX base region for this device. However, a wide distribution of base currents was observed, indicating possible bulk or surface recombination site defects, which may be associated with the SIMOX process. The current gain is flat over five decades of collector current, as seen in Fig. 4. High-frequency f_t measurements were also performed on these devices using a Cascade probe and HP network analyzer setup. A peak f_t of 4.5 GHz at $I_C = 0.2$ mA was obtained for a collector width of 0.1 μm. The forward base transit time (τ_F) was plotted versus $1/I_c$. Linear extrapolation yielded an intrinsic $\tau_F = 19.2$ ps, which indicates a base width of 0.16 μm if uniform base doping is assumed. This base width is larger than desired and may be reduced by lowering the base drive-in time and/or temperature. In addition, the intrinsic base resistance increases by approximately 500 Ω for each micrometer of device width, as measured from the base contacts at the device edges. This base resistance effectively debiased much of the 40-μm-wide device that was used for our f_t measurements. DC current measurements for various device widths show that

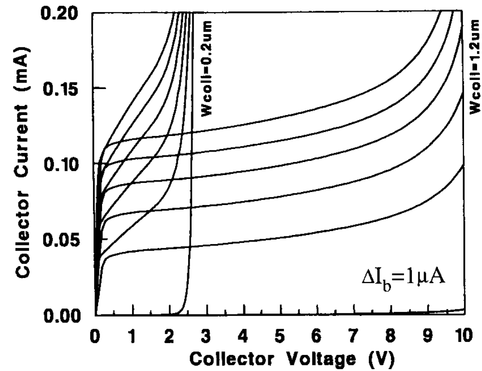

Fig. 2. I_c–V_{ce} characteristics for devices with collector widths of 0.2 and 1.2 μm.

the effective width of this 40-μm device is only 7 μm. Therefore, the f_t device contains excess parasitic capacitance width compared with its actual current drive width. An improved interdigitated device layout containing forty 5-μm-wide device segments in parallel is currently being investigated, and is projected to have $f_t > 25$ GHz. Fig. 5 shows the open-base breakdown voltage (BV_{ceo}) and f_t as a function of n^- collector width. The widths were obtained by lithographically varying the "gate" length. The collector width of each transistor may be optimized for either high speed or high voltage, depending on the particular circuit application.

IV. Conclusion

Simple CMOS-compatible lateral n-p-n transistors have been fabricated on SIMOX SOI substrates. These devices

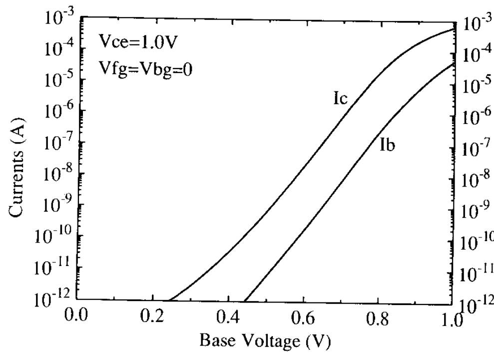

Fig. 3. Gummel plot with V_{ce} = 1.0 V showing ideal base current and h_{fe} = 120.

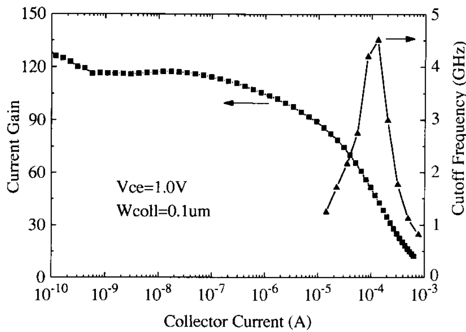

Fig. 4. Current gain and f_t as a function of collector current with V_{ce} = 1.0 V.

utilize a double-diffused, narrow-base structure and oxide isolation to achieve excellent performance. This structure enables an SOI C-BiCMOS technology utilizing complementary lateral BJT's with much lower process complexity than that required for typical BiCMOS processes.

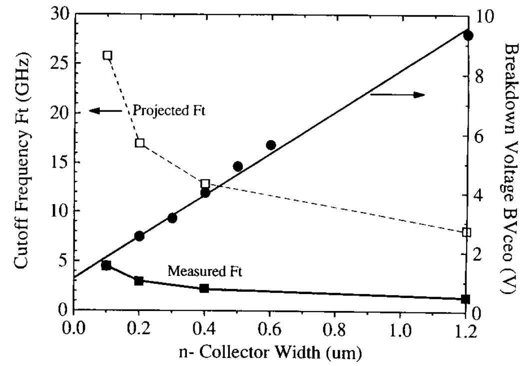

Fig. 5. BV_{ceo} and f_t as a function of n$^-$ collector width. The projected f_t data are for an optimized base width and an interdigitated device layout.

Acknowledgment

The authors thank G. Fuller and M. Varon of Hewlett-Packard Labs for the f_t measurements.

References

[1] A. Tamba, T. Someya, T. Sakagami, N. Akiyama, and Y. Kobayashi, "CMOS-compatible lateral bipolar transistor for BiCMOS technology: Part II—Experimental results," *IEEE Trans. Electron Devices*, vol. 39, no. 8, pp. 1865–1869, 1992.

[2] M. Rodder and D. A. Antoniadis, "Silicon-on-insulator bipolar transistors," *IEEE Electron Device Lett.*, vol. EDL-4, pp. 193–195, 1983.

[3] J. Sturm, J. P. McVittie, J. F. Gibbons, and L. Pfeiffer, "A lateral silicon-on-insulator bipolar transistor with a self-aligned base contact," *IEEE Electron Device Lett.*, vol. EDL-8, pp. 104–106, 1987.

[4] J. P. Colinge, "Half-micrometer-base lateral bipolar transistors made in thin silicon-on-insulator films," *Electron. Lett.*, vol. 22, no. 17, pp. 886–887, 1986.

[5] N. Higaki *et al.*, "A thin-base lateral bipolar transistor fabricated on bonded SOI," in *1991 Symp. VLSI Technology Dig. Tech. Papers*, pp. 53–54.

[6] G. G. Shahidi *et al.*, "A novel high-performance lateral bipolar on SOI," in *1991 IEDM Tech. Dig.*, pp. 663–666.

[7] S. Verdonckt-Vandebroek, S. Wong, and P. K. Ko, "High gain lateral bipolar transistor," in *1988 IEDM Tech. Dig.*, pp. 406–409.