Electromigration Performance of Electroless Plated Copper/ Pd-Silicide Metallization

Jiang Tao, Nathan W. Cheung, *Member, IEEE,* Chenming Hu, *Fellow, IEEE,* H.-K. Kang, and
S. Simon Wong, *Senior Member, IEEE*

Abstract—**The electromigration reliability of copper interconnect has been studied under dc, pulse-dc, and bipolar current stressing conditions. Electroless plating was used to selectively deposit Cu in oxide trenches by using Pd silicide as a catalytic layer at the bottom of the trenches to initiate copper deposition. The dc and pulse-dc lifetimes of Cu are found to be about two orders of magnitude longer than that of Al–2%Si at 275°C, and about four orders of magnitude longer than that of Al–2%Si when extrapolated to room temperature. On the other hand, Cu ac lifetimes are found to be comparable to the ac lifetimes of Al–2%Si. The pulse-dc lifetime of copper interconnects follows the similar frequency and duty factor dependence as aluminum and the prediction of the vacancy relaxation model.**

I. INTRODUCTION

As THE device dimension enters the sub-half-micrometer region, the need for a high electric conductivity and high electromigration resistance metal as interconnect material in integrated circuits is becoming more urgent. Copper has been investigated as a candidate [1], [2] because it has a higher melting point and lower electrical resistivity than Al-based alloys, which should significantly improve its electromigration behavior. However, little data are available to confirm or quantify these expectations. The objective of this work is to study the electromigration behaviors of copper metallization under continuous current and time-varying current stressing conditions.

II. EXPERIMENTS

A 600-Å LPCVD polysilicon film was deposited onto the ⟨100⟩ Si wafers covered with 5000-Å thermally grown SiO_2. After polysilicon etching, trenches of 1.5 and 2.5 μm width and 100 μm length were etched through 8000-Å LTO layer by dry etching. Then 2000-Å Pd was evaporated and annealed at 245°C for 15 min in Ar ambient to react with the underlying polysilicon. The unreacted Pd on oxide and trenches were selectively removed by wet etch. The wafers were then immersed in the normal electroless copper bath which contains cupric salt ($CuSO_4$–$5H_2O$), formaldehyde (as the reducing agent), and ethylenediaminetetraacetic acid (EDTA) (as the complexing or chelating agent). The pH value of the plating solution was 13. The plating bath temperature was kept at 70°C, and the plating rate was about 250 Å/min. The plated Cu film thickness is about 3000 Å. As the Cu film is easily oxidized in air, a 6000-Å overcoating of SiO_2 layer was deposited by low-temperature PECVD, and the contact holes were formed by dry etching. Pure 1-μm-thick aluminum was sputtered, and etched to form the contact pads. The inset of Fig. 1 shows the cross section of the structure. The resistivity of this Cu/Pd-silicide stack film was measured by four-point probe and found to be 2.1 $\mu\Omega \cdot$cm, and the temperature-resistance-coefficient (TRC) film is 3.4×10^{-3}/°C.

For comparison, a group of Al–2%Si samples is also prepared. Al–2%Si film of 5000 Å thickness is sputter-deposited onto the silicon wafers covered with 600-Å thermally formed SiO_2. Test stripes of 1 and 2 μm width, 86 and 170 μm length were formed by RIE dry etching process. The test structures are not passivated.

A current source regulated by a transistor and driven by the output of a TTL gate was used to generate pulsed dc and ac currents [3]. Electromigration testing was performed on wafers placed directly on the heated stage of probe station. All electromigration tests were carried out at an ambient temperature of 275°C. The failure was defined to be when the circuit was completely open.

III. RESULTS AND DISCUSSION

Fig. 1 shows a log-normal plot of the lifetime distribution of Cu and Al–2%Si samples for $J_{DC} = 1.5 \times 10^7$ A/cm^2. We can see that the median time to failure (MTTF) of Cu is about two orders of magnitude longer than that of Al–2%Si. The longer lifetime for Cu suggests a higher energy barrier for atomic motion. Indeed, from the Arrhenius plot of MTTF, the activation energy of electroless plated Cu is found to be about 0.8 eV [4], versus 0.4 eV for Al–2%Si [3]. Scanning electron microscopy (SEM) was used to observe the failure sites. Cu depletion (void) and accumulation (hillock) were observed, as shown in Fig. 2(a) and (b), respectively.

The vacancy relaxation model of Liew *et al.* [3] has been

Manuscript received April 16, 1992; revised June 11, 1992.

J. Tao, N. W. Cheung, and C. Hu are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720.

H.-K. Kang and S. S. Wong are with the Center for Integrated Systems, Stanford University, Stanford, CA 94305.

IEEE Log Number 9202475.

0741-3106/92$03.00 © 1992 IEEE

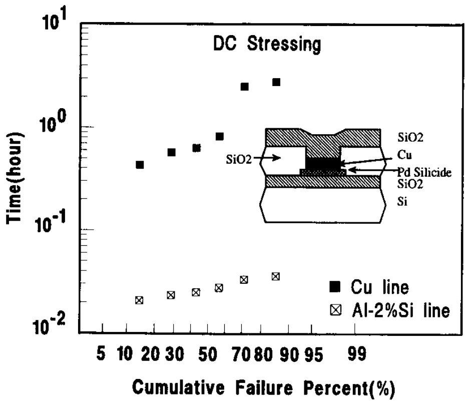
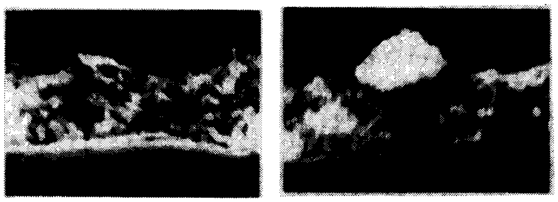


Fig. 1. Log-normal plot of the cumulative failure rate for Cu and Al–2%Si stripes under $J_{\mathrm{DC}} = 1.5 \times 10^7$ A/cm^2 and $T = 275$°C. The inset shows the cross-section structure of the electroless plated Cu sample.



(a) (b)

Fig. 2. SEM micrographs of (a) void and (b) hillock formation in Cu stripes under $J_{\mathrm{DC}} = 1.5 \times 10^7$ A/cm^2 and $T = 275$°C.

used to satisfactorily explain the difference between the electromigration characteristics of Al metal [3], [5] under pulse dc and dc stressings. Under the special condition of the rectangular current waveform, the MTTF can be written as [5]

$$\mathrm{MTTF}_{\text{pulse-DC}} = \frac{\mathrm{MTTF}_{\mathrm{DC}}}{D\left[1 - \dfrac{(1-e^{-aD})(1-e^{-a(1-D)})}{aD(1-e^{-a})}\right]}. \tag{1}$$

D is the pulse dc duty factor and $a \equiv 1/(f\tau)$, where f is the pulse dc repetition frequency, and τ is the vacancy relaxation time constant which is a function of temperature, material, microstructures, and will be longer at lower temperatures. Fig. 3 shows the frequency dependence of $\mathrm{MTTF}_{\text{pulse-DC}}$ under peak current density of 1.5×10^7 A/cm^2 and duty factor of 50% for electroless Cu and Al–2%Si stripes. The Cu pulse-dc lifetimes are still about two orders of magnitude longer than that of Al–2%Si. The predictions of (1) are also shown in Fig. 3. $\tau = 1.1$ and 20 μs were the only fitting parameters for Cu and Al–2%Si, respectively. The τ for Cu is about 20 × smaller than that for Al–2%Si. Such difference is not surprising considering these are two quite different metals. Fig. 4 shows the experimental results and predictions by (1) of the duty factor dependence of $\mathrm{MTTF}_{\text{pulse-DC}}/\mathrm{MTTF}_{\mathrm{DC}}$ for Cu stripes. We can see that the pulse dc lifetime enhancement varies more rapidly with duty factor at high frequencies and the vacancy relaxation model agrees very well with the experimental data for Cu interconnects.

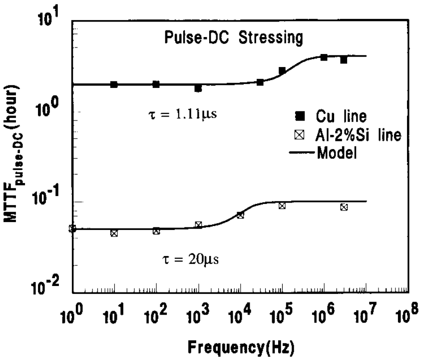


Fig. 3. Plot of pulsed dc lifetime $\mathrm{MTTF}_{\text{pulse-DC}}$ as a function of current repetition frequency for Cu and Al–2%Si stripes under $J_{\text{pulse-DC}} = 1.5 \times 10^7$ A/cm^2 and $T = 275$°C. The predictions by the vacancy relaxation model for Cu and Al–2%Si are also shown in the figure by the solid lines.

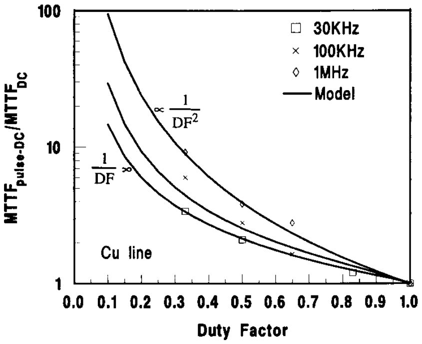


Fig. 4. Plot of normalized $\mathrm{MTTF}_{\text{pulse-DC}}/\mathrm{MTTF}_{\mathrm{DC}}$ as a function of duty factor for Cu stripes under $J_{\text{pulse-DC}} = 1.5 \times 10^7$ A/cm^2 and $T = 275$°C for different current repetition frequencies. The predicted results by the vacancy relaxation model are also shown in the figure by the solid lines.

Fig. 5 shows the log-normal plot of the cumulative failure data for Cu and Al–2%Si stripes under ac, i.e., bipolar stressing conditions. A symmetrical 1-MHz rectangular ac waveform with a peak current density of 1.5×10^7 A/cm^2 and duty factor of 50% was used. The failed Cu and Al–2%Si test stripes were examined by using SEM, and almost all of the ac stress failures were found to occur at the transition region between the metal pad and the metal line. This observation suggests that under ac stressing case, the transition region fails due to the geometrical asymmetry and the thermal gradient at this region, which causes comparable ac lifetimes for Cu and Al–2%Si lines. The ac lifetimes of the metal lines are much longer because of the healing effect of the two opposite flows of vacancy flux. The phenomenon requires further tests at lower current density.

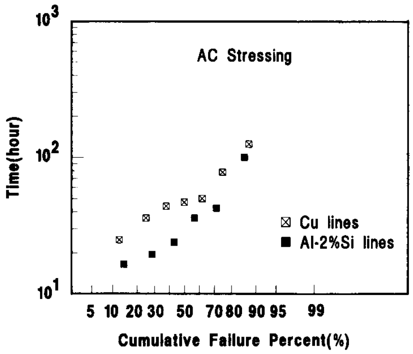


Fig. 5. Log-normal plot of the cumulative failure rate for ac stressing under $J_{AC} = 1.5 \times 10^7$ A/cm^2 and $T = 275°C$ for Cu and Al–2%Si stripes.

IV. CONCLUSION

The characteristics of electroless plated Cu/Pd-silicide interconnects have been studied under constant current and time-varying current stressings. Our results show that under dc and pulse-dc current stressing, the Cu lifetimes are about two orders of magnitude longer than that of Al–2%Si at 275°C, and four orders of magnitude longer than that of Al–2%Si at room temperature using the measured activation energy for extrapolation. Cu pulse-dc lifetime is well predicted by the vacancy relaxation model with a vacancy relaxation time 20 × smaller than that of Al–2%Si. Under bipolar current stressing, the lifetimes of Cu are comparable to the lifetimes of Al–2%Si. As a result, the ratio of $\text{MTTF}_{AC}/\text{MTTF}_{DC}$ for Cu is about 50 versus 2500 for Al–2%Si.

REFERENCES

[1] S. P. Murarka, "Overview of copper technology," in *Tungsten and Other Advanced Metals for ULSI Applications in 1990*, G. C. Smith and R. Blumenthal Eds. Pittsburgh: MRS, 1990, pp. 179–187.

[2] P. L. Pai and C. H. Ting, "Selective electroless copper for VLSI interconnection," *IEEE Electron Device Lett.*, vol. 10, no. 9, pp. 423–425, 1989.

[3] B. K. Liew, N. W. Cheung, and C. Hu, "Projecting interconnect electromigration lifetime for arbitrary current waveforms," *IEEE Trans. Electron Devices*, vol. 37, no. 5, pp. 1343–1351, 1990.

[4] H.-K. Kang, J. S. H. Cho, I. Asano, and S. S. Wong, "Electromigration of electroless and CVD Cu metallization," in *Proc. 9th Int. VLSI Multilevel Interconnection Conf.*, 1992, pp. 337–343.

[5] J. Tao, K. K. Young, N. W. Cheung, and C. Hu, "Comparison of electromigration reliability of tungsten and aluminum vias under DC and time-varying current stressing," in *Proc. 30th Int. Reliability Phys. Symp.*, 1992, pp. 338–343.