# INTERNAL PASSIVATION FOR SUPPRESSION OF DEVICE INSTABILITIES INDUCED BY BACKEND PROCESSES

Vivek Jain, Dipankar Pramanik, Subhash R. Nariani, Chenming Hu*

VLSI Technology Inc.,1109 McKay Drive, MS-02, San Jose, CA 95131.
* Dept. of Electrical Engineering and Computer Sciences, U.C.Berkeley, CA 94720.

## ABSTRACT

The concept of "internal passivation" has been introduced as a means of suppressing device degradation due to backend processes. The proposed concept has been demonstrated by tailoring the composition of a PECVD oxide film to achieve such an internal passivation, resulting in a process with built-in-reliability. Specifically, field inversion and hot carrier degradation induced by backend processing have been suppressed. The results have been duplicated on two different commercially available PECVD systems establishing that neither the problem nor the solution was related to a specific deposition system.

## INTRODUCTION

Topside passivation layers of PECVD oxide and PECVD nitride have commonly been used to protect IC devices from external sources of device degradation such as sodium ions and moisture. However, IC devices are also susceptible to charge buildup, charge trapping and the electric fields induced by the backend processing. Shrinking geometries have led to the increased use of plasma-assisted processes and Spin-On-Glass (SOG) for multilevel interconnect schemes. These can lead to device instability and poor reliability. For example, it has been shown that the use of PECVD plasma silicon nitride for passivation and the Reactive Ion Etch (RIE) of the metal layer can lead to worse hot carrier lifetimes[1,2]. Water absorption in PECVD oxides and SOG results in generation of positive mobile charges[3] with degradation of hot carrier lifetimes[4]. The use of carbon based SOG in Inter Metal Oxide (IMO) leads to field inversion[5]. Generation of mobile positive ion in the BPSG interlevel dielectric resuls in charge loss in EPROMs[6]. These examples clearly show the origins of device degradation that are internal rather than external. We propose the concept of "internal passivation" for suppressing device degradation from such internal sources. The proposed internal passivation/gettering layer would act as an effective barrier against various internal sources of device degradation. Clearly, this approach provides 'built-in-reliability' and has wider applicability than the traditional approach of identifying and eliminating/suppressing the source of each specific degradation.

In this study we have demonstrated that the composition of a PECVD oxide film can be tailored to provide a layer of "internal passivation" that is capable of suppressing device degradation due to backend processes. Specifically, the field inversion due to a carbon-based SOG in the IMO and the hot carrier degradation due to hydrogen from the nitride passivation have been suppressed. In addition, the results have been duplicated on two different commercially available PECVD systems in order to establish that neither the problem nor the solution was related to a specific deposition system. The internal passivation was achieved by modifying the composition of PECVD oxide used for the intermetal oxide. We believe that the modified PECVD oxide film proposed in this study may be effective against other types of backend induced device degradation and is probably similar to that reported by Araki et. al[7] for reducing charge loss in EPROMs.

## EXPERIMENT

Devices were fabricated using a 0.8µm CMOS technology with 165Å gate oxide, polycide gates, LDD structures, and double level metal process. The inter metal oxide (IMO) consisted of 2.5KÅ of a $SiH_4$ based PECVD oxide followed by 2.5KÅ of siloxane (carbon based) SOG. The SOG was capped with 5KÅ of PECVD oxide without any etch back of SOG. The passivation on top of the second metal consisted of two layers of dielectric - 5KÅ PECVD oxide followed by 10KÅ of PECVD nitride. An alloy step at 400°C in forming gas was carried out after passivation. The internal passivation properties were obtained by modifying the deposition conditions and making the oxide in the IMO sandwich silicon-rich. In order to establish that the problem and the solution was not related to a specific deposition system, the results were duplicated on two different commercially available PECVD systems, A and B.

The IMO PECVD oxide film was characterized using FTIR and Electron Paramagnetic Resonance (EPR) in addition to refractive index, stress and wet etch rates. EPR spectra were used to estimate electron spin densities and the associated defect centers.

The effect of the composition of the oxide on its ability to suppress device degradation is measured on field isolation transistors and active area n-channel transistors. The corresponding manifestations of device degradation were field $V_t$ shifts and enhanced hot carrier degradation. Field threshold measurements and the hot carrier lifetime measurements were made after oxide passivation (first layer of passivation film) and repeated after second layer passivation consisting of plasma nitride deposition and a 400°C alloy step. The change in drain current($\Delta I_{ds}$) at $V_{gs}$=5.0V and $V_{ds}$=0.1V and change in threshold voltage of N-MOS transistor were used to measure degradation from hot carrier injection. Typical stress conditions were $V_{ds}$=7.0V and $V_{gs}$=2.0V. The $L_{eff}$ was around 0.55µm for all the hot carrier lifetime measurements.

CH3084-1/92/0000-0011$01.00 © 1992 IEEE/IRPS

## RESULTS AND DISCUSSION

**PECVD oxide film properties:** FTIR spectra were used to obtain the Si-H content in the film. The ratio of the peak heights of the Si-H and the Si-O-Si stretch bands has been defined as %Si-H. Fig 1 shows that the refractive index of the oxide film increases with increase in Si-H content. Stoichiometric PECVD oxide has a RI of 1.45 and nearly zero Si-H content. Silicon rich oxides have higher RI and Si-H content than the stoichiometric oxide. Fig 2 shows the electron spin densities from EPR spectra as a function of Si-H content. Higher spin densities with increasing Si-H indicates that the modified PECVD oxide films have higher dangling bond densities.

**N-field isolation transistor:** The effect of nitride passivation on the threshold voltage of N-field transistor for the various PECVD oxides is shown in fig 3. Clearly, the field thresholds are good prior to nitride passivation for all the processes. The standard stoichiometric PECVD oxide is unable to suppress any device degradation due to nitride passivation and results in shorted field transistors. These can be turned off by applying a negative back bias of 1.5 Volts, as shown in fig 4(a), indicating the presence of positive charge over the field oxide. On the other hand, the modified silicon rich oxide in the IMO results in no $V_t$ shift of the field transistor after the nitride passivation. Fig 4(a) and 4(b) compare the poly N-field transistor I-V characteristics at different back bias for stoichiometric and silicon rich oxides respectively. Rough calculations show that a positive charge density of the order of $1E12/cm^2$ would be required to cause such a field inversion. It has been shown that hydrogen released from the passivation nitride film interacts with carbon in the SOG, which results in the formation of positive charges[4] that lead to field inversion. We propose that the silicon rich oxide provides dangling bonds to neutralize this positive charge formation and thus suppress the parasitic leakage. Fig 5 shows the N-field transistor $V_t$ for various films obtained from two different PECVD systems. Similar trends on two different systems clearly show that the field threshold is affected by the composition of the IMO film and not by the type of deposition system.

**Hot carrier lifetimes:** Hot carrier lifetimes were measured on active n-channnel transistors after oxide passivation and repeated after oxide + nitride passivation. The estimated lifetimes based on a 100mV change in $V_t$ and a 10% change in drain current are shown in fig 6 and fig 7 respectively. The stress conditions were $V_{ds}$=7.0V and $V_{gs}$=2.0V. The plots clearly show that modifying the PECVD oxide film can result in more than an order of magnitiude improvement in hot carrier lifetime even prior to nitride passivation. The silicon-rich oxide films show very little degradation due to nitride passivation while the stoichiometric oxide shows more than an order of magnitude drop in hot carrier lifetime after nitride passivation. Trends in hot carrier lifetime based on $V_t$ change are similar to that based on $I_{ds}$ change and suggest that the hot carrier degradation is due to interface trapping rather than bulk trapping.

In order to investigate hole trapping differences for the stoichiometric oxide and silicon-rich oxide films, N-MOS hot carrier stressing was done at $V_{gs}$=1.0V and $V_{ds}$=7.0V. The threshold voltage change with time is shown in fig 8 for the two oxides. Negative threshold shifts could not be observed for either of the films even at short stress times indicating absense of hole trapping. The change in drain current as a function of threshold voltage change for the two oxides is shown in fig 9. Since the curves for the two oxides fall on top of each other, we can conclude that there is no difference in bulk trapping for the two oxides and the hot carrier degradation for both oxides is due to interface trapping.

These results point to the device interface as the area that is degraded by the backend processing. Furthermore this suggests that some mobile species is diffusing to the gate oxide interface to cause the degradation. The modified PECVD oxide film is preventing the mobile species from getting to the interface and hydrogen is a likely candidate. This hydrogen may come from the backend plasma processes as well as from the silicon nitride passivation. Silicon-rich oxide films have higher dangling bond density than stoichiometric oxide. It is hypothesized that these dangling bonds act as trap centers for the hydrogen or other mobile species and hence result in a better hot carrier performance. Similar results were obtained for the two deposition systems.

**EPR studies:** In order to get a better understanding of the type of defect centers involved in the stoichiometric and the silicon rich films, the EPR spectra were examined in detail. Fig 10(a) and fig 10(b) are representative EPR spectra for stoichiometric and silicon-rich oxide films, respectively, for deposition system A. The g-value (2.001) of the stoichiometric oxide was found to be close to the g-values of the E' and $P_b$ resonances. The g-value of the silicon rich oxide is in the range 2.005 and 2.006 and corresponds to the A and B resonances described by DiMaria et. al[8]. The A-line is attributed to the dangling bonds in an amorphous silicon environment and the B-line is attributed to the dangling bonds at the interface between amorphous silicon and SiO2 components. EPR spectra for system B are shown in fig 11(a) and 11(b) for the stoichiometric and silicon rich oxide, respectively. The g-value of the spectrum of stoichiometric oxide are similar for the two system and the internal passivation properties are non-existent although stoichiometric oxide from system B shows an order of magnitude higher spin densities than that for System A. The spectra for the two system are very similar for the silicon-rich oxides used for the internal passivation. Hence it is important to note that it is the type of defect rather than the total spin densities that are critical to achieve the desired "internal passivation" and the "built-in-reliability".

## CONCLUSIONS

The concept of "internal passivation" has been introduced as a means of suppressing device degradation due to backend processes. The proposed concept has been demonstrated by tailoring the composition of a PECVD oxide film to achieve such an internal passivation, resulting in a process with built-in-reliability. Specifically, field inversion and hot carrier degradation induced by backend processing have been suppressed. The modified silicon-rich oxide has a large number of dangling bonds associated with amorphous silicon like clusters in $SiO_2$ environment. Field inversion is caused by formation of positive charges due to interaction of hydrogen and carbon in SOG. The dangling bonds in silicon-rich oxide neutralize these positive charges and thus suppress the field inversion. These dangling bonds also prevent some mobile species from reaching the gate oxide interface to silicon thereby improving the hot carrier performance. The results have been duplicated on two different commercially available PECVD system establishing that neither the problem nor the solution was related to a specific deposition system.

## ACKNOWLEDGEMENTS

The authors would like to thank the VLSI pilot line for processing the wafers, the TD test lab for device measurements, Charlotte Larin for carrying out various IMO splits and Mohammad Farr for extensive hot carrier and bench measurements.

### REFERENCES


1. M. Chen et. al, "Suppression of hot-carrier effects in submicrometer CMOS technology", IEEE Trans. Elec. Device vol 12, 2210 (1988).
2. S. Yoshida et. al, "Improvement of endurance to hot carrier degradation by hydrogen blocking P-SiO2" Proceedings of IEEE IEDM, 22 (1988).
3. N. Lifshitz, G. Smolinsky, J.M.Andrews, "Mobile charge in a novel spin-on oxide(SOX): detection of hydrogen in dielectrics", J. Electrochem. Soc., vol 136, 1440 (1989).
4. N. Lifshitz, G.Smolinsky, "Hot-carrier aging of MOS transistor in presence of spin-on glass as the interlevel dielectric", IEEE Elec. dev. Lett. vol 12, 140 (1991).
5. D. Pramanik, S. Nariani, G. Spadini, "Field inversion in CMOS double metal circuits due to carbon based SOGs", Proceedings of IEEE VMIC, 454 (1989).
6. G. Crisenza et. al, "Charge loss in EPROM due to ion generation and transport in interlevel dielectric", Proceedings of IEEE IEDM, 107 (1990).
7. H. Araki et. al, "High reliability passivation film for EPROM", Extd. Abs. of ECS spring meeting, 352 (1991).
8. D. J. DiMaria et. al, "Electroluminescence studies in silicon dioxide films containing tiny silicon islands", J. Appl. Phys., vol 56, 401 (1984).

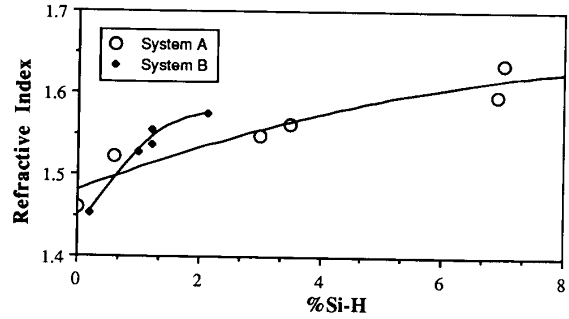




**Fig. 1.** Refractive index as a function of Si-H content for the two systems.

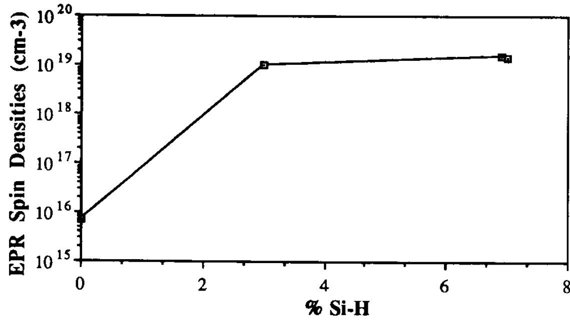



**Fig. 2.** Electron spin densities as a function of Si-H content.

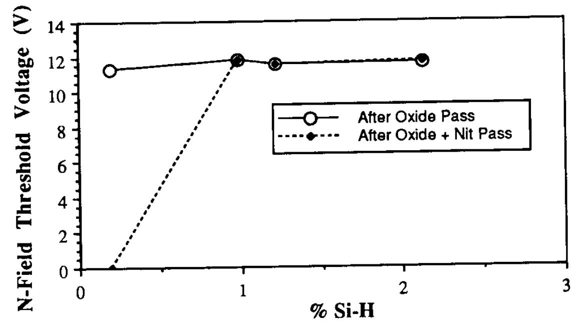
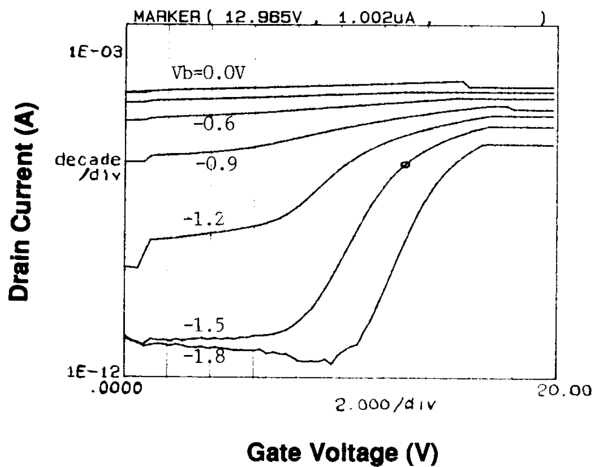
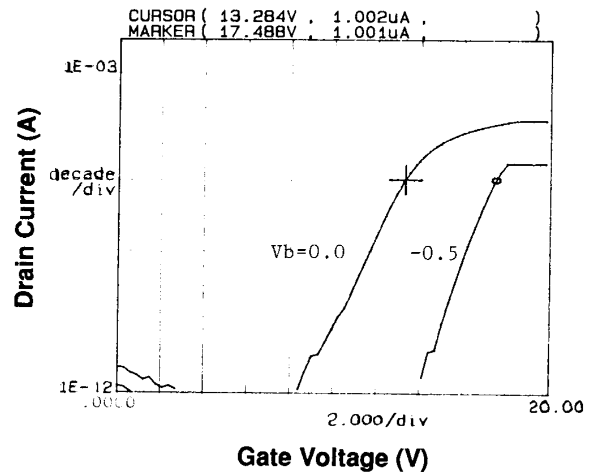



**Fig. 3.** Effect of nitride passivation on poly N-field threshold as a function of Si-H content.




(a)




(b)

**Fig.4.** N-field transistor as a function of back bias voltage at $V_{ds} = 0.1V$ for (a) Stoichiometric oxide and (b) Silicon rich oxide.

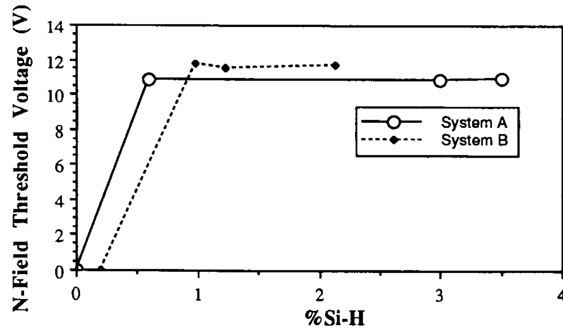



**Fig. 5.** Poly N-field threshold as a function of Si-H content for the two systems after oxide + nitride passivation.

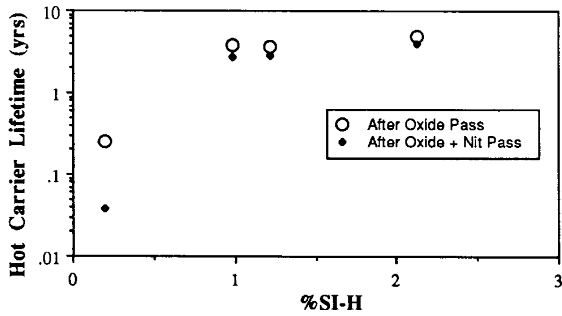



**Fig. 6.** Estimated hot carrier lifetime at $V_{ds}$=5.5V of 0.55µm $L_{eff}$ based on 100mV change in threshold voltage. The stress conditions were $V_{gs}$=2.0V and $V_{ds}$=7.0V.

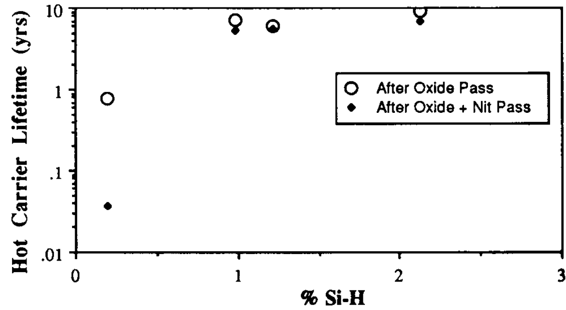



**Fig. 7.** Estimated hot carrier lifetime at $V_{ds}$=5.5V of 0.55µm $L_{eff}$ based on 10% change in drain current. The stress conditions were $V_{gs}$=2.0V and $V_{ds}$=7.0V.

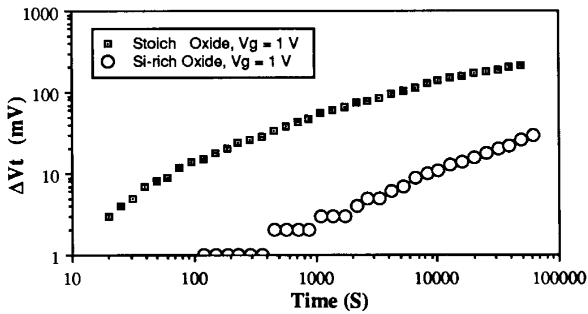



**Fig. 8.** Threshold voltage change as a function of stress time for the two oxides. The stress conditions were $V_{gs}$=1.0V and $V_{ds}$=7.0V and $L_{eff}$=0.55µm.

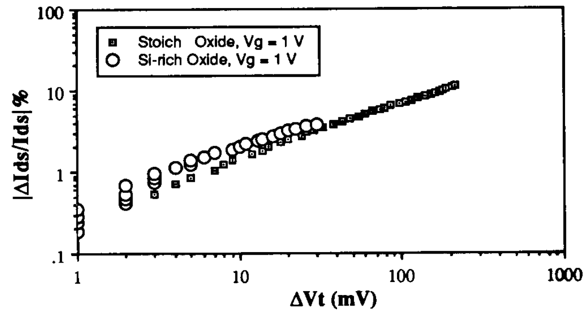
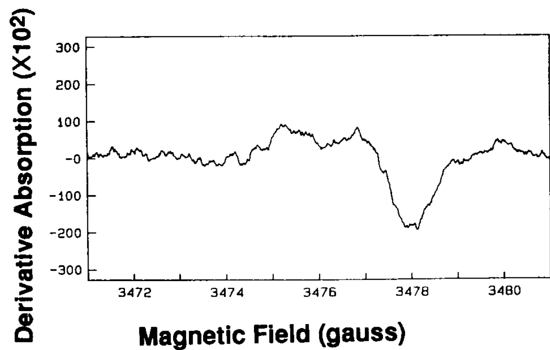
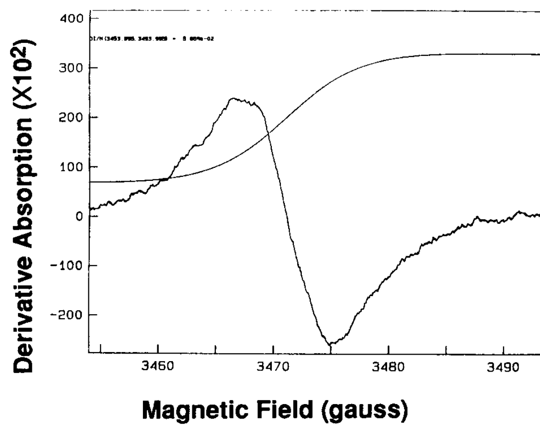



**Fig. 9.** Change in drain current as a function of threshold voltage change for the two oxides. The stress conditions were $V_{gs}$=1.0V and $V_{ds}$=7.0V and $L_{eff}$=0.55µm.

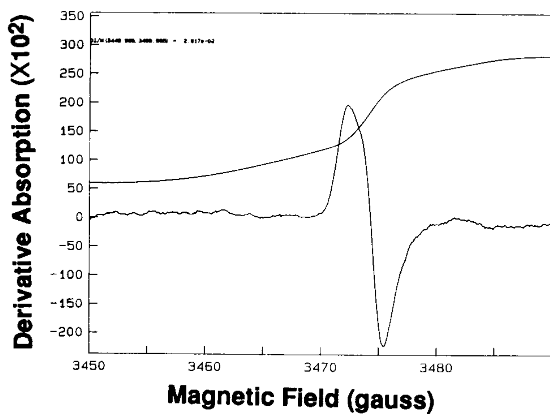



(a)

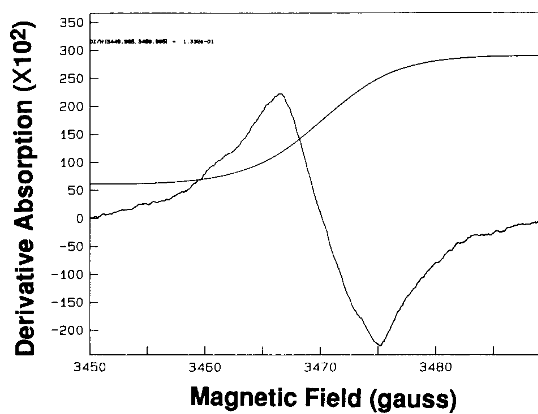



(b)

**Fig. 10.** EPR spectra for system A (a) Stoichiometric oxide (b) Silicon-rich oxide.




(a)




(b)

**Fig. 11.** EPR spectra for system B (a) Stoichiometric oxide (b) Silicon-rich oxide.