

**CHARACTERIZATION OF THIN OXIDE DAMAGE
DURING ALUMINUM ETCHING AND PHOTORESIST ASHING PROCESSES***

*by H. Shin, C.-C. King, R. Moazzami, T. Horiuchi** and C. Hu*

University of California at Berkeley
Department of Electrical Engineering and Computer Sciences
and the Electronics Research Laboratory
Berkeley, California 94720

Abstract

Plasma-induced damage can be simulated and modeled as damage produced by constant voltage electrical stress. These voltage produced by plasma process increases with the "antenna" size of the device structure. Photoresist ashing is capable to degrade oxide integrity even more rapidly than Al etching. However, the stress voltage produced during ashing exhibits a large spread and is randomly distributed across the wafer. CV measurement is shown to be a more sensitive technique for characterizing plasma-etching induced damage than oxide breakdown.

Introduction

Plasma processes have been widely used in VLSI manufacturing for Aluminum etching and photoresist stripping. In the plasma ambient, reactive ions generated in the discharge are accelerated by the self bias voltage and collide with the surface of the wafer. These ions can cause damage to the wafer. Degradation of gate oxides in MOS devices due to the plasma process has been observed and attributed to electrostatic charging during the process^{1,2}.

In the plasma ambient, charges are collected by aluminum pads, which serve as "antennas". The

stress can cause trapped charges in the oxide as well as surface states at SiO₂-Si interface, therefore decrease the breakdown voltage and deform the CV curve of the gate oxide. In this study, we use breakdown voltage and CV to determine the amount of stress during the process.

Experiment

The test structures used are polysilicon-gate MOS capacitors fabricated on n-type (100) silicon substrate with 64Å and 116Å gate oxide grown in dry oxygen at 900°C. After gate definition, 5000Å aluminum was deposited. Aluminum etching was done in Lam Research Autoetch 690B system with a 50% overetch after the detection of endpoints for a total of 60 seconds and the subsequent photoresist ashing was done in a Technics Micro-stripper Series 2000 plasma system for one hour. To characterize the damage during the plasma processes, the oxide integrity was monitored after each step. Changes in the ramp breakdown voltages or quasi-static CV curves after each step are used to determine the stress current(or voltage) produced by each plasma step. Control wafers receiving only wet-etching were also fabricated. If the plasma-induced damage is due to electrostatic charging, the damage to gate oxide should be identical to that produced by applying a constant current(or voltage) to the gate electrode for a duration equal to the process time. The current would correspond to that collected by the antennas.

* This research is sponsored by SRC, Sandia Laboratory and AMD under MICRO program and ISTO/SDIO administered by ONR under Contract N00014-85-K-0603.

** On leave from NEC Corp. Kanagawa, Japan.

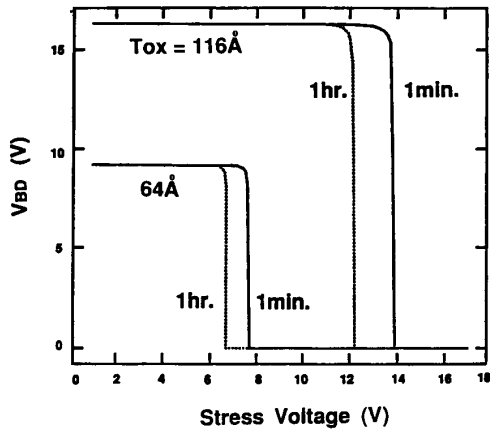


Fig.1. The ramp breakdown voltage after 1 minute or 1 hour electrical stress for oxides of two different thicknesses.

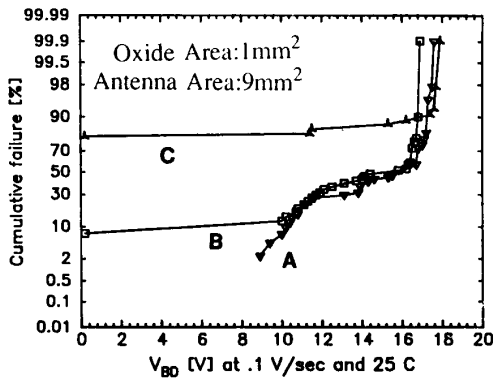


Fig.2. Cumulative failure vs. breakdown voltage for 116Å capacitors with area= 1mm \times 1mm under different processing conditions. A: control wafer, B: plasma Al etching for 100 seconds with power=250 watts, C: condition B + plasma PR ashing for 1 hour.

Breakdown Voltage Studies

Fig. 1 plots the effect of voltage stressing on the breakdown voltage⁶. Fig. 2 shows the ramp breakdown voltage distribution of large capacitors (1mm²) with 9mm² metal pads after etching and ashing steps. Oxides with initial breakdown voltage less than 10V became shorts after Al etching(B), suggesting that about 7 volts was produced by Al etching⁶. Similarly curve C suggests that about 11

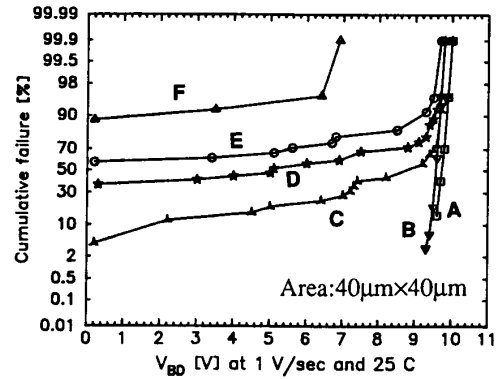


Fig.3. Cumulative failure vs. breakdown voltage for 64Å capacitors with area= 40µm \times 40µm under different processing conditions and ratios of Al area to oxide area (R). A: control wafer, B: plasma Al etching for 100 seconds with power=250 watts, R=300, C: condition B + plasma PR ashing for 1 hour, R=10, D: same as C, R=30, E: same as C, R=50, F: same as C, R=100.

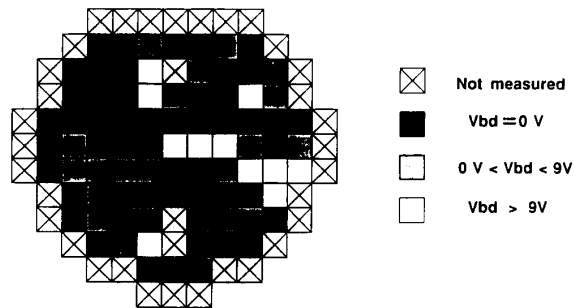


Fig.4. Distribution of breakdown voltage for 64Å capacitors with area= 40µm \times 40µm, R=50, over the wafer.

volts was produced by plasma ashing. The breakdown statistics of intrinsic(very small area) capacitors were measured to investigate the effect of different metal areas to oxide area ratios(antenna effect) and the spatial uniformity of the process induced stress voltage. Fig. 3 shows that there is very little change in the intrinsic breakdown strength for oxides subjected to Al plasma etching only(B). However, plasma ashing causes significant reduction in breakdown strength even for intrinsic oxides. Capacitors with larger metal pads have higher failure

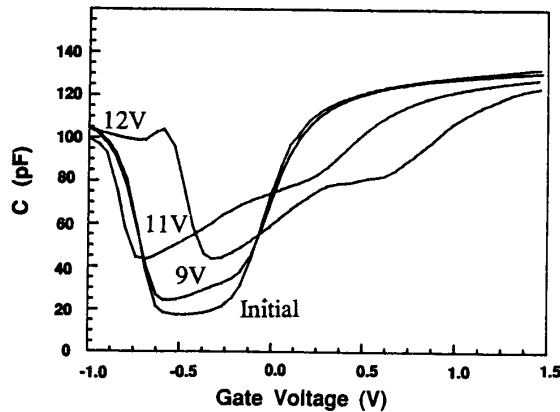


Fig. 5. The quasi-static C-V curves for 116Å capacitors after 1 hour constant voltage stressing.

rates as expected. However, the plasma-induced stress voltage varies over that range between less than 5 volts to larger than 8 volts for a given metal to oxide area ratio as extracted from the large variation in breakdown voltage for small area capacitors after processing shown in Fig. 3. This variation has never been reported before. This non-uniformity is fairly random (as opposed to radially distributed, for example), as shown in Fig. 4.

CV Studies

Changes in the breakdown voltage can be clearly measured only when the process-induced problem is very severe and using large-area oxide samples (thus making it difficult to study large antenna-to-oxide ratios) and large number of test devices. Even then it cannot give high resolution in quantitative study. Accurate estimation of the amount of charge collection can be obtained by comparing the CV curves of MOS capacitors after plasma process with control devices after electrical stress. Fig. 5 shows the effect of the voltage stressing on CV curve. Fig. 6 shows the quasi-static CV characteristics of capacitors after various processing steps. The difference between the control wafer and the one after aluminum etching is very small, while the CV curve changes dramatically after photoresist ashing. The photoresist ashing process causes much more damage than the etching step. Comparison

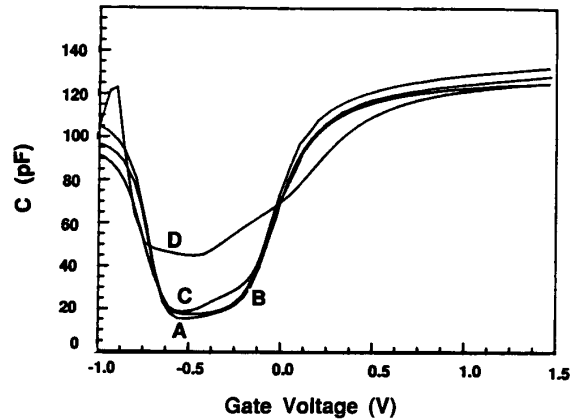


Fig. 6. The quasi-static C-V curves for the same test structure as used in Fig. 2 under different processing conditions. A: control wafer (Al wet-etched), B: plasma Al etching for 100 seconds with power=250 watts, C: plasma Al etching for 60 seconds with power=500 watts, and D: condition B + plasma PR ashing for 1 hour.

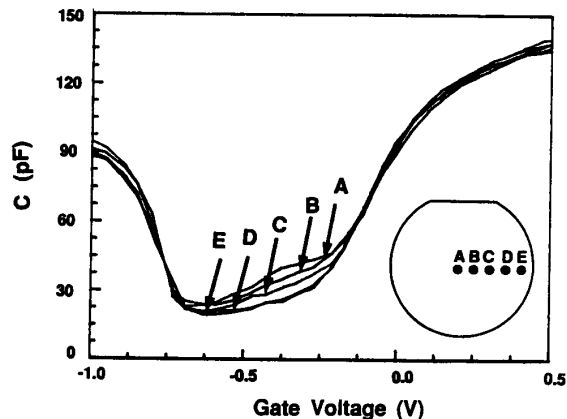


Fig. 7. The quasi-static C-V curves for 116Å capacitors after 60 seconds plasma Al etching for five different positions on a wafer.

between Fig. 6 and Fig. 5 confirms that about 11V was produced by photoresist ashing and 7V by Al etching. Also note that the plasma-induced damage during Al etch step is not uniform across the wafer as shown in Fig. 7. More damage is observed near the center of the wafer.

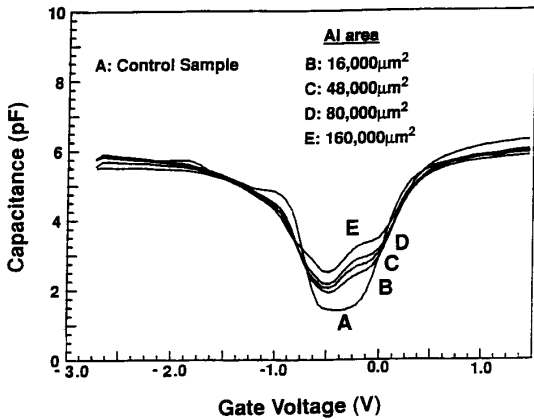


Fig. 8. $1,600\mu\text{m}^2$, 116\AA oxide CV after 60 second plasma etching of Al. Curve A is the CV of wet etched samples.

Fig. 8 shows the quasi-static CV curves for MOS capacitors with different aluminum pad sizes after pad capacitances were subtracted. The size of the capacitors is $1,600\mu\text{m}^2$ with identical layout except for the size of aluminum pads ranges from $16,000$ to $160,000\mu\text{m}^2$. The CV curve for wet-etched capacitor is also shown as curve A. Because larger aluminum pad collects more charge during the etching, the CV curve of capacitors with larger pads show higher degree of degradation. The differences in breakdown voltage and charge to breakdown between A and E are within the ranges of sample to sample random variations (Fig. 1). Clearly, CV degradation is a more sensitive technique suitable for process monitor and for quantitative study of the charging process.

Summary

Photoresist ashing is capable to degrade oxide integrity even more rapidly than Al etching. Plasma-induced damage can be simulated and modeled as damage produced by constant voltage electrical stress. These voltage produced by plasma process increases with the antenna size of the device structure. However, the stress voltage during ashing step exhibits an unexpectedly large spread and is randomly distributed across the wafer. Plasma etch-

ing of Al is shown to produce severe distortions in the oxide CV characteristics, from which one can easily deduce the equivalent voltage during etching. A clear radial variation of stressing is found for plasma etching process.

REFERENCES

- [1] I.-W. Wu, R.H. Bruce, G.B. Anderson, M. Koyanagi, and T.Y. Huang, "Damage to gate oxides in reactive ion etching," *Proc. SPIE*, vol. 1185, pp. 284-295, 1989.
- [2] Y. Kawamoto, "MOS gate insulator breakdown caused by exposure to plasma," *Proc. 1985 Dry Process Symp.*, The Inst. Elect. Eng. of Japan, pp. 132-137, Oct. 1985.
- [3] Tsunokuni et al., "The effect of charge build-up on gate oxide breakdown during dry etching," *Solid State Devices and Materials*, Tokyo, pp. 195-198, 1987.
- [4] F. Shone, K. Wu, J. Shaw, E. Hokelet, S. Mittal, and A. Haranahalli, "Gate oxide charging and its elimination for metal antenna capacitor and transistor in VLSI CMOS double layer metal technology," *Sym. VLSI Tech. Dig. papers*, pp. 73-74, 1989.
- [5] C. Gabriel and J. C. Mitchener, "Reduced device damage using an ozone based photoresist removal process," *Proc. SPIE*, vol. 1086, pp. 598-603, 1989.
- [6] R. Moazzami and C. Hu, "Projecting Gate Oxide Reliability and Optimizing Reliability Screens," *IEEE Trans. Electron Devices*, vol. ED-37, no. 7, p 1643, Jul. 1990.