P–MOSFET GATE CURRENT AND DEVICE DEGRADATION

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Abstract

Hot-carrier-limited device lifetime of surface-channel p-MOSFETs is found to correlate well with gate current over a wide range of bias. The same result is not observed for buried-channel p-MOSFETs. A gate current model for surface-channel p-MOSFETs is presented. Using this gate current model, reasonable estimates of AC (pulse) stress lifetime can be made based on DC stress data.

Introduction

Most of the studies about hot-carrier effects concentrated on n-MOSFETs rather than p-MOSFETs simply because hot-carrier-induced problems are more serious in n-MOSFETs due to the longer mean-free path, hence higher energy of electrons. For example, peak substrate current in n-MOSFETs is about 3 to 4 orders larger than in p-MOSFETs. In near-micrometer CMOS integrated circuits, n-MOSFETs are known to fail earlier than p-MOSFETs.

Hot-carrier-induced degradation in MOSFETs is usually characterized with a device lifetime defined as the time required to reach a certain level of degradation. For n-MOSFETs, I_{SUB} (or $\frac{I_{SUB}}{I_D}$) is a well-accepted monitor for hot-carrier-induced degradation, such as ΔV_t, ΔG_m and $\frac{\Delta I_D}{I_D}$. Device lifetime of an n-MOSFET does not appear to have a distinct correlation with gate current. For the device lifetime of a p-MOSFET, different authors have reported a correlation with I_{SUB} [1,2] or I_G [3,4]. However, the empirical relationship between p-MOSFET DC lifetime and lifetime monitor is usually obtained over narrow V_G ranges, for example V_G near the peak of I_{SUB} or I_G, and may not be suitable for lifetime modeling for arbitrary stressing waveforms. A general expression which can well describe device degradation over a wide range of bias is thus required. In the following, hot-carrier-induced degradation and gate current model in SC p-MOSFETs are presented. The lifetime of a SC p-MOSFET is found to correlate with I_G over a wide range of V_G. Using this correlation and a gate current model based on lucky electron approach, lifetime of a SC p-MOSFET under pulse stress can be estimated.

Test devices are non-LDD MOSFETs. Both surface-channel (SC) and buried-channel (BC) p-MOSFETs are studied. The SC p-MOSFETs are n^+ polysilicon-gate MOSFETs fabricated on n-type substrate without threshold adjust implant. The substrate doping is $4\times10^{16}cm^{-3}$. The BC p-MOSFETs are also n^+ polysilicon-gate MOSFETs but fabricated with n-well CMOS technology and with channel and punch-through implants performed to achieve desired threshold and punch-through voltages.

Lifetime Monitor

Figures 1(a) and 1(b) show the device lifetime, τ, vs. I_G and I_{SUB} for SC p-MOSFETs with 432 Å and 160 Å gate oxides respectively. τ is defined as the time at which $\frac{\Delta I_D}{I_D}$ (V_G=-5V, V_D=-0.2V) reaches certain percentage (2-4%). Devices were stressed with fixed V_D and varying V_G. In both cases, the correlation can be expressed as $\tau \propto I_G^{\ m}$ with m=1.5. The correlation of τ with I_{SUB} needs to be fitted with two lines, one for high V_G's and one for low V_G's. For the BC p-MOSFETs, the correlation with I_G or I_{SUB} is V_G dependent as shown in Fig. 1(c).

During stress, the time dependences of I_D, I_{SUB} and I_G were also recorded. The gate currents always show a rapid decay within the first 1 or 2 minutes, then gradually settle down. So do the substrate currents, but the relative rates of decrease are much smaller. The gate currents and substrate currents in Figs. 1(a)-(c) are the values recorded at $t \approx 0$. The decreases of I_G and I_{SUB} are caused by trapped electrons in the oxide, which decrease V_t and therefore the channel field[5].

ΔI_D, ΔG_m, and ΔV_t of p-MOSFETs are always positive for the stress conditions in Figs. 1(a)-(c). In n-MOSFETs, ΔV_t is observed to be positive as well but the transconductance change is negative after stress. These results indicate the presence of trapped negative charges in both cases. The negative charges can be trapped electrons in the oxide and/or acceptor type interface traps. The acceptor type interface traps are negatively charged when occupied by electrons and neutral when

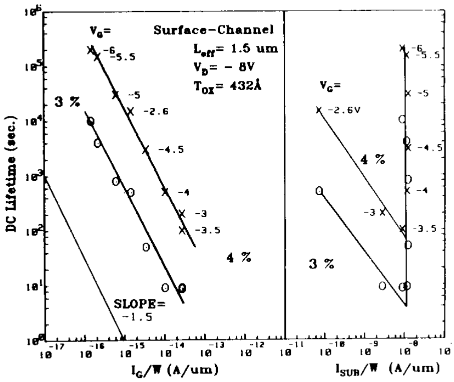


Fig. 1(a) — Lifetime vs. I_{SUB} and I_G for 432Å SC p-MOSFETs stressed with V_D = -8V and varying V_G. Lifetime is defined for $\frac{\Delta I_D}{I_D}$ = 3% or 4%.

unoccupied. In n-MOSFETs, the electron density is high, causing the acceptor type interface traps to be occupied and negatively charged. Therefore, degradation of n-MOSFETs can be caused by both trapped electrons in the oxide and acceptor type interface traps. In p-MOSFET channel, the electron density is very small, most of the acceptor type interface traps are neutral and have no effects on V_t and I_D. This explains the observation that a large density of hot-carrier-generated interface traps, determined by charge pumping technique, are not accompanied by ΔV_t and ΔI_D [6]. As a consequence, the changes of V_t and I_D are mainly due to trapped electrons in the oxide.

Gate Current Model

Since gate current is a better monitor than substrate current for device degradation in p-MOSFETs, modeling of gate current is therefore important. Unlike n-MOSFETs, p-MOSFETs exhibit the largest gate current when biased in the saturation region at low V_G. The gate current of p-MOSFETs results from electron rather than hole injection into the oxide because electrons have a longer mean free path. Also, the $Si-SiO_2$ barrier height is lower for electrons and the vertical field at low V_G favors electron injection. Since p-MOSFETs can take twice as large channel field as n-MOSFETs before breakdown[5], electron gate current can be higher in p-MOSFETs than in n-MOSFETs despite that the number of electrons in p-MOSFETs, created by impact ionization, is several orders of magnitude smaller than in n-MOSFETs. Based on the lucky electron model[7], an electron in the channel will eventually reach the gate if (1) it can acquire enough energy from the channel field to surmount the $Si-SiO_2$ energy barrier, and (2) it does not suffer an energy-stripping collision in silicon bulk and in the "image potential well" where the oxide field opposes the injection of electrons. Since the source of electrons in p-MOSFETs is from impact-ionization process which produces electron current I_{SUB}, the gate current can be expressed as[7],

$$I_G \approx 0.5 \frac{I_{SUB} T_{ox}}{\lambda_r} \left(\frac{\lambda E_m}{\Phi_b} \right)^2 P(E_{ox})\, exp\left(\frac{\Phi_b}{E_m \lambda} \right) \quad (1)$$

$\frac{P(E_{ox})}{\lambda_r}$ is the lumped probability that an electron does not suffer an energy-stripping collision per unit length in the silicon bulk and the oxide. The same expression of $P(E_{ox})$ as in [7] is used. λ_r=616Å is the re-direction scattering mean free path and $exp\left(\frac{\Phi_b}{E_m \lambda} \right)$ is the probability that an electron possesses energy larger than Φ_b in a field of E_m. λ=105Å is the scattering mean free path of electron. $\Phi_b = 3.2 - 2.6\times10^{-4}\sqrt{E_{ox}} - 4\times10^{-5} E_{ox}{}^{2/3}$ (in V) is the $Si-SiO_2$ barrier height considering image force barrier lowering and electron tunneling[8]. $E_{ox} = \frac{V_G - V_D - V_{FB}}{T_{ox}}$ with V_{FB} being the flat-band voltage. Eq.(1) differs from the n-MOSFET I_G expression[7] only in I_{SUB} replacing I_D. I_{SUB} and E_m can be calculated using the model described in [5]. I_G's predicted by (1) are shown in Fig. 2. The reasonable agreement between the measurement data and calculated values demonstrates the validity of lucky electron model in SC p-MOSFETs. BC p-MOSFETs, on the other hand, often exhibit higher gate current than SC devices of the same size[6]. This is due to the difference in flat band voltage. The difference in I_G thus favors p^+ poly-gate or metal-gate SC p-MOSFETs over n^+ poly-gate BC devices for hot-carrier reliability. Another advantage of p^+ poly-gate p-MOSFETs is the smaller off-state drain leakage current due to band-to-band tunneling[9].

Notice that as the channel field in a p-MOSFET increases, E_{ox} also increases and hence Φ_b decreases. This implies large electron injection in p-MOSFETs. Fig. 3 shows I_{SUB} and I_G of an n-MOSFET and a p-MOSFET (both are n^+

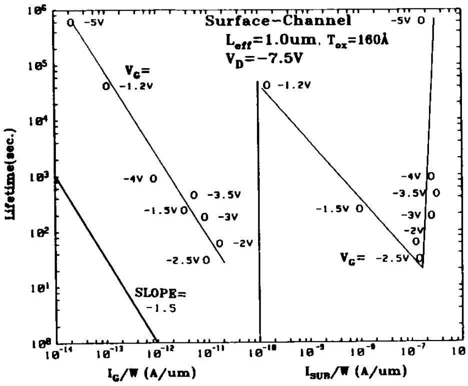


Fig. 1(b) — Lifetime vs. I_{SUB} and I_G for 160Å SC p-MOSFETs stressed with V_D = -8.5V and varying V_G. Lifetime is defined for $\frac{\Delta I_D}{I_D}$ = 2%.

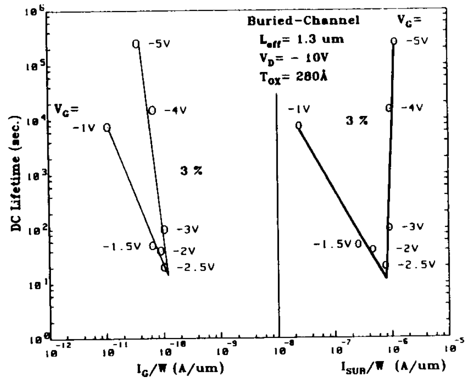


Fig. 1(c) — Lifetime vs. I_{SUB} and I_G for 280Å BC p-MOSFETs stressed with V_D = -10V and varying V_G. Lifetime is defined for $\frac{\Delta I_D}{I_D}$ = 3%.

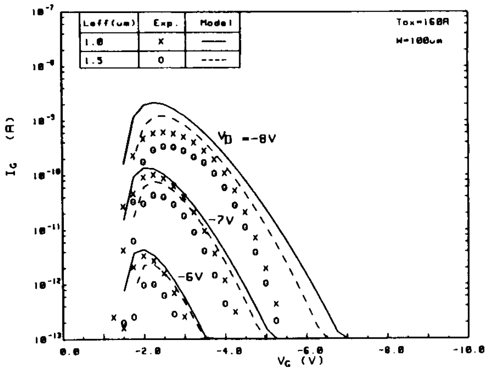


Fig. 2 — I_G vs. V_G for a 160Å SC p-MOSFET.

poly-gates). The devices are fabricated on the same substrate using an n-well CMOS technology. As can be seen, at the same V_D, the peak I_{SUB} of p-MOSFET is about 2 orders smaller than that of n-MOSFET because hole temperature is much lower than electron temperature due to $\lambda_e > \lambda_h$. However, the peak I_G of BC MOSFET is larger than that of SC n-MOSFET by about 1 order.

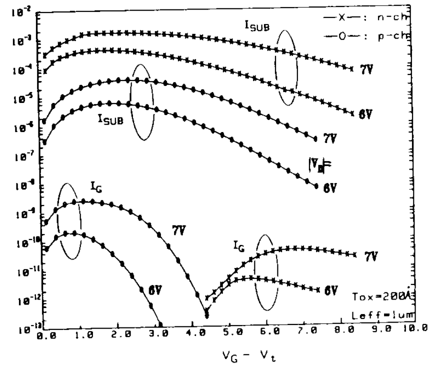


Fig. 3 — I_G and I_{SUB} of an n-MOSFET and a BC p-MOSFET. T_{ox} = 200Å. $|V_D|$= 6V and 7V.

Pulse Stress

Significant difference between AC (pulse) and DC hot-carrier stress results has been reported for n-MOSFETs[10,11]. AC stress creates more, or at least equal, damage than DC stress[10-13]. The mechanism for the extra damage under AC stress is still not well understood. A proposed mechanism is the interaction between trapped holes and hot electrons[10,14].

Fig. 4(a) shows ΔV_t and $\frac{\Delta I_D}{I_D}$ of an n-MOSFET under low-high V_G stressing. The device was stressed with low V_G and high V_G alternately for 4 cycles. As can be seen, degradation rate is enhanced after each low V_G stress. Since hole gate current has been observed in n-MOSFETs at low V_G[15], the enhancement in degradation is believed to be caused by the interaction between holes and electrons. Hole injection can lead to trapped holes in the oxide. Once these trapped holes recombine with electrons(injected during high V_G stress), interface traps and/or neutral electron traps[16-18] can be generated and degradation is aggravated. In p-MOSFETs, however, high V_G stress (favoring hole injection) followed by low V_G stress (favoring electron injection) does not produce the same result as shown in Fig. 4(b). ΔV_t and $\frac{\Delta I_D}{I_D}$ become saturated as the high-low V_G stress proceeds. The difference between n- and p-MOSFETs may be due to that hole injection in p-MOSFETs at high V_G is much smaller than n-MOSFETs at low V_G. No measurable hole gate current has been reported for p-MOSFETs under any bias condition so far. Therefore, no additional neutral traps and/or interface traps are created, and ΔV_t and $\frac{\Delta I_D}{I_D}$ are not enhanced in p-MOSFETs. This eliminates a possible cause of enhanced AC degradation in p-MOSFETs.

The lifetime under DC stress, τ_{DC}, can be expressed as

$$\tau_{DC} = B\, I_G^{-m}\,, \tag{2}$$

where B is a constant and m(=1.5) is the slope of the line in Fig. 1(a). The lifetime under AC stress is then calculated by[19]

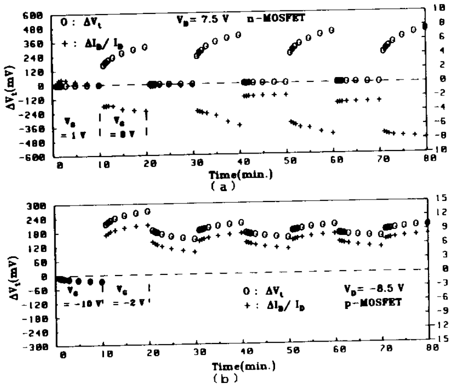


Fig. 4(a) — $\frac{\Delta I_D}{I_D}$ and ΔV_t of an n-MOSFET after repeated low-high V_G(1V and 8V) stressings. T_{ox} = 200 Å, L_{eff} = 1.25 μm.

Fig. 4(b) — $\frac{\Delta I_D}{I_D}$ and ΔV_t of a p-MOSFET after repeated high-low V_G (-10V and -2V) stressings. T_{ox} = 160 Å, L_{eff} = 0.8 μm.

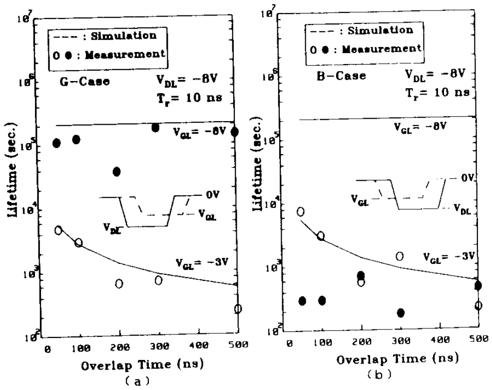
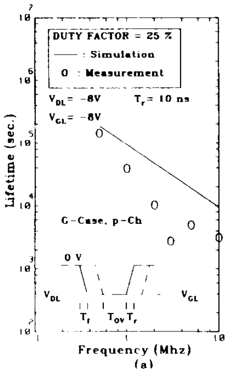


Fig. 5(a) — Lifetime calculated from eq. (7) for the good-case or G-case (inverter-like) waveform. $\frac{\Delta I_D}{I_D}$ = 4% for the lifetime definition. $T_r = T_f$. (b) — Lifetime calculated from eq. (7) for the bad-case (B-case) waveform. $\frac{\Delta I_D}{I_D}$ = 4% for the lifetime definition. $T_r = T_f$. Open symbols for V_{GL}=-3V, closed symbols for V_{GL}=-8V. Frequency is 1 MHz.

$$\tau_{AC} = \frac{T}{\int_0^T B^{-1}\,(\,I_G\,(t)\,)^{\,m}\,dt}\,, \tag{3}$$

where T is the period, $I_G\,(t)$ is the gate current at t (t ≤T). $I_G\,(t)$ can be calculated from (1). τ_{AC}'s (at $\frac{\Delta I_D}{I_D}$ = 4%) thus calculated are shown in Figs. 5(a) and (b) for V_{GL} = -3 V and



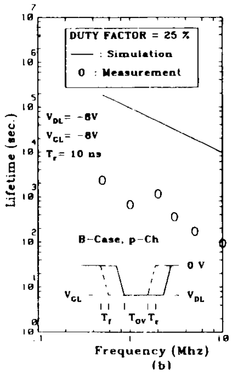


Fig. 6(a) — Calculated lifetime for inverter-like waveform. Duty cycle is the ratio of T_{ov} to the period of the pulse. $\Delta I_D / I_D$=4% for the lifetime definition. $T_r = T_f$. T_{ox}=432Å.

Fig. 6(b) — Calculated lifetime for B-case waveform. Duty cycle is the ratio of T_{ov} to the period of the pulse. $\Delta I_D / I_D$=4% for the lifetime definition. $T_r = T_f$. T_{ox}=432Å.

-8 V. The calculated lifetimes agree with measured data very well except for the B-case (bad-case) waveform at V_{GL} = -8 V. Figs. 6(a) and (b) show AC lifetime vs. frequency for the G- and B-case waveforms at V_{GL} = -8V. For the G-case waveform (good-case), eq.(3) gives reasonable agreement with measurement data for frequency up to 10 MHz. However, the measured AC lifetimes are always shorter than the prediction by eq.(3) for the B-case waveform with the same range of frequency. An explanation for the extra degradation under the B-case waveform for n-MOSFETs is the existence of an excess substrate current generated during V_G turn-off transient in the presence of high V_D [20]. The same explanation is applicable to p-MOSFETs. The average drain and substrate currents shown in Fig. 7 are varied by varying the overlap time. Ordinarily, one would expect I_{SUB} to be proportional to I_D because both are proportional to the overlap time. This is indeed true for the G-case (good-case) waveform in Fig. 7. The B-case, however, exhibits an excess substrate current, ΔI_{SUB}. Through (1), excess substrate current results in excess gate current and therefore extra degradation. This extra component of I_{SUB} is believed to be due to the discharge of stored channel charge through the very high field region at drain during V_G turn-off transient (low V_G results in low V_{DSAT} and therefore high V_D - V_{DSAT}) in the presence of large V_D.

Notice that even for the bad-case, the excess substrate current would only contribute a small additional degradation if V_{GL} = -3V because most of degradation occurs during T_{ov} when V_G=V_{GL} and only a small amount of channel charge is stored and discharged. This is evident in Fig. 5(b). While for the high V_{GL} case, little degradation occurs during T_{ov} yet a large amount of excess hot carriers are produced during the V_G turn-off transient. As a result, τ_{AC} can be orders of magnitude smaller than the quasi-static model (eq.(3)) would predict as shown in Fig. 5(b). Fortunately, the bad-case waveform is rarely encountered in inverter or transmission gate circuits. Therefore, predicting pulse stress p-MOSFET lifetime from DC stress data should be valid at least below 10 MHz of frequency.

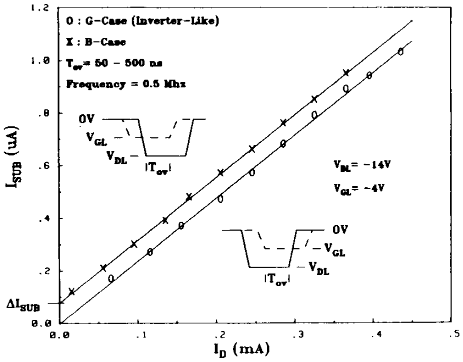


Fig. 7 — Average substrate current vs. average drain current with the gate-drain overlap time, T_{ov}, as a parameter. Data are obtained by varying T_{ov} from 50 ns to 500 ns. Excess substrate current is attributed to the V_G turn-off transient in the presence of high V_D.

Conclusions

Hot-carrier-induced device instability in p-MOSFETs is caused by electron trapping in the oxide. Device lifetime shows a -1.5 power law dependence on I_G for surface-channel (SC) p-MOSFETs. Buried-channel p-MOSFETs do not exhibit a simple τ–I_G correlation. Correlation between lifetime and I_{SUB} is poor. I_G model derived and proven for n-MOSFETs also applies to SC p-MOSFETs with I_D (source of electrons in n-MOSFETs) being replaced by I_{SUB} (source of electrons in p-MOSFETs).

Degradation of p-MOSFETs stressed with inverter-like waveforms can be estimated from DC stress data and a quasi-static model. For the AC stressing waveforms with V_G turn-off transient in the presence of high V_D, more degradation than predicted by the quasi-static model is observed. This extra degradation in p-MOSFETs is probably caused by the excess substrate current (hot carriers) generated by the discharge of stored channel charge through the high field region during V_G turn-off transient.

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