GATE-INDUCED DRAIN LEAKAGE IN LDD AND FULLY-OVERLAPPED LDD MOSFETs

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INTRODUCTION

Gate-Induced Drain Leakage (GIDL), caused by band-to-band tunneling in the gate-overlap region of the drain, has been shown to impose a major constraint on the design of thin-oxide MOSFETs[1,2]. This off-state leakage is especially troublesome for low-power and long-retention applications, such as DRAMs. Because the tunneling current is exponentially dependent on the electric field, even small changes in the drain doping profile or oxide thickness can substantially affect the GIDL current. Indeed, GIDL has exhibited several orders of magnitude variation for different drain designs[3,4,5].

Simple, analytical models for the vertical field in the overlap region have been applied to both single-diffusion (SD) and LDD devices[1,2,4,6]. However, these 1-D models are unable to explain the magnitude of GIDL reduction observed in LDD devices as compared with SD devices. Furthermore, they cannot explain the "inverse" dependence of GIDL on n- concentration which has been observed in fully-overlapped LDD devices, such as TOPS[3]. This paper describes the sensitivities of GIDL to LDD design parameters, and utilizes a new, analytical 2-D model to explain the results.

EXPERIMENT

Three types of drain structures were fabricated: Arsenic n+ (SD), non-overlapped Phosphorus n- (LDD), and fully-overlapped Phos n-/As n+ (TOPS), as shown in Fig.1. In addition, oxide thicknesses of 8.5 and 11nm, n- doses of 3, 6, and $12x10^{13}/cm^2$, and n- spacer lengths of 150 and 250nm were fabricated. Typical sub-threshold characteristics for the three device types are shown in Fig.2. Fig.3 shows the Id-Vd characteristics measured with the gate grounded and source floating. At a leakage criterion of 0.1pA/um, the TOPS device exhibits a 1.7V improvement in Vdg over the SD device, while the LDD device shows a 3.0V improvement.

MODEL

The band-to-band tunneling current is modelled by:

$$I_d/W = AE_{TOT}^2 \exp(-B/E_{TOT})$$

In order to extract the parameters A and B, the experimental data is typically plotted as shown in Fig.4, where the slope equals $-3BT_{OX}$. Even though these devices all have the same T_{OX}, the slopes in Fig.4 are not equal. This is explained by the large built-in lateral field at the abrupt n+ arsenic junction, which is overlapped by the gate in the SD and TOPS devices, but not in the LDD devices. This lateral field is modelled as the gradient of the surface potential along the drain profile. Assuming uniform N_D in the x dimension, it is given by:

$$E_{LAT} = G\psi_s \frac{V_{dg}-\psi_s}{V_{dg}+\psi_s}$$

$$G = \frac{d(\ln N_D(y))}{dy}$$

At V_{dg}=5V, the lateral field can be as large as 2MV/cm for very shallow arsenic junctions. The vertical field is given by:

$$E_{VERT} = \frac{\varepsilon_{OX}}{\varepsilon_S}\frac{V_{dg}-\psi_s}{T_{OX}}$$

The lateral field is vectorially added to the vertical field, thus increasing the GIDL current:

$$E_{TOT} = \sqrt{E_{VERT}^2+E_{LAT}^2}$$

The data of Fig.4 is replotted in Fig.5, using this new model. Since the lateral field for the non-overlapped LDD device is negligible, its slope was used to extract a value for B of 36MV/cm, which is larger than previously reported[1,2]. Using this value for B, lateral gradients of $G=2x10^5$ and $G=2.3x10^6/cm$ were obtained for the TOPS and SD devices, respectively. The new model fits the experimental results for all three drain structures over a wide current range, as shown in Fig.3.

LDD DESIGN SENSITIVITIES

The sensitivity of GIDL to LDD design parameters is measured by the drain-to-gate voltage which the device can sustain at a leakage current of 0.1pA/um. The experimental results for the various oxide thicknesses, spacer lengths, n- doses and drain structures are shown in Fig.6. All devices exhibit a 1.0-1.4V reduction in sustainable V_{dg} when T_{OX} is reduced from 11 to 8.5nm, due to increased vertical field in the overlap region. The TOPS devices exhibit lower GIDL current for the 250nm n- spacer length. This is due to a reduction in the lateral field for the longer n- drain, which is characterized by a gradual n- phosphorus gradient instead of the abrupt n+ arsenic gradient.

As shown in Fig.7, the LDD devices exhibit the expected increase in GIDL current (decrease in sustainable V_{dg}) as the n- concentration is increased, again due to increased vertical field. The TOPS devices, however, exhibit an inverse dependence on the n- concentration. This result is only possible if the total field decreases with increasing n- concentration. The new model is used to calculate the vertical and lateral field components for both TOPS and LDD devices in Fig.8. As the n- concentration is increased, the TOPS arsenic n+ lateral gradient decreases sharply while the phosphorus n- gradient increases very slowly, due to its larger diffusion length. Thus, the total field is dominated by the lateral component for TOPS, and the vertical component for LDD devices.

SUMMARY

LDD devices exhibit substantial reductions in GIDL current as compared with the conventional SD device. The fully-overlapped LDD structure can exhibit low GIDL approaching that of the non-overlapped LDD as the n- concentration is increased toward $1x10^{19}/cm^3$. A longer n- spacer also helps reduce GIDL in the fully-overlapped devices. These GIDL design constraints must be weighed against the hot-electron reliability and device performance constraints in order to optimize the drain design.

ACKNOWLEDGMENTS

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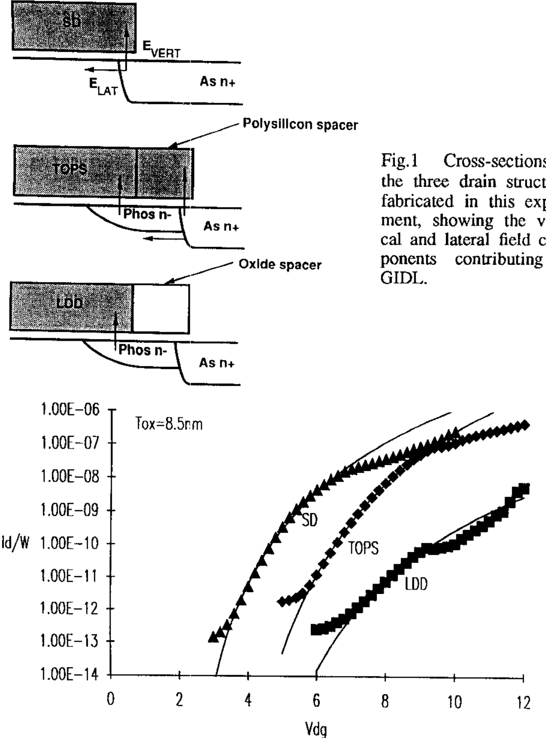

Fig.1 Cross-sections of the three drain structures fabricated in this experiment, showing the vertical and lateral field components contributing to GIDL.

Fig.3 Drain leakage current characteristics of SD, TOPS, and LDD devices, measured with the gate grounded. The solid curves are modelling results, showing an excellent fit.

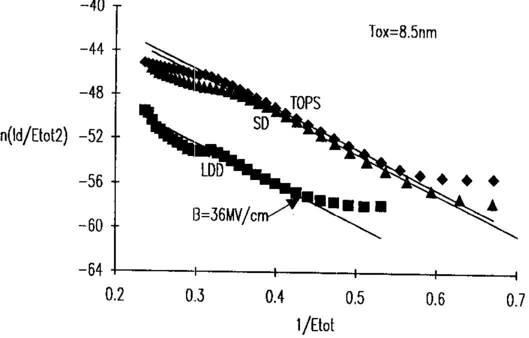

Fig.5 The tunneling characteristics of Fig.4 which have been plotted for E_{TOT} instead of V_{dg}, using the new model. B=36MV/cm is extracted from the LDD slope, and values of G=2x10^5 and G=2.3x10^6/cm are used to fit the TOPS and SD data, respectively.

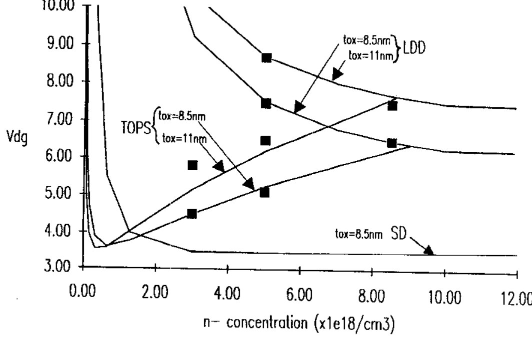

Fig.7 V_{dg} at I_d=0.1pA/um versus n- concentration. The solid squares are the experimental data from Fig.6. The solid curves show the modelling results for T_{OX}=8.5 and 11nm.

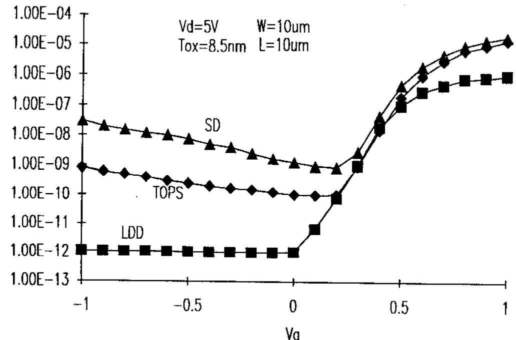

Fig.2 Subthreshold characteristics of SD, TOPS, and LDD devices, measured at V_d=5V.

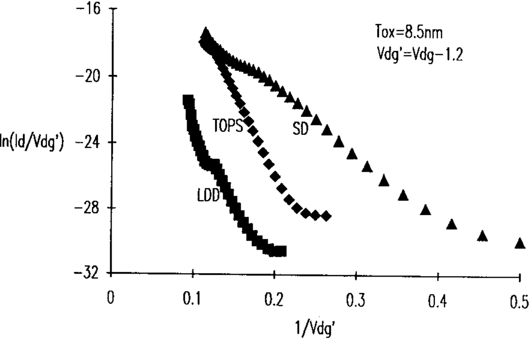

Fig.4 The band-to-band tunneling characteristics of the SD, TOPS, and LDD devices from Fig.3, with a common T_{OX} of 8.5nm. The slopes are not equal, indicating that the electric field contains both lateral and vertical components.

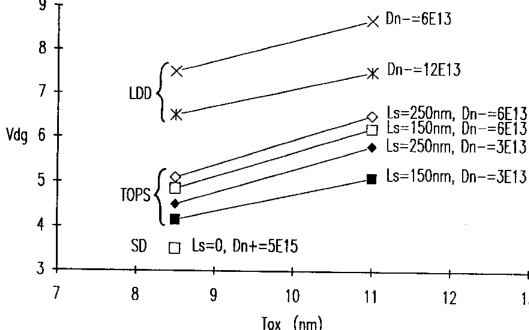

Fig.6 V_{dg} at I_d=0.1pA/um is plotted for the various oxide thicknesses, n- doses, and n- spacer lengths in this experiment. GIDL increases with n- dose for LDD devices, but decreases for TOPS devices.

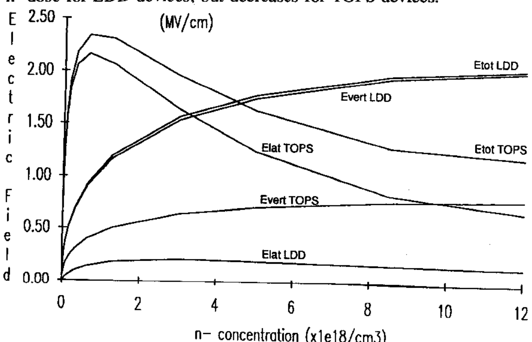

Fig.8 The field components in the gate-overlap region of the LDD drain plotted as a function of n- concentration, using the new analytical model. The lateral field of the TOPS arsenic n+ junction is reduced by increasing the phosphorus n- doping.