23.2 A Modular 1mm³ Die-Stacked Sensing Platform with Optical Communication and Multi-Modal Energy Harvesting

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Wireless sensor nodes have many compelling applications such as smart buildings, medical implants, and surveillance systems. However, existing devices are bulky, measuring >1cm³, and they are hampered by short lifetimes and fail to realize the "smart dust" vision of [1]. Smart dust requires a mm³-scale, wireless sensor node with perpetual energy harvesting. Recently two application-specific implantable microsystems [2][3] demonstrated the potential of a mm³-scale system in medical applications. However, [3] is not programmable and [2] lacks a method for re-programming or re-synchronizing once encapsulated. Other practical issues remain unaddressed, such as a means to protect the battery during the time period between system assembly and deployment and the need for flexible design to enable use in multiple application domains. To this end, we propose a 1.0mm³ general-purpose heterogeneous sensor node platform with a stackable multi-layer structure that includes a new, ultra-low power I²C (Inter-Integrated Circuit) interface for inter-layer communication. The system has an ultra-low-power optical wakeup receiver and GOC (Global Optical Communication), which enables re-programming and synchronization. It also includes an ultra-low power PMU (Power Management Unit) with BOD (Brown-Out Detector) to prevent processor malfunctions and battery damage. The BOD also controls a POR (Power-On Reset) module in other layers to enable a proper reset sequence. Image and temperature sensors are implemented, but the modularity of the system allows end-users to easily replace or add layers to incorporate specific circuits in appropriate technologies as needed.

Figure 23.2.1 shows the system block diagram and stack structure where four IC layers and one thin-film Li battery layer are wire-bonded on one side. Each layer measures less than 2.21×1.1mm², and the height of the entire system is 0.4mm, resulting in a 1.0 mm³ system. Power consumption ranges from 11nW in sleep mode up to ~40μW in active mode. A flexible PMU allows harvesting for perpetual operation from various energy sources. Two ARM Cortex-M0 processors are located in separate layers: 1) The DSP CPU efficiently handles data from the imager (or other sensors) and is built in 65nm CMOS (Layer 3) with a large 16kB non-retentive SRAM (NRSRAM). 2) The CTRL CPU manages the system using an always-on 3kB retentive SRAM (RSRAM), which maintains the stored operating programs, and is built in low-leakage 180nm CMOS (Layer 4). Solar cells for energy harvesting and a low-power imager are placed in the top layer (Layer 1) for light exposure. A gate-leakage-based timer [4] and temperature sensor are also implemented in Layer 1, fabricated in 130nm CMOS for gate-leakage current optimization and timer accuracy. Time tracking with temperature compensation provides a timing reference to synchronize radios that will be attached to this modular platform in future work.

All layers communicate via a modified I²C protocol, which requires only two bidirectional wires: clock (SCL) and data (SDA). I²C is chosen due to the pad count limitation in the 1mm³ form factor, and for easy expansion of the platform to any I²C-compatible devices. However, conventional I²C relies on pull-up resistors, which consume mWs when wires are pulled down. We therefore propose an ultra-low power, time-divided pull-up/pull-down scheme that is compatible with standard I²C (Fig. 23.2.2). I²C requires SDA to be changed when SCL is high. Therefore, we divide the SCL-low cycle into five sub-cycles where any attached layer can pull up SDA in the second sub-cycle and pull down in the fourth. This gives higher priority to a layer pulling down just as in standard I²C, without a large pull-down current. A standard I²C unit can be attached to the system at the cost of occasional short-circuit current for one SDA sub-cycle when a low power I²C unit pulls up the SDA and a standard I²C unit pulls down. The energy consumption was measured to be 88pJ/bit whereas typical commercial I²C unit consumes >3nJ/bit.

The PMU (Fig. 23.2.3) provides two supply voltages (0.6V and 1.2V) from the 3.2 – 4.1V battery through a switched capacitor network (SCN), automatically configured to either a 6× or 5× conversion ratio. The PMU achieves 61.2% and 62.4% down-conversion efficiency during active and sleep mode, respectively. A 242pW BOD uses a continuous comparator, followed by a clocked comparator with a 200mHz leakage-based oscillator to reduce power. When the battery voltage falls below 3.1V, the BOD turns off all supplies and enters a 185pW Deep Sleep mode in which only the solar cell is monitored. When sufficient light is detected the system enters Recovery mode, enabling energy harvesting. After the battery has reached a sufficient voltage (>3.4V), the system returns to its normal operational state. A harvesting-SCN (h-SCN) up-converts the energy source by 2× or 3×, which is then connected to either the 0.6V or 1.2V terminals of the battery-SCN (b-SCN). This reconfigurability enables approximate maximum power point tracking for a range of energy sources. Every 6.2s, the h-SCN is disconnected from b-SCN for 0.9s to determine the open-circuit voltage of the energy source. A programmable fraction of the h-SCN outputs is compared to the 1.2V and 0.6V terminals of b-SCN to automatically find the optimal configuration. By tailoring the fraction to the energy source impedance, we have demonstrated harvesting within the system from Layer 1's 0.54mm² solar cell, as well as an external 125mm² TEG, and an ocean microbial fuel cell. Harvested power delivered to the battery from the solar cell is shown in Fig. 23.2.3.

GOC serves three critical purposes that enhance the usability of the sensing platform: initial programming after system assembly, re-synchronization during use, and re-programming out of Deep Sleep mode or when the program has become corrupted. At 228pW standby power, it is ~20,000× lower power than typical RF wakeup radios (4.4μW in [5]), which rely on an uncorrupted software stack, defeating the purpose of re-programming. The GOC module consists of a main controller and three majority-voted front-end receivers for robustness (Fig. 23.2.4). The front-end consists of a photodiode, a pull-down resistor for faster response time, and a comparator. The tunable resistor is implemented with off-state MOSFETs. Since the GOC is located in Layer 4, the front-end receivers are placed between bonding pads to ensure light exposure. To prevent a false trigger, a predetermined 16-bit pattern is used as a passcode. Once initiated, the GOC operates at an 8× faster rate to enable a higher transmission rate. Additionally, a local chip-ID/mask allows for selective batch-programming of multiple sensor nodes. GOC is measured to be operational up to 120bps, consuming 72pJ/bit. A gate-leakage-based timer [4] and temperature monitor provide temperature-compensated time tracking, which is critical for synchronizing wireless communication. The temperature sensor (Fig. 23.2.5) consumes 806nJ/pt with a standard deviation of 0.51°C. Combined with an LDO and 2T voltage reference [6] the timer consumes 8.6nW. Also shown in Fig. 23.2.5 is a low power, dual-supply 96×96 imager that uses psub/n+ diodes in a standard CMOS process and consumes 680nJ/frame.

Figure 23.2.6 shows a measured operating scenario executed on the complete sensor platform when running off the battery and powered by the PMU. The captured traces show communication among the three layers. In this trace, dies were connected using board-level connections that were identical to the connections in the stacked system; the dies themselves were identical to those shown in the stacked system in Fig. 23.2.1, with the exception of added observability to aid measurement. In sleep mode, the system consumes 11nW and the solar cell can provide up to 40nW through the PMU to charge the battery, leading to energy autonomous operation. Without harvesting, the 0.6μAh battery can support the system in sleep mode for up to 2.3 days.

Acknowledgements:
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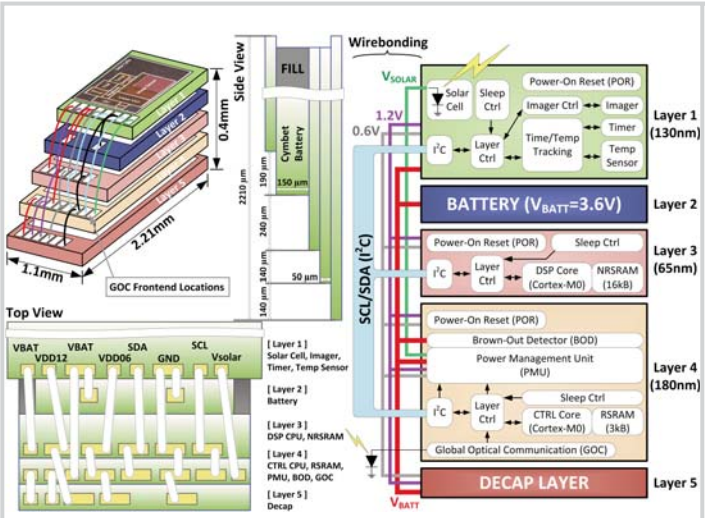

Figure 23.2.1: 5-layer chip-stacking assembly specifications (left) and system block diagram (right).

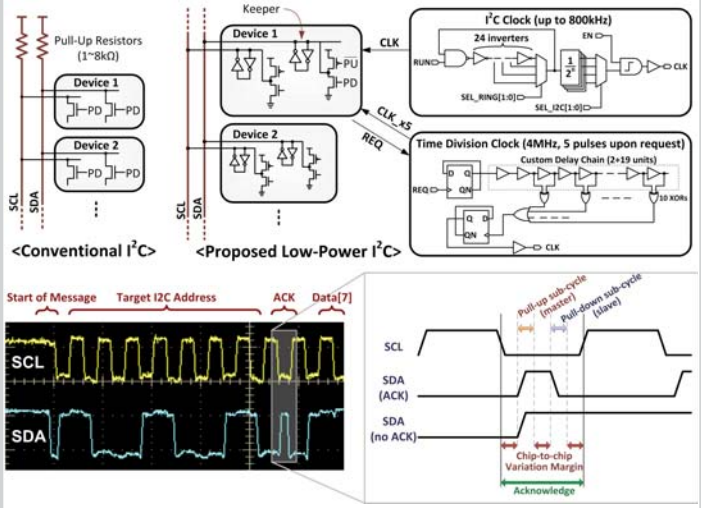

Figure 23.2.2: Circuit implementation of conventional and low power I²C (top) and measured waveforms (bottom).

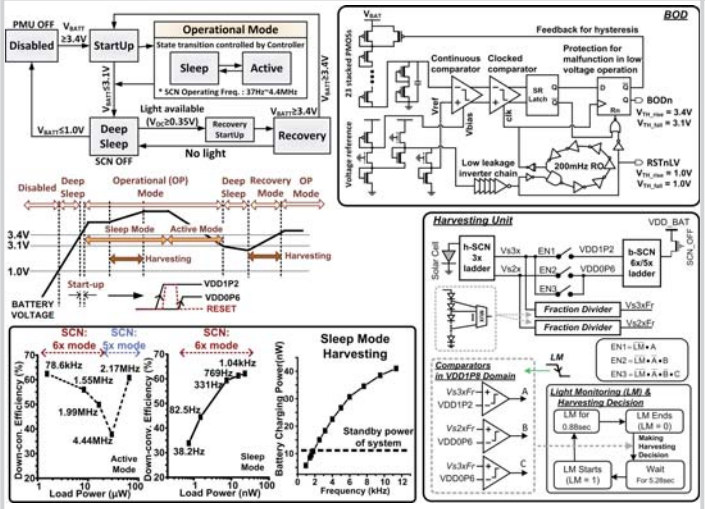

Figure 23.2.3: PMU state diagram and an example with battery voltage waveform and measured results (left). Circuit diagram of BOD (top right) and harvesting unit in PMU (bottom right).

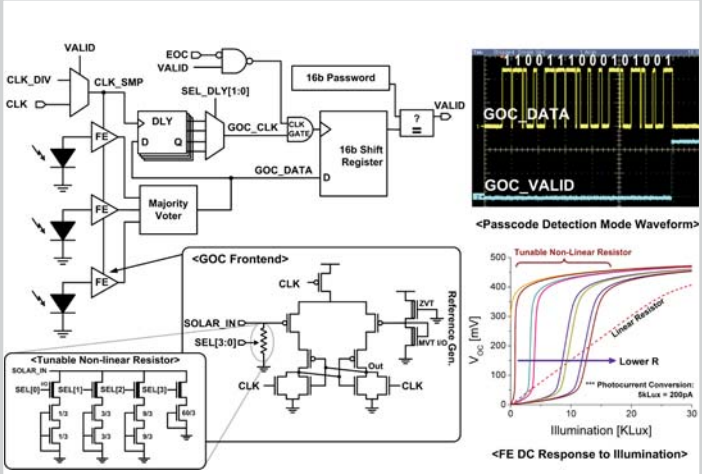

Figure 23.2.4: Circuit diagram for GOC (left) and measured waveform for passcode detection (top right). Simulations show that non-linear resistance in the front-end offers a 14× sharper slope (bottom right).

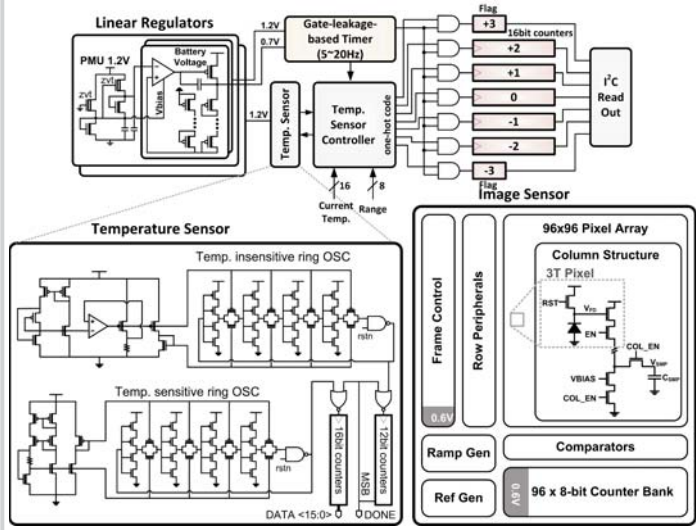

Figure 23.2.5: Block and circuit diagrams for time/temperature tracking (top). The low-power image sensor and a sample image (right).

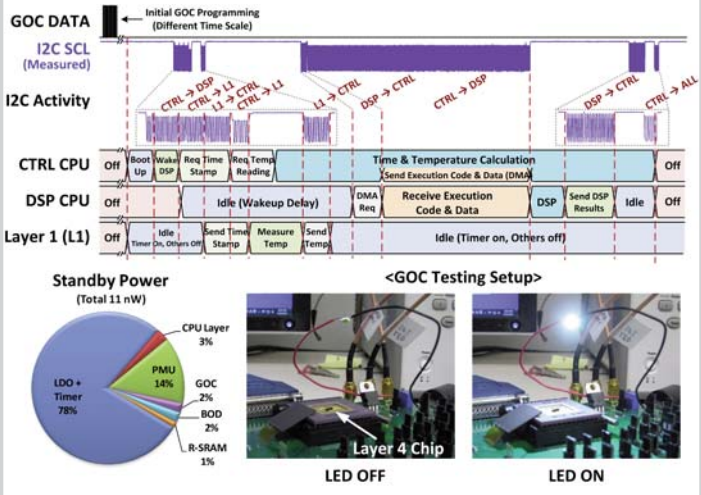

Figure 23.2.6: Measured waveform of the I²C SCL line along with the corresponding usage scenario (top). Measured standby power distribution (bottom left) and testing setup for GOC (bottom right).

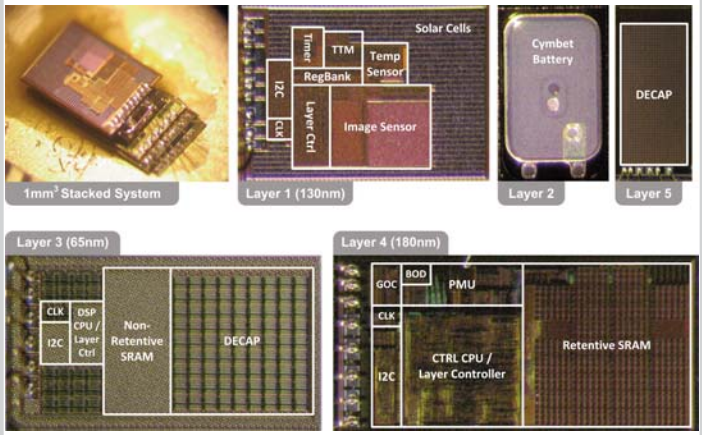

Figure 23.2.7: Photograph of the 1mm³ stacked sensor platform and die micrograph of each layer. The system consists of 5 layers, of which 4 layers are manufactured in 3 different CMOS technologies.

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