

$$C_x = \frac{g_m + g_o}{g_m - g_o} C_d + \frac{g_o}{g_m - g_o} C_g \quad (1)$$

As a result, apart from the dynamic charge injection effects particularly from the memory's switches, the comparator's residual errors can be adjusted to virtually zero with this scheme.

After phase ϕ_1 goes low where the circuit is configured as in Fig. 2c, the regenerative amplifier formed by PMOS transistors Pa-b starts regeneration in the direction corresponding to the polarity of the input signal. After a short delay, when the regenerative amplifier produces a sufficient voltage difference between nodes A and B which can overcome all the mismatches (typically < 1 ns after starting regeneration), ϕ_2^{dr} goes high. This turns on ϕ_2^{dr} and the circuit is configured as in Fig. 2d. Thus, both PMOS and NMOS regenerative amplifiers combine to speed up the regeneration process. The voltages at nodes A and B are then regeneratively amplified until they reach the supply rails. Note that by using clock phase ϕ_1' (dotted line in Fig. 1) for input switches to isolate the output capacitance of the preceding stage, the regeneration speed can be further increased. In a multiplexed comparator scheme, this isolation is readily obtained.

Table 1: Performance comparison between basic and enhanced SI comparators

Characteristics (typical process at 25°C)	Basic comparator	Enhanced comparator
Differential input range	$\pm 125\mu\text{A}$	$\pm 125\mu\text{A}$
Offset currents:		
Systematic input offset of $10\mu\text{A}$	$\sim 1\mu\text{A}$	$\sim 20\text{nA}$
Monte-Carlo analysis	$\sim 1.8\mu\text{A}$	$\sim 290\text{nA}$
Resolution	6 bit	8.5 bit
Comparison rate	$\geq 200\text{MHz}$	$\geq 270\text{MHz}$
Power consumption	1.7mW	1.7mW

Practical simulated results: The enhanced SI comparator in Fig. 1 with a multiplex configuration has been designed and simulated for a standard 3.3V and 0.6 μm digital CMOS process. The neutralisation capacitors C_x were implemented using NMOS transistors with minimum channel length where their widths were designed to provide the gate-drain capacitances according to eqn. 1. This helps to track inevitable parameter variations in Na-b with process and temperature. Note that simulations of the original basic SI comparator (without error neutralised C_x s and ϕ_2^{dr} switches) were also carried out to compare the performance of the two cells. Simulated performances of these comparators are summarised in Table 1 where it is seen that, for a systematic offset current of $10\mu\text{A}$ in both circuits, the enhanced comparator obtains a near-zero offset current. To verify the effectiveness of the proposed enhanced comparator in practice, Monte-Carlo simulations were also conducted with the statistical parameter variations provided by the employed process to take into account both process spread and device mismatch. Under the same conditions, an improvement in resolution of ~ 2.5 bits over that of the basic comparator can be obtained (Table 1). In terms of maximum operating speed, the enhanced comparator exhibits an improvement by more than a factor of 1.35. Thus, the use of the presented enhanced techniques should enable us to implement switched-current A/D converters with high resolution for applications at several hundreds of megahertz.

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Extended chaos control method applied to Chua circuit

L.A.B. Tôrres and L.A. Aguirre

An extended chaos control strategy, based on previous work, is developed and applied to a real implementation of Chua's circuit. The new approach leads to improvements in the stability and controllability of this electronic oscillator, which has been used to study secure communication systems.

Introduction: Recently, much effort has been devoted to the development of control and synchronisation strategies in order to make viable the use of simple chaotic oscillators in communication systems [1]. Synchronisation can be regarded as a special case of the control problem and therefore both are of great importance.

One of the most studied oscillators is Chua's circuit [2]. This oscillator is very robust and can be easily implemented. The main purpose of this Letter is to describe an alternative control strategy for Chua's circuit, thus overcoming two main shortcomings in [3], namely the use of large values for the proportional gain means that the control can only be switched on when the state to be controlled is close to the reference signal ($x(t) \approx x_{ref}(t)$), and the oscillator cannot be stabilised over the entire state space. Another important contribution of this Letter is that an actual implementation of the new strategy for a real oscillator is described, unlike the majority of pages published in the field which validate results based exclusively on simulations.

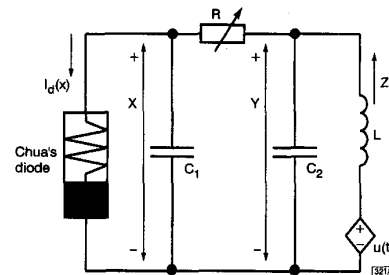


Fig. 1 Monovariate control of Chua's circuit

Hwang control strategy: The dynamical equations describing the system in Fig. 1 are

$$\dot{x} = \frac{y-x}{RC_1} - \frac{i_d(x)}{C_1} \quad \dot{y} = \frac{x-y}{RC_2} + \frac{z}{C_2} \quad \dot{z} = \frac{-y}{L} + \frac{u(t)}{L} \quad (1)$$

$$i_d(x) = m_0 x + 0.5(m_1 - m_0)\{|x + B_p| - |x - B_p|\} \quad (2)$$

where x and y are the voltages across the capacitors C_1 and C_2 , respectively, and z is the current through inductor L . The control signal $u(t)$ in eqn. 1 can be written as

$$u(t) = y + Lk_1 \underbrace{\left(\frac{x-y}{RC_2} + \frac{z}{C_2} \right)}_{\dot{y}} + Lk_p(x_{ref} - x) \quad (3)$$

Using the above control law, the equilibrium manifold M_{eq}^c of eqn. 1 is a function of x_{ref} , namely

$$\begin{aligned} \dot{x} = \dot{y} = \dot{z} = 0 \\ \Rightarrow M_{eq}^c = \begin{cases} Lk_p(x_{ref} - x_{eq}) = 0 \rightarrow x_{eq} = x_{ref} \\ y_{eq} = x_{ref} + Ri_d(x_{ref}) \\ z_{eq} = i_d(x_{ref}) \end{cases} \quad (4) \end{aligned}$$

Therefore, stabilising the system on this new equilibrium manifold is equivalent to guaranteeing that $\lim_{t \rightarrow \infty} x - x_{ref} = 0$. This can be achieved by means of local analysis of the system eqn. 1 around $x = x_{ref}$. In this case, the flow can be approximated by the truncated Taylor expansion

$$\begin{aligned} \dot{\tilde{x}} &= f(\tilde{x}) \simeq f(\tilde{x}_{ref}) + D_J(\tilde{x} - \tilde{x}_{ref}) \\ \dot{\tilde{e}} &= \tilde{x} - \tilde{x}_{ref} \Rightarrow \dot{\tilde{e}} = f(\tilde{x}_{ref}) + D_J\tilde{e} - \dot{\tilde{x}}_{ref} \end{aligned} \quad (5)$$

where $\tilde{x} = [x \ y \ z]^T$ and D_J indicates the Jacobian. If the following two hypotheses are verified:

- (i) $f(\tilde{x}_{ref}) = 0$, i.e. the vector \tilde{x}_{ref} is in the equilibrium manifold of eqn. 1 and hence from eqn. 4, $\tilde{x}_{ref} = [x_{ref} \ y_{eq} \ z_{eq}]^T$
- (ii) x_{ref} is constant or slow compared to D_J so that $\dot{\tilde{x}}_{ref} \approx [0 \ 0 \ 0]^T$ then $\dot{\tilde{e}} = D_J\tilde{e}$. It is easy to show that for the control law eqn. 3 proposed in [3] the above requirements are satisfied. The task becomes to correctly choose the control parameters (k_1, k_p) in order to assure that the Jacobian matrix

$$D_J|_{x=x_{ref}(t)} = \begin{bmatrix} \left(-\frac{1}{RC_1} - \frac{1}{C} \frac{di_d(x)}{dx}\right) & \frac{1}{RC_1} & 0 \\ \frac{1}{RC_2} & -\frac{1}{RC_2} & \frac{1}{C_2} \\ \frac{1}{L} \frac{du(t)}{dx} & \left(-\frac{1}{L} + \frac{1}{L} \frac{du(t)}{dy}\right) & \frac{1}{L} \frac{du(t)}{dz} \end{bmatrix} \quad (6)$$

is stable over the entire state space. Indeed, it is necessary to analyse only two possible Jacobian matrices, because only the first element of eqn. 6 changes as the slope of eqn. 2 assumes one of the two values (m_0 or m_1).

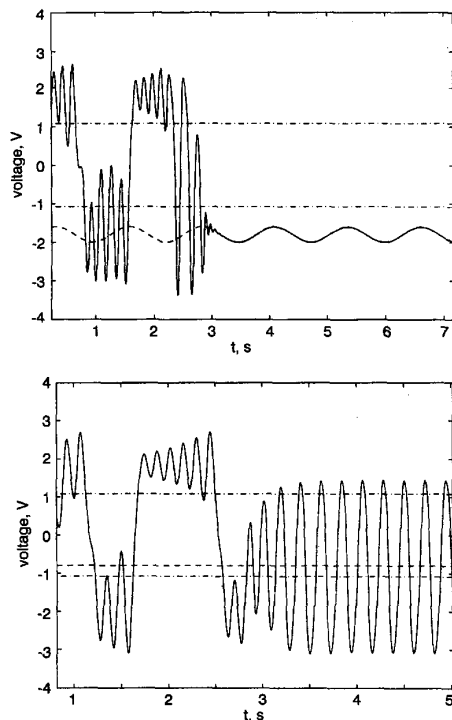


Fig. 2 Real data and $x(t)$

— $x(t)$
 - - - $x_{ref}(t)$
 - · - · $B_p = \pm 1.08 \text{ V}$
 Upper: real data
 Lower: $x(t)$
 Original control law is not effective for $x_{ref} \in [-B_p, +B_p]$

Stability of the linearised system is achieved by satisfying the Routh-Hurwitz criterion for the coefficients of the characteristic polynomial of eqn. 6. This produces a set of restrictions on the control parameters that must be satisfied.

Real data measured from the controlled circuit using the original control law (eqn. 3) switched on at $t = 2.3 \text{ s}$ are given in Fig. 2 (upper), where an adaptive proportional gain

$$k_p = 1 + 5[1 + 5(x_{ref}(t) - x)^2]^{-1} \quad (7)$$

was used to avoid large excursions of the state x that lead the circuit to unstable regions. At the same time, the gain was gradually increased as $|x_{ref}(t) - x(t)| \rightarrow 0$, diminishing the steady state error.

As pointed out in [3], $\exists (k_1, k_p)$ such that the controlled system is stable for $-B_p \leq x_{ref} \leq +B_p$ as seen in Fig. 3.

New control strategy: The cause for instability in the central portion of eqn. 2 is not parameter tuning, but rather is related to the form of eqn. 3. It is possible to extend the method in [3] in order to realise a controller that stabilises the system in all the state space by changing the structure of $u(t)$.

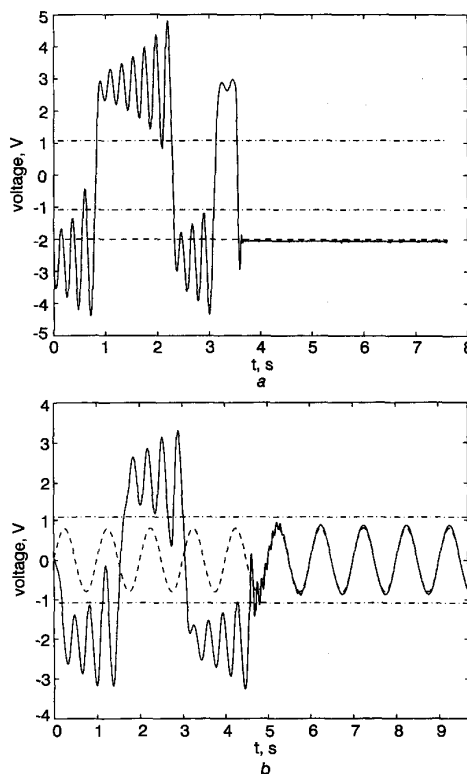


Fig. 3 $x(t)$ for constant reference and sinusoidal reference

— $x(t)$, - - - $x_{ref}(t)$
 $B_p = \pm 1.08 \text{ V}$
 a Constant reference
 b Sinusoidal reference

Note that the control strategy proposed above relies on stabilising the system on M_{eq}^c . Therefore, to apply the method mentioned earlier, it is necessary to guarantee $f(\tilde{x}_{ref}) = 0$ and $\dot{\tilde{x}}_{ref} \approx [0 \ 0 \ 0]^T$. The design of the new control law can be described in two steps: **structure selection:** $u(t)$ must guarantee hypothesis 1, i.e. $x_{eq} \approx x_{ref}$, $y_{eq} = g(x_{ref})$ and $z_{eq} = h(x_{ref})$, where $g(\cdot), h(\cdot)$ are real functions; and **parameter tuning:** D_J in eqn. 6 must have stable eigenvalues in all regions of eqn. 2. It should be realised that eqn. 3 satisfies the structure constraint, but not the parameter tuning constraint over the entire state space.

There are innumerable structures that satisfy these design constraints. For example, starting from the original control expression and using linear feedback, Lk_2v can be added to eqn. 3 in order to gain another degree of freedom in the search for stable D_J . The new control expression becomes

$$u(t) = y + L \left\{ k_1 \left(\frac{x-y}{RC_2} + \frac{z}{C_2} \right) + k_2 y \right\} + Lk_p(x_{ref} - x) \quad (8)$$

and it is possible to find values of (k_1, k_2, k_p) that yield a globally stable system. Substituting eqn. 8 into eqn. 1 and making $\dot{x} = \dot{y} = \dot{z} = 0$ yields the new equilibrium manifold

$$M_{eq}^c = \begin{cases} x_{eq} = \frac{B_p(m_a - m_b)R + (k_p/k_2)x_{ref}}{[(k_p/k_2) - m_c R - 1]} \\ y_{eq} = k_p/k_2(x_{eq} - x_{ref}) \\ z_{eq} = 1/R[x_{eq} - k_p/k_2(x_{eq} - x_{ref})] \end{cases} \quad (9)$$

where if $x < -B_p \Rightarrow a = c = 0, b = 1$, or if $x > B_p \Rightarrow a = 1, b = c = 0$ or if $x \leq |B_p| \Rightarrow a = b = 1, c = 1$. It is easy to verify that the greater the value of k_p , the smaller the difference between x_{eq} and x_{ref} . Hence this choice of control law structure still guarantees that $x_{eq} \approx x_{ref}$, just as in eqn. 4.

Implementation results: To experimentally verify the new control strategy, a real implementation of an electronic oscillator was used with $C_1 = 5.91\mu\text{F}$, $C_2 = 49.5\mu\text{F}$, $R = 1.8\text{k}\Omega$, $L = 11.75\text{H}$ (L was implemented with a gyrator), $B_p = 1.08\text{V}$, $m_0 = -0.37\text{mS}$, $m_1 = -0.68\text{mS}$. For these parameters the circuit exhibits chaos. The control algorithm runs on a PC using $k_1 = -0.1$, $k_2 = -2.5$ and k_p as defined in eqn. 7. A data acquisition board was used both to measure x, y and z at a high frequency rate and to continuously actuate, by applying the voltage $u(t)$ in eqn. 8, using an analogue output port.

Both strategies, the original eqn. 3 and the new control eqn. 8, exhibit high robustness to parameter mismatch (up to 50% on the values of the capacitors and up to 25% on the value of the inductor). Owing to the high gain proportional control law eqn. 7, the control effort is quite high.

Figs. 2 and 3 show real data measured from the circuit. In particular, Fig. 3b confirms that the new procedure also stabilises the oscillator for $x_{ref}(t) \in [-B_p, +B_p]$.

Conclusions: A new strategy for the control of a chaotic oscillator has been developed based on [3] and applied to Chua's circuit. The new approach overcomes two shortcomings of the original method. First, by using an adaptive gain, the new controller can be switched on at any time and the steady state error is also diminished. Secondly, the present method can stabilise the oscillator over the entire state space. The results briefly reported are relevant in many ways especially taking into account that many recent studies have considered the control of Chua's circuit in the context of communication systems [1].

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Phase accumulator synthesis algorithm for DDS applications

R. de J. Romero-Troncoso and G. Espinosa-Flores-Verdad

An algorithm for area-speed optimisation in phase accumulator synthesis is presented. Digital direct synthesis (DDS) requires an efficient phase accumulator as its main functional block. However, fast phase accumulators are very area-demanding and the tradeoff between area and speed is very critical. The approach can be used for the optimisation and synthesis of phase accumulators in FPGAs and ASICs.

Introduction: Fig. 1 shows the block diagram of a phase accumulator. The basic operation of this structure can be found in [1]. The output frequency of the phase accumulator is given by

$$f_o = \frac{N}{2^n} f_{ck}$$

where f_o is the output frequency, f_{ck} the clock frequency, n the number of bits and N varies from 0 to 2^n-1 . Since N can be programmed to lie anywhere between 0 and 2^n-1 , the output frequency can be selected linearly with a very high resolution. For example, if we had a 16 bit phase accumulator with an input clock frequency of 20MHz then we can choose output frequencies from 0 to 10MHz in steps of 305Hz.

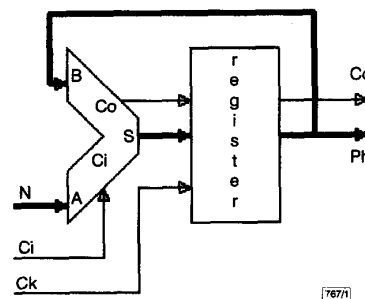


Fig. 1 Phase accumulator

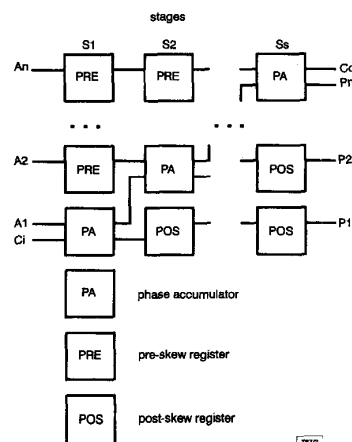


Fig. 2 Pipeline approach

The main disadvantage of a phase accumulator with the architecture shown in Fig. 1 is that the adder must be very fast in order to achieve its highest performance, but for wide accumulators the propagation delay in the adder will be very high and the operating frequency will drop. Therefore, high frequency operation is required (and for most applications it is) then another architecture must be used and the pipeline approach is the best suited to this task. Pipeline operation allows us to achieve a higher operating frequency [2] because the full operation is segmented in small parts. Each part is computed in a single stage, then it is passed to the next stage to the second computation and at the same time new information comes into the first stage like in a production line, as shown in Fig. 2.