LETTER

A Design of CMOS Chua-Type Analog Chaos Circuit Based on a Signal Flow Graph

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SUMMARY This paper presents a design of CMOS Chua-type analog chaos circuit by using a signal-flow-graph (SFG) method. In this circuit, the transmittance of a nonlinear element is realized by an OTA with a feedback resistor, and other linear elements are realized by op-amp based circuits. The proposed circuit is insensitive to the finite admittance of OTA's and to the parasitics of resistors except a feedback resistor in the nonlinear element. The performance and chaotic behavior of the proposed circuit are confirmed by SPICE simulations.

key words: *chaos, Chua-type circuit, signal flow graph, operational amplifier, operational tranceconductance amplifier*

1. Introduction

A Chua's circuit is the most typical chaos circuit and is the simplest autonomous electronic circuit generating chaotic signals [1]. Therefore, a Chua's circuit has become a favorite tool for analytical, numerical, and experimental studies of chaotic phenomena.

In the past design of chaos circuits, discrete analog elements have been used as their building blocks. Recently, there has been a strong motive for on-chip chaos signal generation in the field of communications and signal processing systems [2]–[4]. For this reason, several attempts have already been made for the monolithic IC realization of a chaos circuit. Among those, Chua's circuits have been realized by using operational transconductance amplifier's (OTA's) [5] and CMOS technologies [6]. However, all of these continuous-time Chua's circuits have been realized being based on circuit-element simulations.

In this paper, we realize a CMOS Chua-type analog chaos circuit by using a signal flow graph (SFG) method. In this circuit, a nonlinear element is realized by an CMOS OTA with a feedback resistor, and other linear elements are realized by CMOS op-amp based circuits. Since every terminal of these elements is connected to the voltage source or the virtual ground, the proposed circuit is insensitive to finite admittance of OTA's and to the parasitics of resistors except for a feedback resistor composed of the nonlinear element. This is advantageous to practical applications. The performance and chaotic behavior of the proposed circuit are confirmed by SPICE simulations. A strange attractor like "double scroll" is obtained from the simulation results.

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2. Proposed CMOS Chua-Type Circuit

2.1 Circuit Dynamics and Structure

The dynamics of the typical Chua's circuit [1] can be rewritten as

$$V_{C1} = -\frac{1}{C1}\int\left[-\left(\frac{V_{C2}}{R}\right)+\left(\frac{V_{C1}}{R}\right)+g(V_{C1})\right]dt$$
$$V_{C2} = -\frac{1}{C2}\int\left[-\left(\frac{V_{C1}}{R}\right)+\frac{V_{C2}}{R}+\frac{1}{L}\int V_{C2}dt\right]dt\ , \quad (1)$$

where V_{C1} and V_{C2} are the voltage across the capacitors $C1$ and $C2$, respectively, and $g(V_{C1})$ is the DC transfer characteristic of the nonlinear element.

The SFG of the Chua's circuit can be derived directly from Eq. (1). The resulting SFG is shown in Fig. 1. If we introduce a capacitor $C3$ defined by $C3 = L/R^2$, we can realize all integrators in Fig. 1 by using conventional op-amp based RC-active integrators. The RC-active realization of a Chua-type circuit based on the SFG in Fig. 1 is shown in Fig. 2. This circuit is composed of a nonlinear conductor (NLC) block, an inductor block, two capacitor blocks, two inverter blocks, and other four resisters.

In this realization, the NLC block realizes the DC transfer characteristic like the shape of Chua diode's I–V characteristic. The NLC block is realized by a typical source-coupled pair type CMOS OTA with a feedback resistor r_0. The inductor block and the capacitor blocks are realized by using CMOS op-amp based RC-active integrators.

2.2 Design

Here, we will show the design of each building block of the proposed Chua-type circuit. We first consider the NLC block. We assume that the OTA is an NMOS source-coupled pair loaded with a PMOS current mirror shown in Fig. 3. For simplicity, assume that each MOSFET obeys a square-law model. Then, the DC transfer characteristic of the OTA is given by

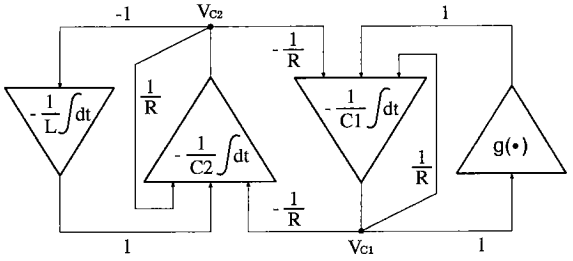

Fig. 1 Signal flow graph representation of a Chua's circuit.

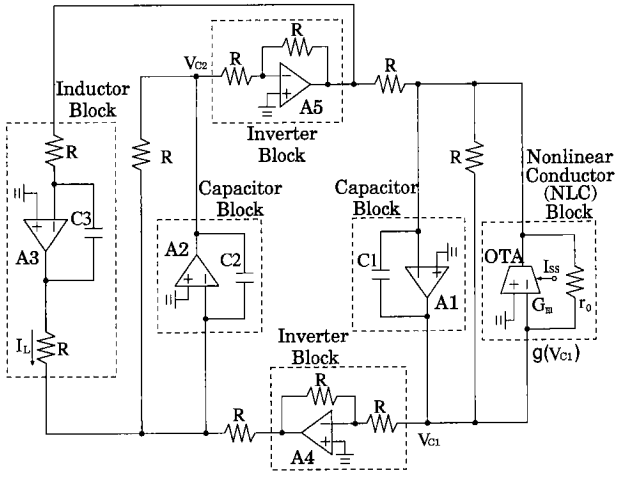

Fig. 2 Circuit structure of the proposed CMOS Chua-type circuit.

$$I_{out} = KV_{in}\sqrt{\frac{2I_{SS}}{K} - V_{in}^2}\ , \tag{2}$$

where K is the conductance coefficient of NMOS transistors of the source-coupled pair, V_{in} is the differential input voltage ($\triangleq V_+ - V_-$), I_{out} is the output current, and I_{SS} is the DC bias current of the OTA.

When G_m denotes the small-signal conductance of an OTA, the small-signal transfer conductance g_e of the NLC block in Fig. 3 is given by the following approximation,

$$g_e = \begin{cases} -G_m + \dfrac{1}{r_0}, & \text{for} \quad |V_{in}| < \sqrt{\dfrac{I_{SS}}{K}}\ , \\ \dfrac{1}{r_0}, & \text{for} \quad |V_{in}| \geqq \sqrt{\dfrac{I_{SS}}{K}}\ , \end{cases} \tag{3}$$

where $G_m \triangleq (\partial I_{out}/\partial V_{in})$. Therefore, the output current I_{NC} of the NLC block is $I_{NC} = g_e V_{NC}$. Note that the slops of the DC transfer characteristics of the NLC block are determined by the feedback resistor r_0 and the bias current I_{SS} of the OTA as Eq. (3).

3. Simulations

For the proposed Chua-type circuit, the OTA was given by a typical source-coupled pair type CMOS OTA shown in Fig. 3, and the op-amp was given by a typical CMOS op-amp shown in Fig. 4. SPICE simulations were performed under the condition that the power supplies of the op-amp's and the OTA are $V_{DD} = 4$ V and $V_{SS} = -4$ V, the bias current I_{SS} of the OTA is 100 μA, and the bias current I_{SS} of the op-amp's was 50 μA. The device dimensions of the MOSFET's in the OTA and the op-amp are shown in Tables 1 and 2, respectively. The model parameters of the MOSFET's are shown in Table 3. The proposed circuit is assumed to be designed by a standard 0.8 μm CMOS process.

The solid line in Fig. 5 shows the simulated DC transfer characteristic of the NLC block in Fig. 3. Here, the feedback resistor r_0 chose 20 kΩ since the range of the differencial input voltage of the NLC block that is the oscillation amplitude of the proposed circuit is limited to the extent of ± 1 V. The negative-slope

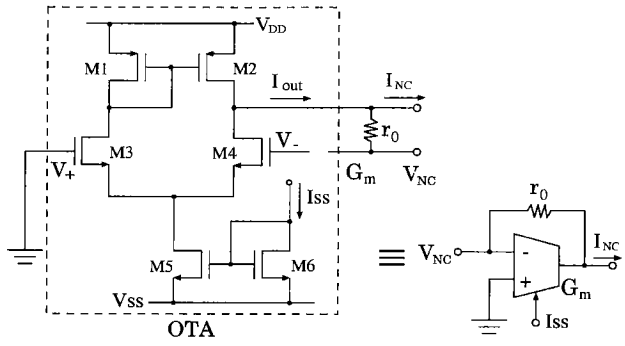

Fig. 3 Circuit diagram and symbol of nonlinear conductor block.

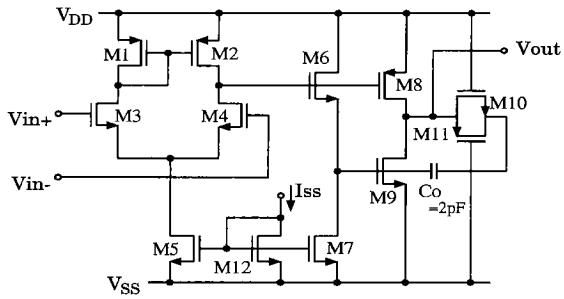

Fig. 4 Circuit diagram of the CMOS op-amp.

Table 1 Device dimensions of MOSFET's in the OTA.

M1, M2	PMOS	W=6 μm L=5 μm AD=16pm AS=12.5pm PD=9.8 μm PS=10 μm
M3	NMOS	W=5 μm L=5 μm AD=9.4pm AS=12pm PD=9.8 μm PS=9.4 μm
M4	NMOS	W=5.45 μm L=5 μm AD=9.4pm AS=12pm PD=9.8 μm PS=9.4 μm
M5	NMOS	W=6 μm L=5 μm AD=12.5pm AS=12pm PD=0.8 μm PS=9.8 μm
M6	NMOS	W=6 μm L=5 μm AD=12.5pm AS=12pm PD=10 μm PS=9.8 μm

Table 2 Device dimensions of the MOSFET's in the op-amp.

M1	PMOS	W=6 μm L=10 μm AD=156pm AS=108pm PD=46 μm PS=36 μm
M2, M8	PMOS	W=6 μm L=10 μm AD=186pm AS=228pm PD=56 μm PS=64 μm
M3, M4	NMOS	W=10 μm L=10 μm AD=164pm AS=50pm PD=42 μm PS=7 μm
M5, M7	NMOS	W=6 μm L=5 μm AD=48pm AS=156pm PD=16 μm PS=46 μm
M6	NMOS	W=10 μm L=5 μm AD=164pm AS=50pm PD=42 μm PS=7 μm
M9	NMOS	W=6 μm L=10 μm AD=48pm AS=156pm PD=16 μm PS=46 μm
M10	NMOS	W=6 μm L=14 μm AD=48pm AS=156pm PD=16 μm PS=46 μm
M11	PMOS	W=6 μm L=5 μm AD=186pm AS=228pm PD=56 μm PS=64 μm
M12	NMOS	W=6 μm L=5 μm AD=156pm AS=156pm PD=46 μm PS=46 μm

Table 3 Model parameters of MOSFET's.

Parameters	NMOS	PMOS
VTO [V]	0.935538	−0.387519
NSUB [cm^{-3}]	$2.0\times10^{+15}$	$4.0\times10^{+16}$
KP [A/V^2]	40.286680×10^{-6}	14.388100×10^{-6}
UO [cm^2/Vs]	700	250
CJ [F/m^2]	2.0×10^{-2}	2.5×10^{-2}
CJSW [F/m]	7.0×10^{-7}	1.0×10^{-7}
CGSO [F/m]	3.5×10^{-10}	3.5×10^{-10}
CGDO [F/m]	3.5×10^{-10}	3.5×10^{-10}
CGBO [F/m]	1.75×10^{-9}	1.75×10^{-9}
NSS [cm^{-2}]	$1.0\times10^{+11}$	$4.0\times10^{+10}$
NFS [cm^{-2}]	$1.0\times10^{+11}$	$4.0\times10^{+10}$
TOX [m]	6.0×10^{-8}	6.0×10^{-8}
XJ [m]	6.0×10^{-7}	6.0×10^{-7}
LD [m]	3.0×10^{-7}	3.0×10^{-7}
NEFF	5	5

Table 4 Simulation condition.

Range of analysis	0 ~ 10 ms
Time step ceiling value	1 μs
Initial values	$V_{C1}=0$, $V_{C2}=0$

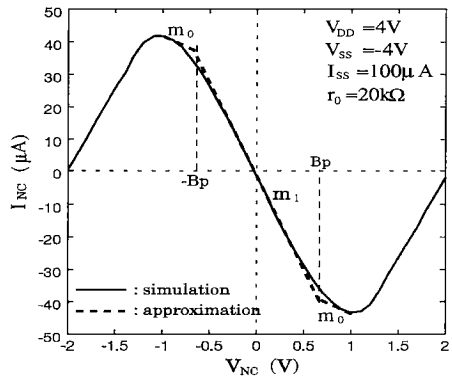

Fig. 5 Typical DC transfer characteristics of the nonlinear conductor block (obtained when $r_0=20\,\mathrm{k}\Omega$).

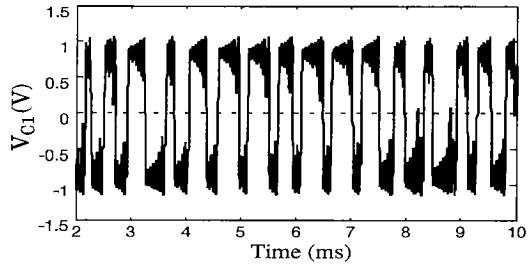

Fig. 6 A waveform of V_{C1} obtained for $C1=122\,\mathrm{pF}$ and $C3=100\,\mathrm{pF}$.

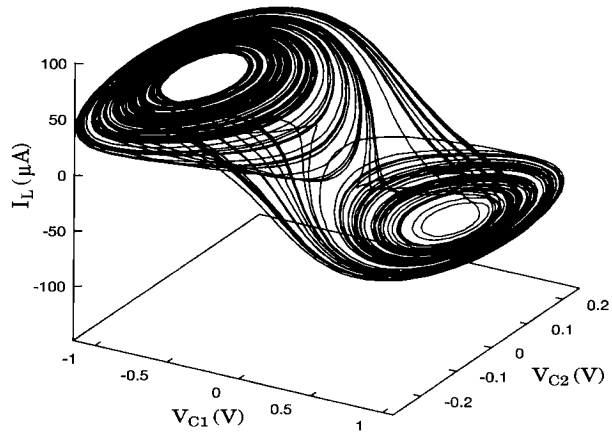

Fig. 7 A double-scroll-type strange attractor obtained for $C1=122\,\mathrm{pF}$ and $C3=100\,\mathrm{pF}$.

characteristic curve is piecewise-linear approximated as the broken line in Fig. 5, where slopes at the end regions m_0 and the middle region m_1 are $-22.930\,\mu\mathrm{S}$ and $-58.275\,\mu\mathrm{S}$, respectively, and the breakpoint B_p is $\pm0.7\,\mathrm{V}$.

Table 4 shows the simulation condition for the transient analysis. In this simulation, capacitors $C1$ and $C3$ were variable parameters, and the other element's values were fixed to $C2=1.1\,\mathrm{nF}$, $R=22\,\mathrm{k}\Omega$, and $r_0=20\,\mathrm{k}\Omega$.

The simulation results of the proposed Chua-type circuit are shown in Figs. 6–9. Figure 6 shows the time waveform of V_{C1}, and Fig. 7 shows the obtained 3-dimentional double-scroll-type strange attractor when $C1=122\,\mathrm{pF}$ and $C3=100\,\mathrm{pF}$ (these values are given by $\alpha=9.016$ and $\beta=11$, where $\alpha \triangleq C2/C1$ and $\beta \triangleq C2/C3$, and see Refs. [1], [7] for details). Figure 8 shows the result of the spectrum analysis of V_{C1} shown in Fig. 6 using the fast furier transform (FFT) with the sampling frequency of 1 MHz. In this figure, the spectrum analysis exhibits $1/f^{\delta}$ (δ denotes a positive constant) type characteristic at frequencies lower than about 100 kHz. On the other hand, the spectrum is flat at fre-

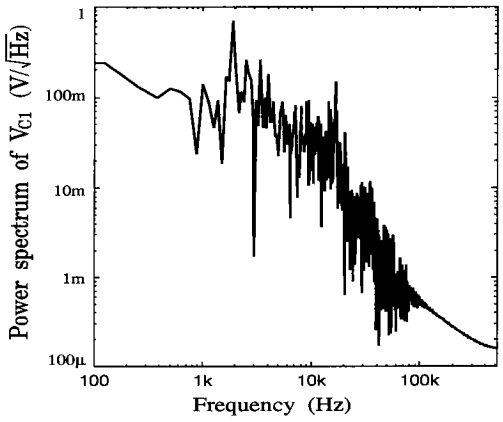

Fig. 8 The result of the spectrum analysis of V_{C1} shown in Fig. 6 using the FFT with the sampling frequency of 1 MHz.

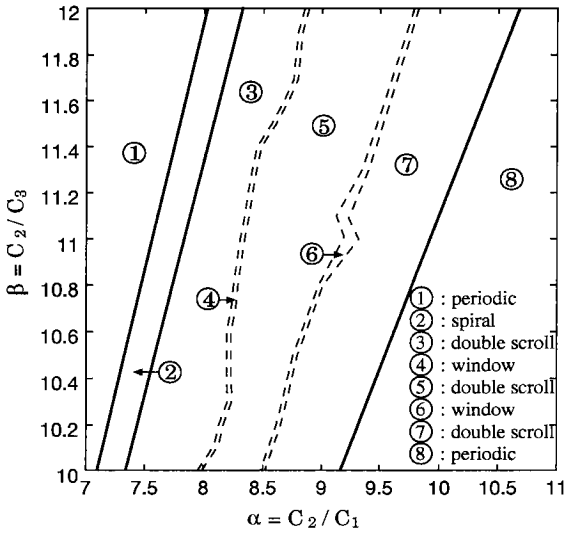

Fig. 9 Bifurcation diagram of the proposed circuit.

quencies greater than 100 kHz.

Figure 9 shows the bifurcation diagram of the proposed citcuit. In Fig. 9, the proposed circuit can observe a periodic attractor in area ①, a spiral attractor in area ②, a double-scroll-type strange attractor in area ③, ⑤, and ⑦, a window attractor in area ④ and ⑥, and a periodic attractor distinct from area ①, in area ⑧. These kinds of attractors have been proved to exist in the conventional Chua's circuit based on the ideal Chua diode.

4. Conclusion

Conventional analog chaos circuits, which have been designed being based on a circuit-element simulation method, have a disadvantage that they are sensitive to the parasitics of the resistors and to the finite admittance of the OTA's. The proposed CMOS Chua-type chaos circuit design is based on an SFG method. The proposed circuit is insensitive to those nonidealities except for a feedback resistor in the NLC block. In addition, the circuit is realizable using only a single OTA along with op-amp based RC-active integrators. It should be also emphasized that the superior frequency characteristic of the OTA is effectively utilized since the output of the OTA is virtually grounded.

In the proposed design, the resistors R's have a same value. The slopes of the DC transfer characteristic of the NLC block are determined by the r_0 and I_{SS} of the OTA. Further, the proposed design is compatible with the design of the conventional SFG-based RC-active filters. These facts are other advantages for the implementation into the IC form with a standard analog CMOS IC filter technology. Hence, the proposed SFG-based chaos circuit design will be a useful building block for chaos application IC's.

References

[1] L.J. Kocarev and T. Roska, "Dynamics of the Lorenz equation and Chua's equation: A tutorial," in Chua's circuit: A Paradigm for Chaos, ed. R.N. Madan, pp.25–55, World Scientific Publishing Co. Pte. Ltd., 1993.
[2] K.M. Cuomo, A.V. Oppenheim, and S.H. Strogatz, "Synchronization of Lorenz-based chaotic circuits with applications to communications," IEEE Trans. Circuits&Syst.-II, vol.40, no.10, pp.626–633, Oct. 1993.
[3] H. Dedieu, M.P. Kennedy, and M. Hasler, "Chaos shift keying: Modulation and demodulation of a chaotic carrier using self-synchronizing Chua's circuits," IEEE Trans. Circuits&Syst.-II, vol.40, no.10, pp.634–642, Oct. 1993.
[4] E.J. Altman, "Normal form analysis of Chua's circuit with applications for trajectory recognition," IEEE Trans. Circuits&Syst.-II, vol.40, no.10, pp.675–682, Oct. 1993.
[5] J.M. Cruz and L.O. Chua, "An IC chip of Chua's circuit," IEEE Trans. Circuits&Syst.-II, vol.40, no.10, pp.614–625, Oct. 1993.
[6] A. Rodriguez-Vázquez and M. Delgado-Restituto, "CMOS design of chaotic oscillators using state variables: A monolithic Chua's circuit," IEEE Trans. Circuits&Syst.-II, vol.40, no.10, pp.596–613, Oct. 1993.
[7] L.O. Chua, M. Komuro, and T. Matsumoto, "The double scroll family," IEEE Trans. Circuits&Syst., vol.33, no.11, pp.1072–1118, Nov. 1986.