PAPER *Special Section of Papers Selected from ITC-CSCC '98*

Synthesis and Analysis of a Digital Chaos Circuit Generating Multiple-Scroll Strange Attractors

Kei EGUCHI[†], **Takahiro INOUE**[††], *and* **Akio TSUNEDA**[††], *Members*

SUMMARY In this paper, a new digital chaos circuit which can generate multiple-scroll strange attractors is proposed. Being based on the piecewise-linear function which is determined by on-chip supervised learning, the proposed digital chaos circuit can generate multiple-scroll strange attractors. Hence, the proposed circuit can exhibit various bifurcation phenomena. By numerical simulations, the learning dynamics and the quasi-chaos generation of the proposed digital chaos circuit are analyzed in detail. Furthermore, as a design example of the integrated digital chaos circuit, the proposed circuit realizing the nonlinear function with five berakpoints is implemented onto the FPGA (Field Programmable Gate Array). The synthesized FPGA circuit which can generate n-scroll strange attractors ($n = 1, 2, \ldots 4$) showed that the proposed circuit is implementable onto a single FPGA except for the SRAM.

key words: *Chua's circuit, neuro-fuzzy circuits, supervised learning, discrete-time circuits, digital circuits, integrated circuits*

1. Introduction

In recent years, interest has been focused on exploring nonlinear systems. Among others, chaos circuits attract many researchers' attention since they open up new vistas for engineering application systems [1]–[3]. For example, Kohda exploits the quasi-chaos signals as the spreading sequences for CDMA system [1] and Nozawa et al. applied the chaotic neural network to the traveling salesman problem [2]. The chaos application systems such as chaos-based CDMA systems claim exact reproducibility of chaos signals as well as high-speed chaos generation.

For chaos application systems, many researcher's have shown prototypes of chaos circuits [4]–[7]. One of the most extensively investigated circuits is Chua's chaos circuit which can generate a double-scroll strange attractor [6],[7]. Being distinct from above-mentioned chaos applications, Chua's chaos circuit is often used as an observation tool of chaos since it is one of the rigorous chaos circuits in which a formal proof of the chaotic behavior has been accomplished and can exhibit chaotic behavior with a rich variety of bifurcation phenomena.

In this paper, a generalized Chua's circuit which can generate multiple-scroll strange attractors is proposed. The additional breakpoints in the nonlinear function enable us to generate an n-scroll strange attractor ($n = 1, 2, 3, \ldots$) as well as a double-scroll attractor. The nonlinear function of the proposed circuit can be determined electronically by using supervised learning based on a neuro-fuzzy scheme [9]. Hence, the proposed circuit can exhibit various bifurcation phenomena. Futhermore, the proposed circuit can provide exact reproducibility of chaos signals thanks to the digital realization. Concerning the learning dynamics and the chaotic behavior, the validity of the proposed digital chaos circuit is confirmed by numerical simulations. As a design example of the integrated digital chaos circuit, the proposed circuit realizing the nonlinear function with five breakpoints is implemented onto the FPGA (Field Programmable Gate Array). An FPGA-realization [8] affords economical realization since the flexible logic architectures and the easy CAD tools [8] can be available. The proposed circuit which can generate n-scroll strange attractors ($n = 1, 2, \ldots 4$) is implementable onto a single FPGA chip except for the SRAM.

2. Chaos Model

The equations of the proposed circuit are based on Chua's chaos model. The equations of Chua's chaos model are given by the following equations:

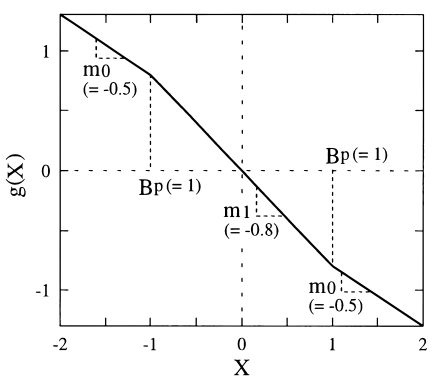


Fig. 1 Piecewise-linear function of Chua's chaos model.

Manuscript received October 1, 1998.
Manuscript revised December 12, 1998.

[†]The author is with the Department of Information and Computer Sciences, Kumamoto National College of Technology, Kumamoto-ken, 861–1102 Japan.

[††]The authors are with the Department of Electrical and Computer Engineering, Kumamoto University, Kumamoto-shi, 860–8555 Japan.

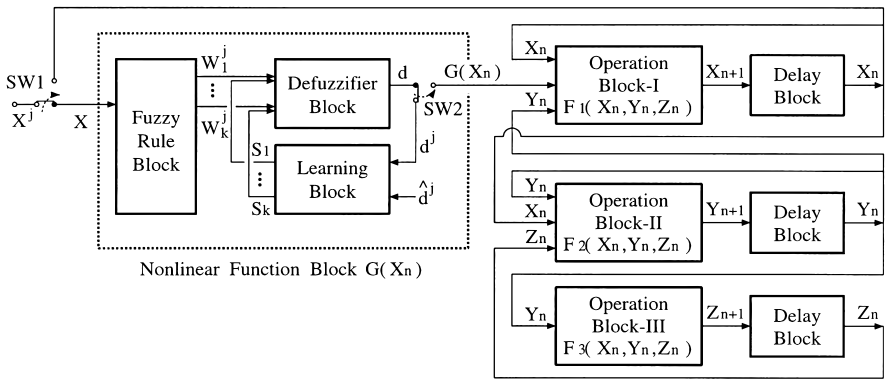


Fig. 2 General circuit architecture of the proposed digital chaos circuit.

$$B^{'}\frac{dx}{dt} = A^{'}(y-x) - g(x),$$
$$C^{'}\frac{dy}{dt} = A^{'}(x-y) + z, \qquad D^{'}\frac{dz}{dt} = -y, \qquad (1)$$

where $A^{'}$, $B^{'}$, $C^{'}$, and $D^{'}$ are variable parameters and $g(x)$ is the piecewise-linear function consisting of two breakpoints given by

$$g(x) = m_0 x + 0.5(m_1 - m_0)|x + B_p| + 0.5(m_0 - m_1)|x - B_p|$$

as shown in Fig. 1. In Eq. (1), we apply the following replacement:

$$\frac{dx}{dt} \Rightarrow \frac{\mathrm{X_{n+1}} - \mathrm{X_n}}{2^E}, \qquad \frac{dy}{dt} \Rightarrow \frac{\mathrm{Y_{n+1}} - \mathrm{Y_n}}{2^E},$$
$$\frac{dz}{dt} \Rightarrow \frac{\mathrm{Z_{n+1}} - \mathrm{Z_n}}{2^E}, \qquad (2)$$

where E is an integer parameter. Then, the corresponding difference equations for the proposed circuit are derived as

$$\begin{aligned}\mathrm{X_{n+1}} &= \mathrm{F_1(X_n, Y_n, Z_n)} \\ &= B\{A(\mathrm{Y_n} - \mathrm{X_n})/2^m - \mathrm{G(X_n)}\}/2^{m-E} + \mathrm{X_n}, \\ \mathrm{Y_{n+1}} &= \mathrm{F_2(X_n, Y_n, Z_n)} \\ &= C\{\mathrm{Z_n} - A(\mathrm{Y_n} - \mathrm{X_n})/2^m\}/2^{m-E} + \mathrm{Y_n}, \\ \mathrm{Z_{n+1}} &= \mathrm{F_3(X_n, Y_n, Z_n)} \\ &= -D\mathrm{Y_n}/2^{m-E} + \mathrm{Z_n}, \end{aligned} \qquad (3)$$

where A, B, C, D, and m are integer parameters on the interval $[0, 2^{m+1}]$ and $\mathrm{G(X_n)}$ is the piecewise-linear function consisting of k $(= 2, 4, 6, \ldots)$ breakpoints. The parameters, A, B, C, and D, satisfy

$$A = [A^{'}2^m], \qquad B = [1/B^{'}], \qquad C = [1/C^{'}],$$
$$\text{and} \qquad D = [1/D^{'}], \qquad (4)$$

where $[\ \cdot\ ]$ is Gauss' notation. In the proposed digital chaos circuit, the nonlinear function $\mathrm{G(X_n)}$ can be determined electronically by using supervised learning based on a neuro-fuzzy scheme. Hence, the proposed circuit can generate an n-scroll strange attractor $(n = 1, 2, 3, \ldots)$ as well as a double-scroll attractor.

The learning rule of the proposed circuit will be described in the following section.

3. Circuit Algorithm

Figure 2 shows the general circuit architecture of the proposed circuit. The synthesis of the proposed circuit is based on Eq. (3). The proposed circuit consists of a nonlinear function block, three operation blocks, and three delay blocks.

In the following subsections, let us consider the circuit algorithm of the functional blocks in Fig. 2.

3.1 Nonlinear Function Block

The nonlinear function block is built with neuro-fuzzy circuit which consists of a fuzzy rule block, a defuzzifier block, and a learning block. The nonlinear function block is in the learning process when the switches SW1 and SW2 are in the lower positions. After the learning process, the switch positions of SW1 and SW2 are reversed. Then, the nonlinear function block functions as $\mathrm{G(X_n)}$.

3.1.1 Fuzzy Rule Block

The inference rules R_i's used in the nonlinear function block are given by the form [9]:

$$R_i : \text{If } x \text{ is } A_i \text{ then } s \text{ is } B_i, \qquad (i = 1, 2, \ldots, k^{'})$$

where x is the input variable and s is the output variable. In these rules, A_i is the fuzzy set defined by the membership function μ_{Ai} and B_i is the fuzzy singleton $1/S_i$ [9]. The matching degree W_i is given by

$$W_i = \mu_{Ai}(x^*), \qquad (i = 1, 2, \ldots, k^{'}) \qquad (5)$$

where x^* is the actual input value. The matching degrees W_i's are the outputs of the fuzzy rule block.

Figure 3 shows the circuit architecture of the fuzzy rule block. In Fig. 3, $\mathrm{MS_1}$, $\mathrm{MS_2}, \ldots, \mathrm{MS_k}$ are discrete

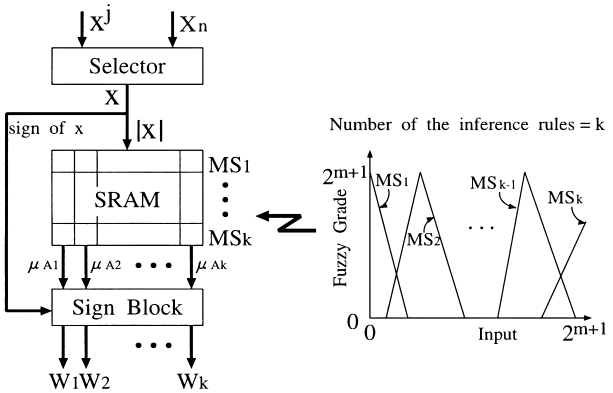


Fig. 3 Circuit architecture of the fuzzy rule block.

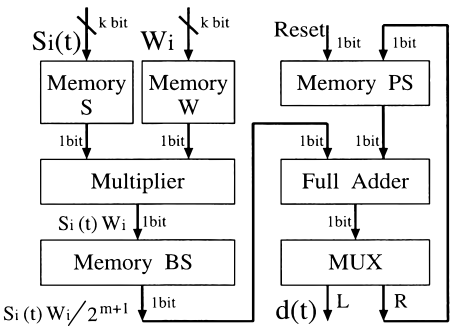


Fig. 4 Circuit architecture of the defuzzifier block.

triangular membership functions whose domain and range are the sets of integers on the interval $[0, 2^{m+1}]$. In the fuzzy rule block, the data of k fuzzy membership functions are stored in the SRAM. Since $G(X_n)$ is a symmetrical function, the number of the membership functions can be reduced from $k^{'}$ to $k^{'}/2+1$ $(=k)$ by setting the signs of W_i's to the same sign of the input x. According to the absolute value of the input x, the SRAM outputs the values of the membership functions, $\mu_1, \mu_2, \ldots, \mu_k$. Corresponding to the sign of the input x, the signs of outputs of the fuzzy rule block, W_i's $(i = 1, \ldots, k)$, are determined.

3.1.2 Defuzzifier Block

In the defuzzifier block, the output fuzzy set, $W_1/S_1 + \ldots + W_k/S_k$, is defuzzified by the center of area (COA) method, where S_i is the singleton's element, / is Zadeh's separator, and + is the union operation [9]. The defuzzified output is given by

$$d(t) = \frac{\sum_{i=1}^{k} S_i(t)\ W_i}{\sum_{i=1}^{k} W_i}. \tag{6}$$

In Eq. (6), to simplify the circuit, the membership functions are chosen such that the summation of the matching degree $\sum_{i=1}^{k} W_i$ becomes the constant value 2^{m+1}. Thus, the division in Eq. (6) can be realized by the bit-shift operation. From Eq. (6), the defuzzified output $d(t)$ is obtained as the output of the defuzzifier block in Fig. 2.

Figure 4 shows the circuit architecture of the defuzzifier block. Firstly, the multiplications in Eq. (6) are realized by the multiplier. The multiplication results $S_i(t)W_i$'s are stored in the memory **BS**. In the memory **BS**, the division in Eq. (6) is realized by the bit-shit operation. Secondly, the summation in Eq. (6) is realized in such manner that

$$\sum_{i=1}^{n} \frac{S_i(t)W_i}{2^{m+1}} + \frac{S_{n+1}(t)W_{n+1}}{2^{m+1}}, \qquad (n \le k-1)$$

where $\sum_{i=1}^{n} S_i(t)W_i/2^{m+1}$ is the partial sum (PS) of the summation in the memory **PS** and $S_i(t)W_i/2^{m+1}$ is the scaled multiplication results in the memory **BS**. When $n < k-1$, multiplexor MUX connects its input to the output terminal R and the output of the full adder is stored in the memory **PS**. When $n = k-1$, MUX connects its input to the output terminal L and the full adder outputs the defuzzified output $d(t)$.

3.1.3 Learning Block

The singleton's elements $S_i(t)$'s are determined in the learning block. In the learning process, the desired outputs $\hat{d}^j$'s are given as the supervisor signals corresponding to the respective sets of sample inputs x^j's, where $\hat{d}^j$'s are user-definable integer parameters on the interval $[-2^{m+1}, 2^{m+1}]$. The learning dynamics occurs such that $J(t) \triangleq \frac{1}{2}\sum_{j=1}^{k}(d^j(t) - \hat{d}^j)^2$ approaches the minimal value. Here, $d^j(t)$ is the actual outputs of the defuzzifier block corresponding to the set of sample inputs x^j. From Eq. (6) and

$$\text{the learning equation}: \ S_i(t+1) - S_i(t) = -\eta \frac{\partial J(t)}{\partial S_i}, \tag{7}$$

the learning dynamics is expressed by the following equation:

$$S_i(t+1) = S_i(t) + \eta \sum_{j=1}^{k} \{(\hat{d}^j - d^j(t))\ W_i^j/2^{m+1}\}, \tag{8}$$

where η is the learning parameter and 2^{m+1} is the constant value corresponding to the summation of the matching degree, $\sum_{i=1}^{k} W_i^j$. In Eq. (8), the choice of the parameter η has to be done to satisfy the necessary and sufficient condition for the convergence of the learning process. Assuming that $W_i^j = 2^{m+1}\delta_{ij}$, which is used in the numerical simulation of the following section, the convergence condition is $0 < \eta < 2$, where δ_{ij} is the Kronecker's delta. In the proposed circuit, the learning parameter η is set to $1/2$ to realize η by the bit-shift operation. From Eq. (8), the singleton's elements $S_i(t)$'s are obtained as the outputs of the learning block. In Eq. (8), the learning process terminates when $S_i(t+1) = S_i(t)$.

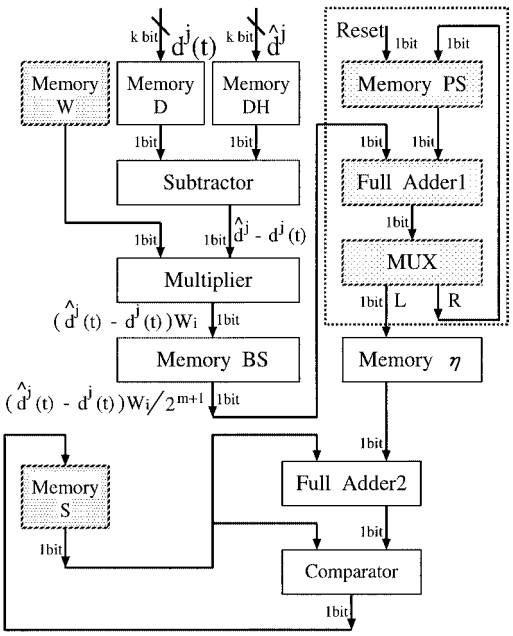


Fig. 5 Circuit architecture of the learning block.

Figure 5 shows the circuit architecture of the learning block. In Fig. 5, the hatched functional blocks can be shared with those in the defuzzifier block. Firstly, the subtraction in Eq. (8) is realized by the subtractor. The outputs $(\hat{d}^j - d^j(t))$'s are provided in a serial manner as the inputs to the multiplier. Secondly, the multiplication in Eq. (8) is realized by the multiplier. The multiplication results $(\hat{d}^j - d^j(t))W_i$'s are stored in the memory **BS**. In the memory **BS**, the division in Eq. (8) is realized by the bit-shift (BS) operation. Thirdly, the summation in Eq. (8) is realized in such manner that

$$\sum_{i=1}^{n} \frac{(\hat{d}^j - d^j(t))W_i}{2^{m+1}} + \frac{(\hat{d}^j - d^j(t))W_{n+1}}{2^{m+1}}, \quad (n \leq k-1)$$

where $\sum_{i=1}^{n}(\hat{d}^j - d^j(t))W_i/2^{m+1}$ is the partial sum (PS) of the summation in the memory **PS** and $(\hat{d}^j - d^j(t))W_{n+1}/2^{m+1}$ is the scaled multiplication result in the memory **BS**. The final result of this summation is stored in the memory η when $n = k-1$. In the memory η, the learning parameter η (=1/2) is realized by the bit-shift operation. Lastly, the addition in Eq. (8) is realized by the full adder2. After the addition is completed, the result of this addition, $S_i(t+1)$, is compared with $S_i(t)$ in the comparator. When $S_i(t+1) \neq S_i(t)$, the singleton's elements $S_i(t+1)$'s are stored in the memory **S**. The learning process terminates when $S_i(t+1) = S_i(t)$.

3.2 Operation Blocks

In Fig. 2, the operation blocks, I, II, and III, function as $F_1(\cdot)$, $F_2(\cdot)$, and $F_3(\cdot)$ (see Eq. (3)), respectively. In the delay blocks, the outputs of the operation blocks are delayed by one cycle and they are fed back to the

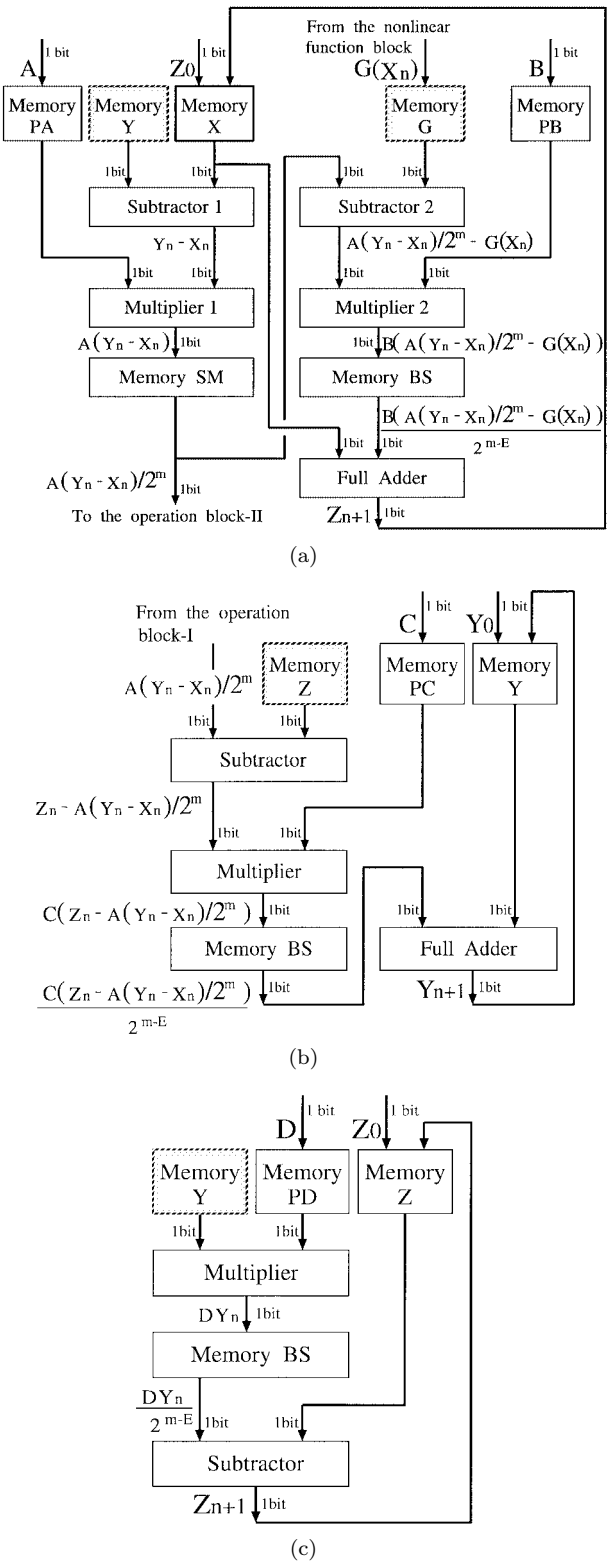


Fig. 6 Circuit architecture of the operation blocks. (a) Operation block-I. (b) Operation block-II. (c) Operation block-III.

inputs of proper operation blocks.

Figure 6 shows the circuit architecture of the operation blcoks. The operations of $F_1(\cdot)$, $F_2(\cdot)$, and $F_3(\cdot)$ are realized by the circuit shown in Figs. 6 (a), (b), and (c), respectively. The operations of these functions are performed in a serial manner. In Figs. 6 (a), (b), and (c), the hatched functional blocks are shared with those of the other operation blocks.

4. Numerical Simulations

To confirm the validity of the circuit algorithm shown in Sect. 3, numerical simulations are performed. As the examples of the multiple-scroll strange attractors, a triple-scroll and a quadruple-scroll strange attractors are realized. In the case where the number of the inference rules $k \geq 5$, the proposed circuit can generate these strange attractors. In the numerical simulations, the following membership functions are used.

• Membership functions:

$$\text{MS1} : \mu_{A1}(x) = 2^{m+1} \ominus 10x,$$

$$\text{MS2} : \mu_{A2}(x) = \begin{cases} 10x & \text{if } x < 2^m/5, \\ 3 \times 2^m - 5x & \text{if } x \geq 2^m/5, \end{cases}$$

$$\text{MS3} : \mu_{A3}(x) = \begin{cases} 5x \ominus 2^m & \text{if } x < 3 \times 2^m/5, \\ (5 \times 2^m) \ominus 5x & \text{if } x \geq 3 \times 2^m/5, \end{cases}$$

$$\text{MS4} : \mu_{A4}(x) = \begin{cases} 5x \ominus (3 \times 2^m) & \text{if } x < 2^m, \\ 2^{m+2} \ominus 2x & \text{if } x \geq 2^m, \end{cases}$$

$$\text{MS5} : \mu_{A5}(x) = 2x \ominus 2^{m+1}, \tag{9}$$

where x is the input variable and $\ominus$ is the bounded-difference operator. Figure 7 shows the membership functions obtained by Eq. (9). Obviously, the membership functions shown in Fig. 7 satisfy the condition, $W_i^j = 2^{m+1}\delta_{ij}$.

In the proposed circuit, the quantization effect which is caused by the parameters, m and E, affect the state of the strange attractor. Here, let's discuss the

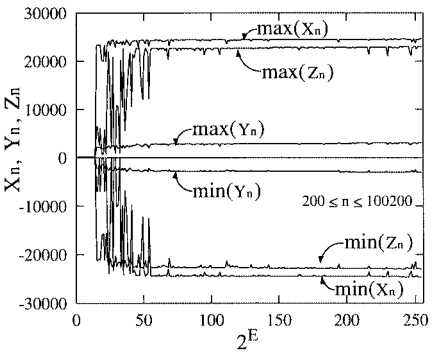


Fig. 9 Finite bit-length effect on the edge of the bifurcation diagram obtained by the quadruple-scroll strange attractor.

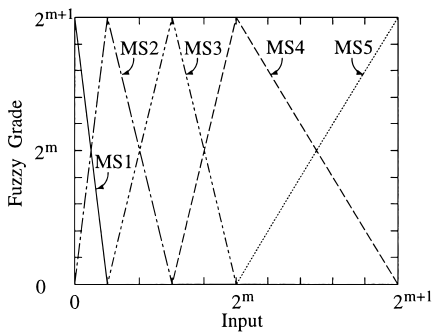


Fig. 7 Membership functions used in the numerical simulations.

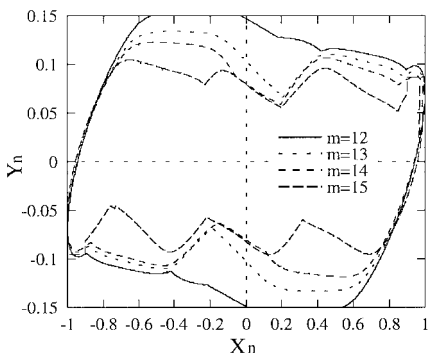


Fig. 8 Finite bit-length effect on the edge of the quadruple-scroll strange attractor.

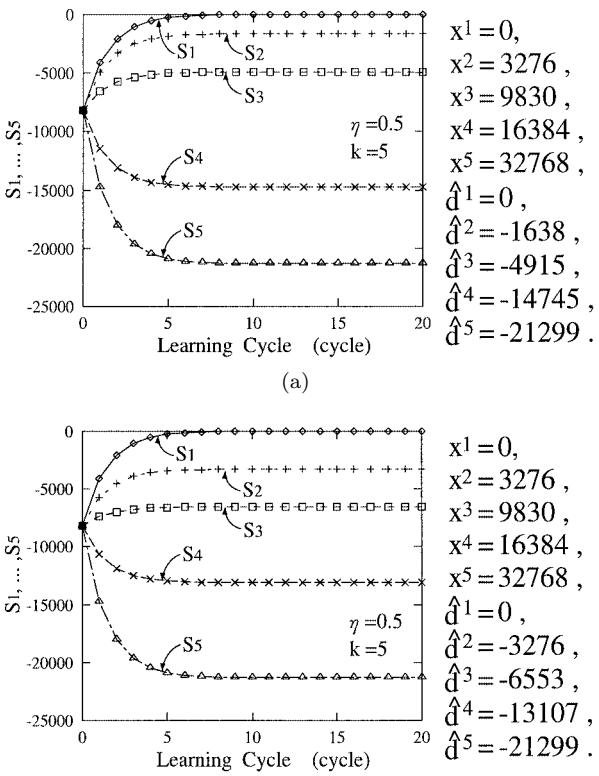


Fig. 10 Simulated convergence behavior of the singletons in the learning process. (a) Triple scroll. (b) Quadruple scroll.

quantization effect to the strange attractor. To save space, the analysis concerning the triple-scroll attractor is omitted. Figure 8 shows the edge of the normalized quadruple-scroll strange attractor when $m \leq 15$. This shows that the proposed circuit can generate the strange attractors when $m \geq 12$. In the proposed circuit, the parameter m was set to 14. Figure 9 shows the edge of the bifurcation diagram obtained by the quadruple strange attractor. This figure shows that the proposed circuit can generate the strange attractor when $E \geq 6$. In the proposed circuit, the parameter E was set to 8. Figure 10 shows the convergence behaviors of the singletons of the proposed circuit. The parameters, x^j's and d^j's, are set to the values shown in Fig. 10. In Figs. 10 (a) and (b), the singletons' element values converged to their final values after 10 learning cycles. Figure 11 shows the examples of the piecewise-linear functions of the proposed circuit. In Fig. 11, the errors from the ideal nonlinear functions which are used to give the supervisor signals were less than 2.5%. Figure 12 shows the examples of the strange attractor obtained from the generated nonlinear functions shown in Fig. 11. In Fig. 12, the initial values were set to 128.

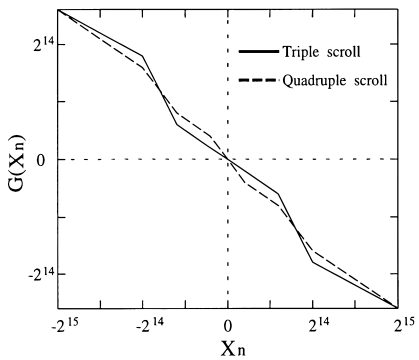


Fig. 11 Piecewise-linear functions of the proposed circuit.

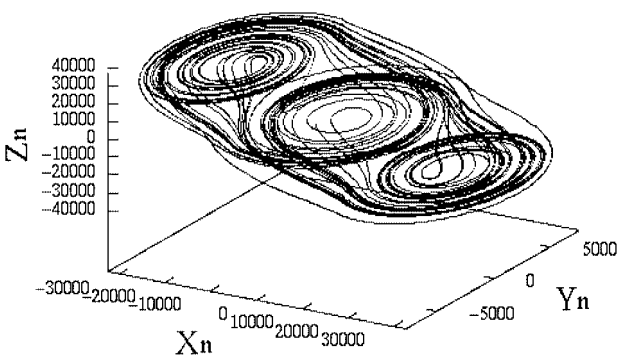


Fig. 12 Simulated strange attractors of the proposed circuit. (a) Triple scroll. (b) Quadruple scroll.

5. Theoretical Analysis for the Strange Attractors

The equilibrium points Eq_i in the strange attractors of Fig. 12 satisfy the following conditions.

$$\begin{aligned} &\mathrm{X_{n+1}} - \mathrm{X_n} = 0, \qquad \mathrm{Y_{n+1}} - \mathrm{Y_n} = 0, \\ &\text{and} \qquad\qquad\quad \mathrm{Z_{n+1}} - \mathrm{Z_n} = 0. \end{aligned} \tag{10}$$

From Eq. (10), the equilibrium points Eq_i of the proposed circuit are given by the following equations:

• Equilibrium points for a triple-scroll attractor:

$$\begin{aligned} Eq_1 &= \left(\frac{5\times 2^{2m-1}}{2^{m+1}-5A},\ 0,\ \frac{-5A\times 2^{m-1}}{2^{m+1}-5A}\right), \\ Eq_2 &= \left(\frac{3\times 2^{2m}}{5A-15\times 2^{m-1}},\ 0,\ \frac{-3A\times 2^{m}}{5A-15\times 2^{m-1}}\right), \\ Eq_3 &= (0,\ 0,\ 0), \\ Eq_4 &= \left(\frac{-3\times 2^{2m}}{5A-15\times 2^{m-1}},\ 0,\ \frac{3A\times 2^{m}}{5A-15\times 2^{m-1}}\right), \\ Eq_5 &= \left(\frac{-5\times 2^{2m-1}}{2^{m+1}-5A},\ 0,\ \frac{5A\times 2^{m-1}}{2^{m+1}-5A}\right), \end{aligned} \tag{11}$$

• Equilibrium points for a quadruple-scroll attractor:

$$\begin{aligned} Eq_1 &= \left(\frac{-3\times 2^{2m}}{10A-5\times 2^{m}},\ 0,\ \frac{3A\times 2^{m}}{10A-5\times 2^{m}}\right), \\ Eq_2 &= \left(\frac{-2^{2m}}{5\times 2^{m}-5A},\ 0,\ \frac{A\times 2^{m}}{5\times 2^{m}-5A}\right), \\ Eq_3 &= \left(\frac{-2^{2m}}{10A-5\times 2^{m}},\ 0,\ \frac{A\times 2^{m}}{10A-5\times 2^{m}}\right), \\ Eq_4 &= (0,\ 0,\ 0), \\ Eq_5 &= \left(\frac{2^{2m}}{10A-5\times 2^{m}},\ 0,\ \frac{-A\times 2^{m}}{10A-5\times 2^{m}}\right), \\ Eq_6 &= \left(\frac{2^{2m}}{5\times 2^{m}-5A},\ 0,\ \frac{-A\times 2^{m}}{5\times 2^{m}-5A}\right), \\ Eq_7 &= \left(\frac{3\times 2^{2m}}{10A-5\times 2^{m}},\ 0,\ \frac{-3A\times 2^{m}}{10A-5\times 2^{m}}\right). \end{aligned} \tag{12}$$

In Eqs. (11) and (12), the proposed circuit must have 3 and 4 stable equilibrium points to generate a triple-scroll and a quadruple-scroll attractors, respectively.

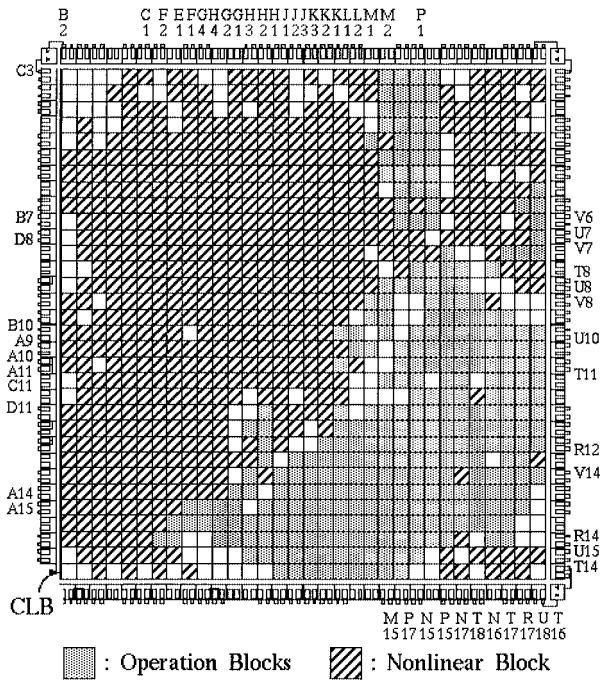


Fig. 13 The functional block allocation view of the FPGA implementing the proposed circuit.

The stable equilibrium points satisfy the following condition:

$$|\det\{J(Eq_i)\}| < 1, \tag{13}$$

where

$$J(\mathrm{X_n}) = \begin{bmatrix} 1 - \frac{AB}{2^{2m-E}} - \frac{B}{2^{m-E}}\frac{\partial \mathrm{G}(\mathrm{X_n})}{\partial \mathrm{X_n}} & \frac{AB}{2^{2m-E}} & 0 \\ \frac{AC}{2^{2m-E}} & 1 - \frac{AC}{2^{2m-E}} & \frac{C}{2^{m-E}} \\ 0 & -\frac{D}{2^{m-E}} & 1 \end{bmatrix}$$

From Eqs. (11)–(13), the equilibrium points, Eq_1, Eq_3, and Eq_5, in Fig. 12 (a) are stable. And the equilibrium points, Eq_2, and Eq_4, in Fig. 12 (a) are unstable. The equilibrium points, Eq_1, Eq_3, Eq_5, and Eq_7, in Fig. 12 (b) are stable. And the equilibrium points, Eq_2, Eq_4, and Eq_6, in Fig. 12 (b) are unstable. Thus, the proposed circuit generates a triple-scroll and a quadruple-scroll attractors in Fig. 12. The coordinates of the center of the strange attractors are given by the following equations.

• Coordinates of the center of the triple-scroll attractor:

$$\begin{aligned} Eq_1 &= ([-(10/7) \times 2^{14}], 0, [(15/14) \times 2^{14}]), \\ Eq_3 &= (0, 0, 0), \\ Eq_5 &= ([(10/7) \times 2^{14}], 0, [-(15/14) \times 2^{14}]), \end{aligned} \tag{14}$$

• Coordinates of the center of the quadruple-scroll attractor:

$$\begin{aligned} Eq_1 &= ([-(6/5) \times 2^{14}], 0, [(9/10) \times 2^{14}]), \\ Eq_3 &= ([-(2/5) \times 2^{14}], 0, [(3/10) \times 2^{14}]), \\ Eq_5 &= ([(2/5) \times 2^{14}], 0, [-(3/10) \times 2^{14}]), \\ Eq_7 &= ([(6/5) \times 2^{14}], 0, [-(9/10) \times 2^{14}]), \end{aligned} \tag{15}$$

where [·] is Gauss' notation.

Table 1 Location of input/output pins.

Address signals for the SRAM	U8,T14,R14,U18,R17,N17,B2,T8,V7, V8,P15,N15,P17,N16,U15,T17,T18
Data signals for the SRAM	D8,C11,A9,D11,K2,L2,J1,J2,H1, H2,K1,J3,L1,K3,B10,A11,A10
Read signals for the SRAM	G2,A15,F1,A14,G1
Desired outputs	G4,E1,F2,H4,C1
Sample inputs	H3,M15,M2,M1,B7
Clock signal	C3
Reset signal	T16
Parameters	U10,V6,U7,T11
Outputs, $\mathrm{X_n}, \mathrm{Y_n}, \mathrm{Z_n}$	V14,R12,P1

Table 2 Results of the circuit design.

Device			
4025ePG223	Occupied CLBs	883/1024	(86%)
	Bonded I/O pins	58/192	(30%)
	Maximum pin delay	68	(ns)
	Average connection delay	53	(ns)
	Highest clock frequency	14	(MHz)

6. Circuit Design by Using Verilog—HDL

As a design example of the integrated digital chaos circuit, the FPGA chaos circuit which can generate n-scroll attractors ($n = 1, 2, \ldots 4$) was designed by using CAD tool, Verilog–HDL [8]. In this design, the number of the inference rules k was set to 5 and the parameter m was set to 14. And SRAM is excluded from the chip as an external memory. Figure 13 shows FPGA's functional block allocation result for the synthesized circuit. The proposed circuit was synthesized by the logic synthesizer with Xilinx FPGA logic unit library XC4000e which targets FPGA XC4025ePG223 [8]. The FPGA XC4025ePG223 has 1024 CLBs (Configurable Logic Block) and 192 IOBs (Input/Output) [8]. The input/output pin locations are shown in Table 1. The results of the FPGA design are summarized in Table 2. The synthesized circuit can generate quasi-chaos signals after 583 ms from start-up when a 10 MHz clock is used.

7. Conclusion

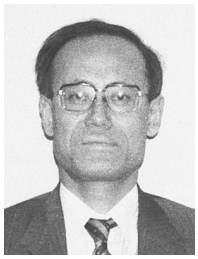
A new digital chaos circuit which can generate multiple-scroll strange attractors has been proposed in this paper. In the neuro-fuzzy based nonlinear block, the nonlinear function is determined by supervised learning. Hence, the proposed circuit can exhibit various bifurcation phenomena. The learning dynamics and the finite

bit-length effect on the strange attractors are analyzed by numerical simulations. As a design example of the proposed digital chaos circuit, the FPGA chaos circuit which can generate n-scroll attractors ($n = 1, 2, \ldots 4$) was designed by using CAD tool, Verilog–HDL. The timing simulations of the synthesized FPGA chaos circuit showed that the proposed circuit features efficient supervised learning of nonlinear functions and high-speed chaos generation. The proposed circuit which can generate n-scroll attractors ($n = 1, 2, \ldots 4$) can be implemented onto a single FPGA except for the SRAM.

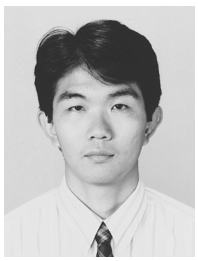
References

[1] T. Kohda and A. Tsuneda, "Pseudonoise sequences by chaotic nonlinear maps and their correlation properties," IEICE Trans. Commun., vol.E76-B, no.8, pp.855–862, Aug. 1993.
[2] H. Nozawa, "A neural network model as a globally coupled map and applications based on chaos," CHAOS, vol.2, no.3, pp.377–386, American Institute of Physics, 1992.
[3] L. Nemes and T. Roska, "A CNN model of oscillation and chaos in ant colonies: A case study," IEEE Trans. Circuits & Syst., vol.42, no.10, pp.741–745, Oct. 1995.
[4] J.Černák, "Digital generations of chaos," Physics Lett. A, no.13, pp.151–160, May 1996.
[5] T. Aida, N. Otani, and P. Davis, "Digital implementation of a nonlinear delayed-feedback system," IEEE Trans. Circuits & Syst., vol.41, no.3, pp.238–242, March 1994.
[6] J.M. Cruz and L.O. Chua, "A CMOS IC nonlinear resistor for Chua's circuit," IEEE Trans. Circuits & Syst., vol.39, no.12, pp.985–995, Dec. 1992.
[7] J.A.K. Suykens and J. Vandewalle, "Generation of n-double scrolls ($n = 1, 2, 3, 4, \ldots$)," IEEE Trans. Circuits & Syst.-I, vol.40, no.11, pp.861–867, Nov. 1993.
[8] Galileo HDL synthesis manual, Exemplar Logic Inc., 1995.
[9] K. Tsukano, T. Inoue, and J. Nohara, "Design and analysis of a current-mode analog neuro-fuzzy singleton controller with supervised learning," Proc. JTC-CSCC'95, Kumamoto, Japan, pp.655–658, July 1995.

Kei Eguchi was born in Saga, Japan, on February 17, 1972. He received the B.E., the M.E., and the D.E. degree from Kumamoto University, Kumamoto, Japan in 1994, 1996, and 1999, respectively. Presently he is a lecturer in Kumamoto National College of Technology. His main research interests are nonlinear circuits and systems.



Takahiro Inoue received the B.E. and the M.E. degree from Kumamoto University, Kumamoto, Japan in 1969 and 1971, respectively, and the D.E. degree from Kyushu University, Fukuoka, Japan in 1982. From 1971 to 1974, he worked as a Research Staff at Hitachi, Ltd., Yokohama, Japan. In 1975, he joined the faculty of Kumamoto University, where he is now a Professor. Dr. Inoue's current research interests include switched-capacitor/switched-current filters, continuous-time IC filters, low-power/low-voltage analog integrated circuits, and analog/digital intelligent circuits and systems. He is a member of the Institute of Electrical and Electronics Engineers and he served as an Associate Editor of Transactions on Fuzzy Systems during 1994–1996. He is also a member of the Institute of Electrical Engineers of Japan, the Japanese Neural Network Society, and the Physical Society of Japan.



Akio Tsuneda received the B.E., M.E. and D.E. degrees in Computer Science and Communication Engineering from Kyushu University, Fukuoka, Japan, in 1990, 1992, and 1995, respectively. From 1995 to 1996, he was with the Department of Computer Science and Communication Engineering, Kyushu University. He is currently an Associate Professor of Electrical and Computer Engineering at Kumamoto University, Japan. His research interests include nonlinear dynamical systems, pseudonoise sequences, and digital communications. He is a member of the Institute of Electrical and Electronics Engineers and the Institute of Electrical Engineers of Japan.