A New Negative Feedback based Poly-Silicon AMOLED Pixel Circuit
With Highly Linear Transfer Characteristics

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Abstract: A new Poly-Silicon pixel circuit is described which is able to achieve highly linear transfer characteristics by reducing the Kink effect in TFT through use of negative feedback. Simulation results show that drive currents as high as 20µA can be achieved with linearity better than ±5%.

1. Introduction.

Organic light emitting diode (OLED) displays are being increasingly viewed as the flat panel technology of the future due to their several advantages including wide viewing angle, fast response time, thin size and low cost [1-3]. These displays can be built either as passive matrix panels consisting only OLEDs or active matrix panels (AMOLED) in which the OLED is integrated with thin film transistors (TFT) in a suitable manner. Passive matrix displays are simpler and cheaper but they suffer from several problems which limits their range of applicability to low information content displays [4-6]. Although active matrix displays are more complex and expensive, they have superior characteristics and are necessary for high resolution applications. AMOLED displays can be built by integrating either amorphous Silicon TFTs [7-8] or Poly-silicon TFTs [9-11] with the light emitting diode. Poly-Silicon is the preferred technology because of its higher current driving capability as a result of better carrier mobility. A pixel circuit can be voltage or current driven depending on the nature of applied input signal. The current driven pixel circuit is preferred because the light output in an OLED varies linearly with the drive current.

The central problem in the design of current driven pixel circuit is to ensure that the OLED is driven with a specified input current not only during the time when the OLED is addressed but during the rest of the frame period as well when the OLED is not being addressed. There are two important factors which cause the OLED current to deviate from the input current. The first is the large variation in TFT threshold voltage and the second is the Kink effect in the Poly-Silicon TFT characteristics. The first problem has been solved by using pixel circuits which belong to the class of switched-current memory circuits [12], an example of which is shown in Figure 1. In the addressing phase (f is high), the input programming current flows through TFT4 and also charges the capacitor Cs to a suitable value of gate voltage required for the flow of this current. Because the gate voltage tracks the threshold voltage of TFT4, the effect of variation in threshold voltage is practically cancelled in this circuit. During the non-addressing phase (f is low), the gate voltage on the capacitor tends to maintain the same current through TFT4 and OLED. Besides insensitivity to threshold voltage variation, another important characteristic that these current-programmed AMOLED pixel circuits must exhibit is small mismatch between the output current during the non-addressing phase and the input programming current. Ideally the relationship between the two current should be linear. However, the Kink effect in the characteristics of Poly-Silicon TFT makes the characteristic highly nonlinear as explained in the next section. In this work, a new pixel circuit is proposed which is able to achieve highly linear transfer characteristics by reducing the Kink effect in the TFT through use of negative feedback.
2. New Pixel Circuit

In the absence of kink effect, the current in saturation mode of operation is almost independent of drain-to-source voltage and is determined largely by the gate-to-source voltage. This makes the design of pixel circuit relatively simpler because it has to be ensured that only gate-to-source voltage remains the same in both addressing and non-addressing periods. The drain-to-source voltages can be widely different as long as they are larger than the saturation voltage. The presence of a kink in I-V characteristics means that current is sensitive to drain-to-source voltage as well. This makes the design task harder because of the necessity of keeping both gate and drain voltages constant. In order to illustrate the impact of Kink effect on the transfer characteristics of the pixel, the circuit shown in Figure 1 was simulated with AIMSPICE simulator using the poly-silicon TFT model (Level-16 ASIA2) with parameters used in earlier studies [9]. A Supply voltage of 14V, \( C_s = 2pF \), n-type TFT sizes of 10\( \mu \)m/10\( \mu \)m and OLED of area 100\( \mu \)m x 100\( \mu \)m were assumed. The OLED model consisting of a nonlinear current source in parallel with a capacitor was chosen such that the I-V characteristics predicted by it matched well with state-of-the-art experimentally reported data. Figure 2 shows the nonlinearity \( \left( \frac{(I_{out} - I_{data})}{I_{out}} \right) \times 100 \) in transfer characteristics. It can be seen that the nonlinearity is very large at \( I_{data} = 1\mu A \) and steadily decreases as the current increases.

It is easy to appreciate the reasons for this nonlinearity using figure 3 which shows the \( I_{ds} \) vs \( V_{ds} \) characteristics of TFT\(_4\). At \( I_{data} = 1\mu A \), the drain-to-source voltage of of TFT\(_4\) during the addressing period \( (V_{ds}^{add}) \) is 3.66V while during the non-addressing phase \( (V_{ds}^{nonadd}) \) it is 9.66V. Because of the presence of a large kink effect the current at the two \( V_{ds} \) values is very different. As the input data current is increased, \( V_{ds}^{add} \) increases because it is same as gate-to-source voltage and higher gate voltage is required for larger current to flow. On the other hand \( V_{ds}^{nonadd} \) decreases due to increased drop across the OLED and TFT\(_3\). This results in two \( V_{ds} \) values coming closer resulting in smaller mismatch between input and output current. The mismatch becomes minimum at the maximum current of 20\( \mu \)A. By changing the TFT sizes, the nonlinearity can be reduced at \( 1\mu A \) but only at the expense of increased nonlinearity at 20\( \mu \)A. To reduce the nonlinearity over the entire range of input current, the kink effect in TFT must be reduced. One of the ways of doing this is by increasing the channel length of TFT\(_4\) in the pixel circuit. However, the channel length required to achieve small nonlinearity can turn out to be prohibitively large in view of the large kink present in the TFT characteristics. In order to alleviate this problem, we propose in the present work use of negative feedback in addition to increasing channel length for reducing kink in the TFT characteristics. It is well known that negative feedback can reduce nonlinearity and is widely used for example in transistor amplifiers to achieve low distortion. Negative feedback can be easily incorporated by connecting a resistor in series with source of TFT\(_4\) as shown in Figure 4(a). An increase in drain current due to kink effect results in increased voltage drop across the resistor. This reduces the gate-to-source voltage of TFT which tends to reduce the current. As a result of this negative feedback the variation in drain current due to Kink effect is reduced. An easy way of implementing a resistor is to employ a TFT with its drain-gate shorted together as shown in Figure 4(b). Figure 5 compares the IV characteristics of single TFT and TFT with negative feedback. It can be seen that the Kink effect is significantly reduced as a result of application of negative feedback.

By incorporating negative feedback in the manner explained above, we obtain a new 5-TFT pixel circuit shown in Figure 6 which is only marginally more complex than the conventional 4-TFT circuit. To obtain an optimal performance of the pixel circuit, the TFT sizes have to be carefully chosen. It can be seen from Figure 5 that there is region of I-V characteristics where the current varies relatively little with the drain-to-source voltage. As a result, TFT sizes should be chosen so
as to ensure that TFT$_4$ operates largely in this constant current region. Since nonlinearity is almost a monotonic function of current, it is sufficient to ensure that nonlinearity is below the specified value at the two extreme values of current. The design methodology used to obtain TFT sizes can be summarized as follows. Initially all TFT sizes are kept at their minimum value (W/L = 10µm/10µm for the present case). The sizes of TFT$_1$ and TFT$_2$ are kept constant at this value because they have very little impact on the characteristics of pixel circuit. The goal of design process is to determine the optimum sizes of the remaining three TFTs. Circuit simulations are carried out to determine nonlinearity at the minimum value of input programming current. If the nonlinearity happens to be below the required value, then nonlinearity is evaluated at the other extreme of current. However, if the level of nonlinearity is unacceptable then the TFT sizes are altered to meet the target. A high value of nonlinearity implies either that the suppression of kink effect by negative feedback is insufficient or that the drain-to-source voltages of TFT$_4$ during the addressing and non-addressing periods are too far apart. At the minimum input data current the drain-to-source voltage during the addressing period ($V_{ds}^{add}$) is smaller than the drain-to-source voltage during the non-addressing period ($V_{ds}^{nonadd}$). To bring the two $V_{ds}$ closer together, there are two options; either increase $V_{ds}^{add}$ or reduce $V_{ds}^{nonadd}$. Noticing that $V_{gs}^{add}$ is same as $V_{gs}^{add}$, an increase in $V_{ds}$ can be achieved by simply increasing the channel length of TFT$_4$. This has the additional benefit that increase in channel length further reduces the Kink effect in the TFT characteristics. Thus the channel length of TFT$_4$ is gradually increased and nonlinearity at the minimum data current is monitored till it drops below the specified value. Next the circuit is simulated at the maximum value of input data current and nonlinearity is measured again. A high value of nonlinearity again implies that the drain-to-source voltages are too far apart. At the maximum current, it is often the case that drain-to-source voltage during the addressing period ($V_{ds}^{add}$) is larger than the drain-to-source voltage during the non-addressing period ($V_{ds}^{nonadd}$). The two voltages can be brought closer together by reducing $V_{ds}^{add}$ or increasing $V_{ds}^{nonadd}$. $V_{ds}^{add}$ can be reduced by increasing the width of TFT$_4$. The drain-to-source voltage in the non-addressing mode can be expressed as:

$$V_{ds}^{nonadd}(TFT_4) = V_{DD} - V_{OLLED} - V_{ds}(TFT_3) - V_{ds}(TFT_5)$$

This expression shows that $V_{ds}^{nonadd}$ can be increased by reducing the $V_{ds}$ drop across TFT$_3$ and TFT$_5$. This can be done by increasing the widths of TFT$_3$ and TFT$_5$. Thus increase in widths of TFT$_3$, TFT$_4$, and TFT$_5$ all bring the $V_{ds}$ closer together. The widths of TFT$_3$, $TFT_4$, and TFT$_5$ are taken to be same and varied till nonlinearity drops below the specified threshold value. Increase in widths of TFT$_3$, $TFT_4$, and TFT$_5$ may lead to larger nonlinearity at the lower current value so the process is iterated till nonlinearity at both extremes falls below the specified threshold.

### 3. Results and Discussion

Using the methodology discussed in the previous section, design of 5TFT pixel circuit was carried out for a current range of 120µA at a supply voltage of 14V. The design was done to reduce the nonlinearity under ±5% over the entire current range. The level of clock voltage ($\phi, \bar{\phi}$) was 0?14V. The optimum TFT sizes obtained are (W/L)$_3$ =36µm/22µm, (W/L)$_3$ = (W/L)$_5$ =36µm/10µm and (W/L)$_2$ = (W/L)$_1$ = 10µm/10µm for $V_{DD}$=14V. Fig. 7 shows the results obtained from simulations with AIMSPICE simulator using the poly-silicon TFT model (Level-16 ASIA2). It can be seen that the match between input and output currents is excellent over the entire current range for this pixel circuit (i.e. ±5%).

### 4. Conclusion

To summarize, a new 5-TFT pixel circuit has been developed which provides very good linearity in the transfer characteristic of the pixel circuit using the concept of negative feedback. It is
shown that nonlinearity under ±5% can be obtained with only marginal increase in circuit complexity.

5. References

**Fig. 3** $I_{DS}$ vs $V_{DS}$ characteristic of n-type Poly-Si TFT

**Fig. 4** (a) TFT with resistance in feedback, (b) TFT with negative feedback using another TFT as a resistor

**Fig. 5** Normalized $I_{DS}$-$V_{DS}$ characteristic of a single TFT and "TFT with negative feedback (Fig. 4b)"

**Fig. 6** New 5-TFT current programmed AMOLED pixel circuit

**Fig. 7** $I_{in}$ vs. $I_{out}$ transfer characteristics for the five TFT AMOLED pixel circuit, where $(W/L)_1=(W/L)_2=10\mu m/10\mu m$, $(W/L)_3=36\mu m/22\mu m$, $(W/L)_4=(W/L)_5=36\mu m/10\mu m$ for $V_{DD}=14V$