

OBJECTIVE

- To obtain a summer intern position as an Analog or RF circuit designer.
- To gain experience in real world product or development IC design.
- To get familiar with potential future employer.

EDUCATION

- University of California, Berkeley
PhD in Integrated Circuits with minor in Communication
Expected Graduation Date: May 2011
GPA: 3.88
- University of California, Berkeley
B.S. in EECS with minor in Physics
Fall 2004 — May 2007
GPA: 3.964
- De Anza College
Engineering Major
Spring 2002 — Summer 2004
GPA: 4.000

CURRENT RESEARCH PROJECT

- Low Power Pipelined ADC utilizing passive inter-stage Gain
Target of performance: 10b 200Ms/s ADC with < 2mW
Device currently under testing

COURSEWORK & KNOWLEDGE

- Analog and Mixed-signal IC
- Radio Frequency IC
- Digital IC
- Digital Communication
- E & M
- Device Physics & Micro-fabrication

CLASS PROJECTS

- Low power switch capacitor OTA with 5ns settling time and 0.1% settling error using 0.18um CMOS technology
- 7b 400Ms/s Flash ADC using 90nm CMOS PTM
- 2GHz 60dB voltage gain and 70dBm IIP3 VGA with 90nm CMOS
- Sense amplifier offset compensation techniques for SRAM applications
- 64X32 Register File using 0.25um CMOS

TOOLS AND INSTRUMENTS

- Circuit Simulator (HSPICE, Spectre, SpectreRF, Cadence, Virsuo layout, Schematic)
- Experience in PCB design
- Matlab
- E&M simulator (HFSS, Q3D)
- Circuit Testing Equipments (Signal Generator, pattern generator, logic analyzer, spectral analyzer, etc.)
- Basic Micro Fabrication lab skill