

A Survey Study of Digital Background Calibration Techniques for Pipeline A/D Converter

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Abstract - Digital background calibration is considered the most promising solution to combat with analog imperfections in pipelined A/D converters in deep submicron processes. Many drastically different calibration approaches have gained their immense popularities. In general, they can be classified into one of the three schools, which are: (a) Calibrate using a slow but accurate ADC [1], (b) Split ADC approach [2], (c) Statistics bases calibration [4], [5], [6]. In this paper, each of this approach is studied in detail and their benefits and limitations are explored. Their performances are comparatively analyzed using Matlab.

I. Introduction

The motivation to use digital calibration is the continued scaling of CMOS technology, which has created a drastic performance gap between analog circuits and digital circuits. On one hand, DSP performance has been greatly benefited due to higher switching speed and lower supply voltage of the transistor, resulting in faster, more complex, more power efficient digital core. On the other hand, scaling has adversely affected analog circuits due to lower transistor intrinsic gain and worse device matching. This trend has reached the point where high gain amplifiers are almost extinct in sub-90nm process. At the point, digital assisted calibration becomes a natural solution to combat these analog imperfections.

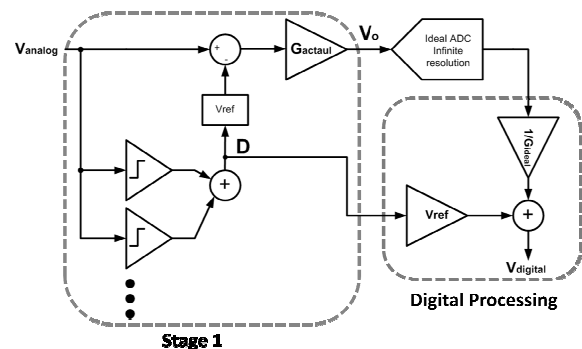
The function of digital background calibration is to measure analog impairments (i.e. capacitor mismatch, finite OTA gain, etc.) and compensate them using DSP processor in

digital domain. In practice, the dominant effect of these impairments presents itself linear stage gain error of the pipeline stages. If not dealt with, this error can causes discontinuities in V_{analog} vs. $V_{digital}$ curve, which in turns gives rise to harmonic distortions. One key feature of digital background calibration is to correct this error continuously in time without interrupting normal operation of the A/D converter.

In this paper, system-level architectural implementations of each of the 3 approaches are discussed in Analysis section. One representative work in each is analyzed in detail. Their performances are compared using Matlab simulation.

II. Analysis

I. Understanding Gain Error



Schematic 1. Simplified Block Diagram for Pipelined ADC

As mentioned earlier, the dominant effect of analog impairments is linear and nonlinear stage gain error. At first glance, linear gain error should not introduce any distortion to most systems. However, it is not true in pipelined A/D. To understand the effect of

linear gain error, consider the first stage of the pipeline, and assume the backend has infinite resolution (*schematic 1*). Then,

$$V_o = G_{actual} \cdot [V_{i, ana log} - D \cdot V_{ref}],$$

where G_{actual} is the actual stage gain, and D is the digital decision of the stage. Suppose there is no calibration, and the real value of is G_{actual} unknown. In digital domain, ideal gain of G_{ideal} is implicitly assumed. Then, digital interpreted input becomes:

$$V_{i, digital} = \frac{V_o}{G_{ideal}} + D \cdot V_{ref}$$

$$V_{i, digital} = \frac{G_{actual}}{G_{ideal}} \cdot V_{i, ana log} + \left(1 - \frac{G_{actual}}{G_{ideal}}\right) \cdot D \cdot V_{ref} \quad (1)$$

From equation (1), if $G_{ideal} = G_{actual}$, $V_{i, ana log} = V_{i, digital}$. When $G_{ideal} \neq G_{actual}$, the first term is a scaled version of analog input voltage, while the second term is a “stair-case” function whose transition points depend on input analog voltage. This causes discontinuities in $V_{i, ana log}$ vs. $V_{i, digital}$ plot, as illustrated in Figure 1. These discontinuities must be eliminated otherwise it distorts the signal.

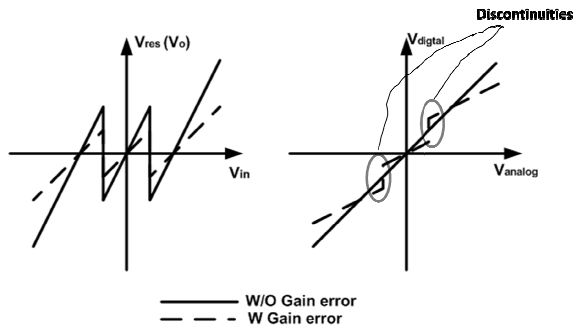


Figure 1. Illustration of Stage Gain Error

II. Differential Approaches For Calibration

(a) Reference ADC Approach [1]

The most conceptually simple approach for calibration is to use a slow but accurate ADC as a reference to calibrate a fast but inaccurate ADC. In this approach, the accurate value of V_{in}

is measured by slow ADC which runs at a fraction of sampling rate as the ADC under calibration, therefore minimizing the power overhead introduced by adding this reference ADC. The slow but accurate ADC (from now on, referred to as reference ADC) output serves as reference to the main ADC under calibration, and gain adjustment are updated at the conversion rate of the slow reference ADC.

Take an N -stage pipelined ADC for example. Suppose the actual gain of each stage is $G(k)$, the digital decision for k^{th} stage is $D(k)$. input to k^{th} stage is $V_o(k)$ the residue output of k^{th} stage is $V_o(k)$, and $V_o(k) = V_i(k+1)$ for intermediate stages. Then we have:

$$V_i(k) = \frac{1}{G(k)} \cdot V_i(k+1) + \frac{V_{ref}}{G(k)} \cdot D(k)$$

Using this recursive equation, we can derive the overall input log voltage as a function of $G(k)$ and $D(k)$:

$$V_i = \sum_{k=1}^N \alpha(k) \cdot D(k) + \prod_{k=1}^N \frac{1}{G(k)} \cdot V_o(N), \quad (2)$$

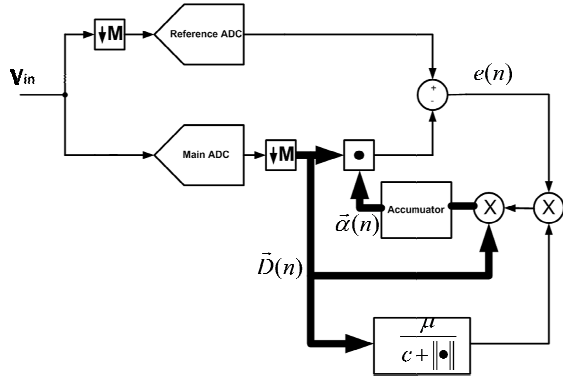
$$\text{where } \alpha(k) = \sum_{i=1}^k \frac{V_{ref}}{G(i)}$$

The 1st term in this equation (2) is the digital representation of the analog-input voltage V_i , and the 2nd term represents the quantization noise of the converter. The problem is how to continuously track $\alpha(k)$'s, given V_i (output of slow but accurate ADC) and $D(k)$'s are known. Fortunately, this problem can be solved by directly applying Adaptive Digital Filter theory. One solution is to use normalized LMS algorithm. We can rewrite the equations into a form similar to ADF:

$$e(n) = Vi(n) - \bar{\alpha}(n) \cdot \bar{D}(n)$$

$$\bar{\alpha}(n+1) = \bar{\alpha}(n) + \frac{\tilde{\mu}}{c + \|\bar{D}(n)\|} \cdot e(n) \cdot \bar{D}(n)$$

Where $\bar{\alpha}(n)$ is $[\alpha(1), \alpha(2), \alpha(3), \dots]$ at cycle n ; and $\bar{D}(n)$ is $[D(1), D(2), D(3), \dots]$ at cycle n ; c is arbitrary positive real constant to ensure the denominator cannot be 0; μ is adaptation constant. The system implementation of this calibration approach can be represented in *schematic 2*.



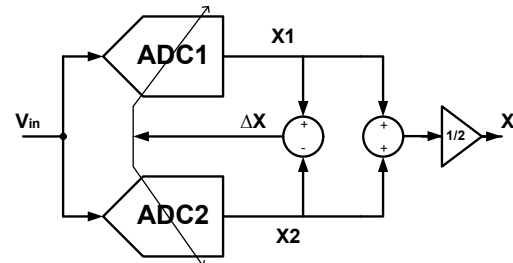
Schematic 2. Block Diagram for Reference ADC Approach

The greatest advantage of this approach is its conceptual simplicity. The reference ADC generates all information necessary to calibrate any errors (both linear and nonlinear) in main ADC, as long as the parameters associated with these errors are slow time varying compared to the sampling rate of reference ADC. It will be shown later that reference ADC approach easily expands itself for nonlinear gain error calibration.

However, it bears several potential problems. First, since the reference ADC runs at only a fraction rate of main ADC, the update of calibration parameters is performed at the rate of slow ADC, which leads to excess conversion

time. Since the reference ADC samples at fractional rate (i.e. $X1/M$) of main ADC, every M cycle, the reference ADC turns on which drastically changes input impedance of the sampling network. This can potentially cause harmonic distortion. Therefore, highly linear and fast front-end sample and hold circuit is added in front of both ADCs creating considerable power overhead.

(2) Split ADC Approach[2]



Schematic 3. Concept of Split ADC Approach

“Split ADC approach” is conceptually similar to using reference ADC approach. Instead of using slow but accurate ADC to calibrate main ADC, it splits one inaccurate ADC into two smaller ones (*Schematic 2*). Each smaller ADC is half in size and power of the original ADC. The outputs are taken as their average to keep thermal noise level unchanged, and the difference of smaller ADC outputs is used to calibrate gain errors. The concept of split ADC approach can be summarized as following.

The input to both ADC can be written as:

$$X_1 = \sum_{k=1}^N \alpha_1(k) \cdot D_1(k)$$

$$X_2 = \sum_{k=1}^N \alpha_2(k) \cdot D_2(k)$$

$$\text{where } \alpha_{1,2}(k) = \prod_{i=1}^k \frac{1}{G_{1,2}(k)^i [1 + \varepsilon_{1,2}(i)]}$$

$G_1(k), G_2(k)$ are correct stage gain's and $\varepsilon_1(k), \varepsilon_2(k)$ are gain errors of kth stage respectively to ADC1 and ADC2.

Suppose $\varepsilon_1(k), \varepsilon_2(k)$ are small, we can Taylor expand X_1 and X_2 and ignore all cross products of $\varepsilon_{1,2}(i), \varepsilon_{1,2}(j)$. Then, we have:

$$\alpha_{1,2}(k) = \left\{ 1 - \sum_{i=1}^k \varepsilon_{1,2}(i) \right\} \cdot \prod_{i=1}^k \frac{1}{G_{1,2}(k)^i}$$

Then, we can rewrite $X_{1,2}$ as:

$$X_1(k) = \sum_{k=1}^N f_1(k) \cdot D_1(k) - \sum_{k=1}^N g_1(k) \cdot \varepsilon_1(k)$$

$$X_2(k) = \sum_{k=1}^N f_2(k) \cdot D_2(k) - \sum_{k=1}^N g_2(k) \cdot \varepsilon_2(k)$$

$$\text{Where } f_{1,2}(k) = \prod_{i=1}^k \frac{1}{G_{1,2}(k)^i}$$

$$g_{1,2}(k) = \sum_{i=1}^{N-k+1} f_{1,2}(k) \cdot D_{1,2}(k)$$

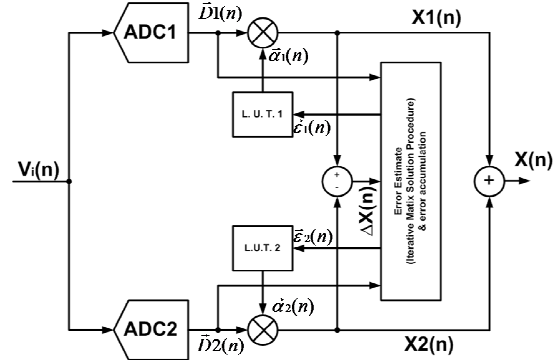
The first term in above equation is the correct digital value of the input, therefore they must be equal. Then,

$$\Delta X(k) = X_1(k) - X_2(k)$$

$$\Delta X(k) = \sum_{k=1}^N g_2(k) \cdot \varepsilon_2(k) - \sum_{k=1}^N g_1(k) \cdot \varepsilon_1(k) \quad (4)$$

From the equation (4), we can easily tell that $\Delta X = 0$, if both error terms are 0 or, both error terms are equal. To make sure the 2nd case does not happen, care must be taken to ensure $g_1(k)$ and $g_2(k)$ are not the same for all possible $D_1(k)$'s and $D_2(k)$. This can be accomplished by using different Sub-ADC thresholds for the 2 signal path [2]. To estimate $\varepsilon_1(k)$ and $\varepsilon_2(k)$, we ideally only need $2N$ iterations to create $2N \times 2N$ matrix in a noiseless environment. In practice, iterative matrix solution procedure is used to create estimates

for $\varepsilon_1(k)$ and $\varepsilon_2(k)$ over many more conversions to minimize the effect of noise. The detailed block diagram of split ADC approach is shown in *Schematic 4*.



Schematic 4. Block Diagram Implementation of Split ADC approach

The advantage of split ADC approach is minimum analog power overhead. Unlike reference ADC approach, it splits the ADC equally into 2 smaller ADC with half the power. In addition, since the 2 ADC's are symmetric, there is not potential distortion caused periodic change in input impedance like the previous case. Lastly, the calibration has much faster conversion rate because error parameters are updated at the same rate of sampling rate.

The main problem for split ADC is calibration robustness. When estimating gain error from difference of output signals, it relies on the gain errors being small. Consequently, the convergence is not guaranteed for large gain errors.

(3) Statistics based calibration [3]

Statistics bases calibration has a broad spectrum of approaches with different appearance. However, all techniques that falls into this category share a common trace: they try to extract gain errors by randomly alternating between 2 residue plots with the

same gain block. One of the representative works in this category is [1], which will be discussed here.

Unlike the previous 2 approaches, statistics based calibration cannot be easily formulated into mathematical representations. Here, an example of calibration of a single stage is discussed. However, it can be easily repeated to implement multistage calibration. To understand this approach, consider the first stage has gain error and the backend is ideal ADC with infinite resolution,

$$V_o = G_{actual} \cdot [V_{i, ana \log} - D \cdot V_{ref}]$$

When interpreting $V_{i, ana \log}$ in digital domain, we use the following equation

$$V_{i, digital} = \frac{V_o}{G_{ideal}} + D \cdot H$$

Where G_{ideal} is the ideal gain, and H is an adjustable parameter. We can rewrite the previous equation as following:

$$V_{i, digital} = \frac{G_{actual}}{G_{ideal}} \cdot V_{i, ana \log} + (H - \frac{G_{actual}}{G_{ideal}} \cdot V_{ref}) \cdot D \quad (5)$$

The 2nd term in equation (5) is discontinuity that needs to be eliminated. An obvious way is to make $H = \frac{G_{actual}}{G_{ideal}} \cdot V_{ref}$. The task is to measure and keep track of this quantity.

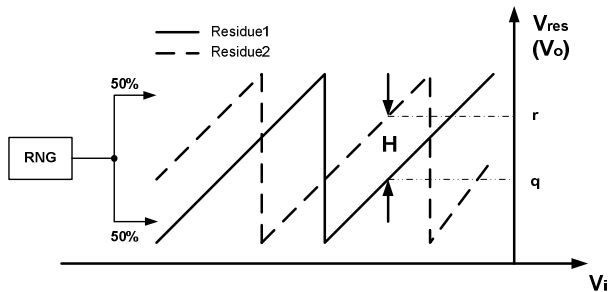
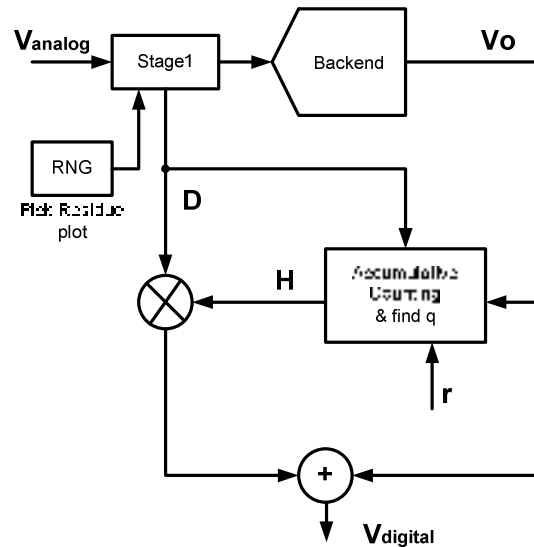


Figure 2. illustration of Statistics based calibration concept

To understand how to track H , consider the residue plot in Figure 2. Suppose the Random Noise Generator alternates randomly between the 2 residue plots with equal probability, and the input signal is uniformly distributed within the input range (statistically white), then the probability, also the accumulative count (CH) of backend results being q must be equal to being r . The difference in height between point q and r is exactly H . To find H , point q is chosen to be reference point, and accumulative counts are calculated around estimated points of r . The point r_0 with $CH(r_0)$ closest to $CH(q)$ is the closest approximation of r . The detailed block diagram implementation is shown in Schematic 5.



Schematic 5. Block Diagram implementation of Statistics based Calibration

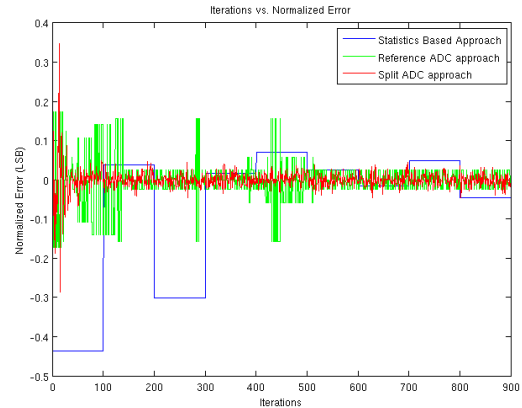
The main advantage for statistics based calibration is small analog power overhead, because it only requires extra comparators (which is not a limit on power) to create the 2nd residue plot. It trades off robustness with

digital processor power. The tolerance gain error is proportional to the number of accumulative counters around point r .

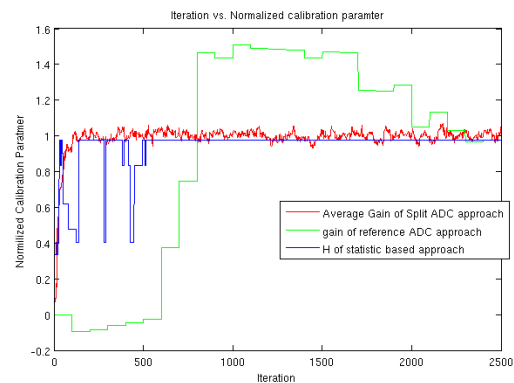
One potential problem with this approach is its reliance on the input signal amplitude being close to statistically white. Input signal amplitude has to have statistically sufficient count in the segment of residue plot that H is tracked. For example, this calibration approach does not work if the input is a constant value.

III. Simulation and Comparison

For simplicity, only gain error of the first stage is considered in Matlab simulation. Since the goal is to study the performance of calibration algorithm only, Ideal ADC with infinite resolution are used for the backend of ADC under calibration in “reference ADC” approach and “statistics based” approach. For fairness of comparison, 5b ADC with 100X smaller sampling rate are used for the reference ADC in “reference ADC” approach; 5b LSB spacing of counter bins are used in “statistics based” approach; each smaller ADC of “split ADC” approach is also 5b. 3 input stimulations are used to study the condition of convergence and convergence rate: uniformly distributed random input, sinusoidal input close to Nyquist rate, and constant input. The results are shown below. A gain error of 0.1 is used to compare convergence speed.



(a)



(b)

Figure 3. Convergence rate of difference approaches with white random input

The result of simulation with uniformly distributed random input signal is shown Figure 3. The gain error of 1.9 is used for this simulation. From figure 3(a), it is apparent that all three approaches converge to the point where normalized error is within LSB of 0.03, which is equivalent to a 5b resolution. We can also observe that the split ADC approach has a must higher convergence rate as expected. However, it is not clear from this simple simulation to differentiate convergence speed between reference ADC approach and statistics based approach.

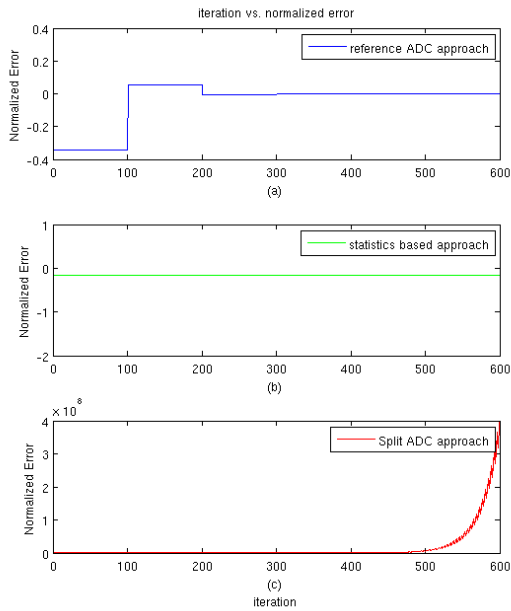


Figure 4. Normalized Error evolution When $V_{in}=-0.45V$

Figure 4 illustrates the calibration robustness under a constant input voltage. As shown in Figure 4(a), reference ADC approach still properly converge to, while statistics based calibration approach stopped working (Figure 4(b)), and calibration loop in split ADC (Figure 4(c)) approach breaks apart.

IV. Conclusion

In summary, the calibration approach with highly performance and lowest overhead cost in split ADC approach. However it is also the most prone to break convergence if the gain error is too large or the input does not meet its statistical condition. Reference ADC approach seems to be most robust technique of them all. Despite its power overhead and potential circuit level problems, the calibration loop works under all input signal condition. However, the preliminary study presented in this work only serves as a general guideline when choosing

proper calibration method. In practice, more detailed analysis is needed given the each case.

References

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