

Project Report

A 7bit 400Ms/s Flash ADC Without Frontend S/H

EE247

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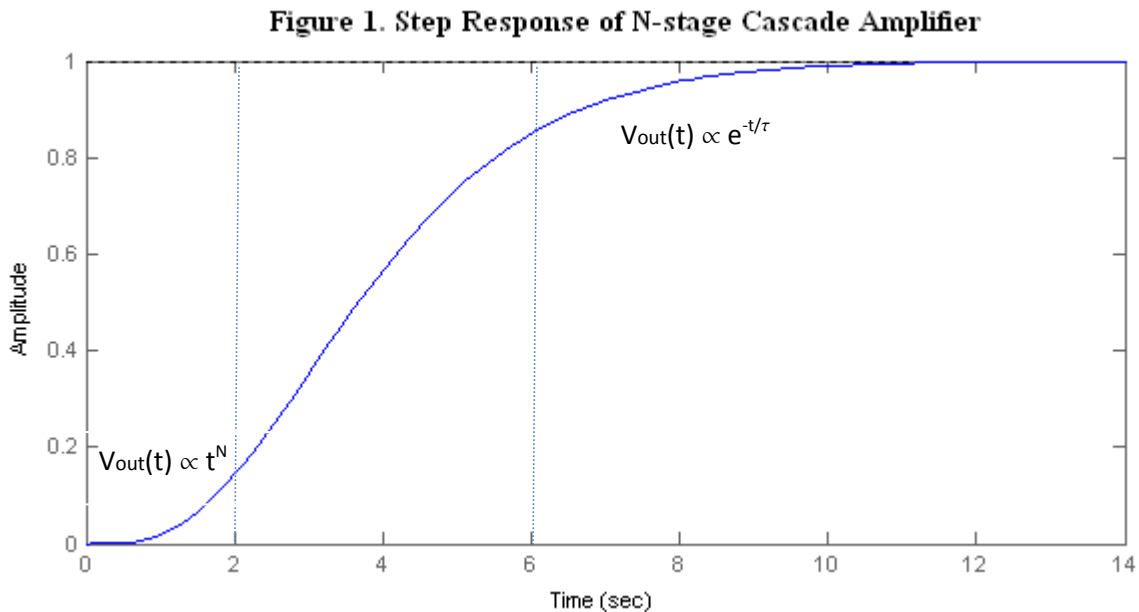
Introduction

Single step flash ADC's in the literature can be generally classified into 2 types: with and without frontend S/H circuit.

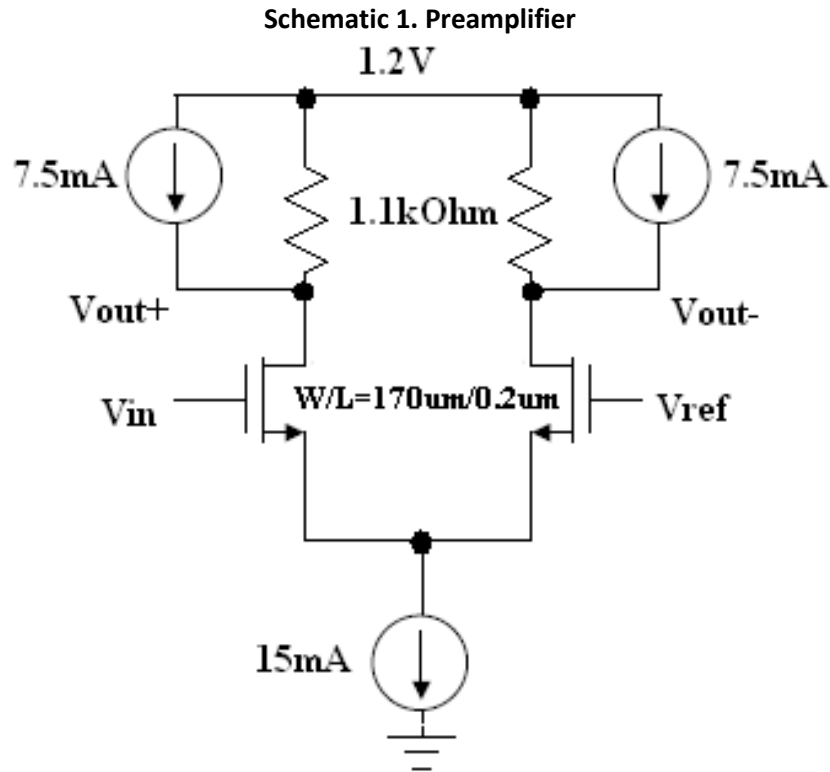
For flash ADC with frontend S/H, input voltage to each comparator stays constant during the entire comparing phase. The input signal each preamplifier "sees" is a perfect step. The preamplifier is followed by a latch and regenerative property of the latch will resolve the difference signal into digital 1's and 0's. The function of preamplifier is only to amplify its input signal larger than the latch offset. Therefore, the output of preamplifier does not have to settle by the time the latch makes the decision. The only requirement for the preamplifier is to have enough effective gain when the latch triggers. This greatly relaxes the bandwidth requirement of preamplifiers. In fact, in most designs with frontend S/H, preamplifiers are built cascade gain stages, and each stage acts as integrators as shown in Figure 1. The down side of this approach is requirement fast, accurate, and possibly low noise amplifiers for frontend S/H.

The 2nd approach is to design without a frontend S/H. In this case, each preamplifier has to continuously "track" the input signal. The large difference in delays across different preamplifiers results in error (or bubble) code. Furthermore, due to different changing rate of input signal that each preamplifier "sees", its delay is amplitude dependent. From reference [1], it is shown that this input dependent delay gives rise to 3rd distortion. In order to suppress this distortion, one has to make the preamplifiers fast enough, which is equivalent to have a large bandwidth. Therefore, the design without frontend S/H poses more stringent requirement on preamplifiers comparing to the one with frontend S/H.

At first glance, it is unclear which approach is advantageous for the given low voltage deep sub-miron technology. This work investigates 2nd approach, the one without frontend S/H. The conclusions are drawn based on the simulation. However, it is worth noting that none of the conclusions are definite without a thorough study of the 1st approach.



Preamplifier Design



(1) Distortion Consideration

Since the sampling frequency is 400Ms/s, it is very costly to build a frontend S/H at such high speed. Preamplifier has to continuously track input voltage. This leads to the requirement of high bandwidth preamplifier. From Reference [1], 3rd order harmonic distortion arises from input signal dependent preamplifier delay. In order to reduce this distortion component to meet SFDR of 7 ENOB at Nyquist rate, the bandwidth of the preamplifier is limited by maximum tolerable distortion.

$$SFDR = 20 \cdot \log\left(\frac{\frac{V_{r, out}}{A \cdot V_{FS}} \cdot \frac{f_b}{f_{in}} + 1}{2 \frac{f_b}{f_{in}}}\right)$$

Where f_b is preamp bandwidth, f_{in} is input signal frequency, $V_{r, out}$ is linear range of preamp input, V_{FS} is full swing input. Assume that $V_{r, out} = AV_{r, in}$, where A is the preamplifier gain, $V_{r, out}$ is preamplifier output swing. The above formula became:

$$SNDR = 20 \cdot \log\left(\frac{\frac{V_{r, out}}{A \cdot V_{FS}} \cdot \frac{f_b}{f_{in}} + 1}{2 \frac{f_b}{f_{in}}}\right)$$

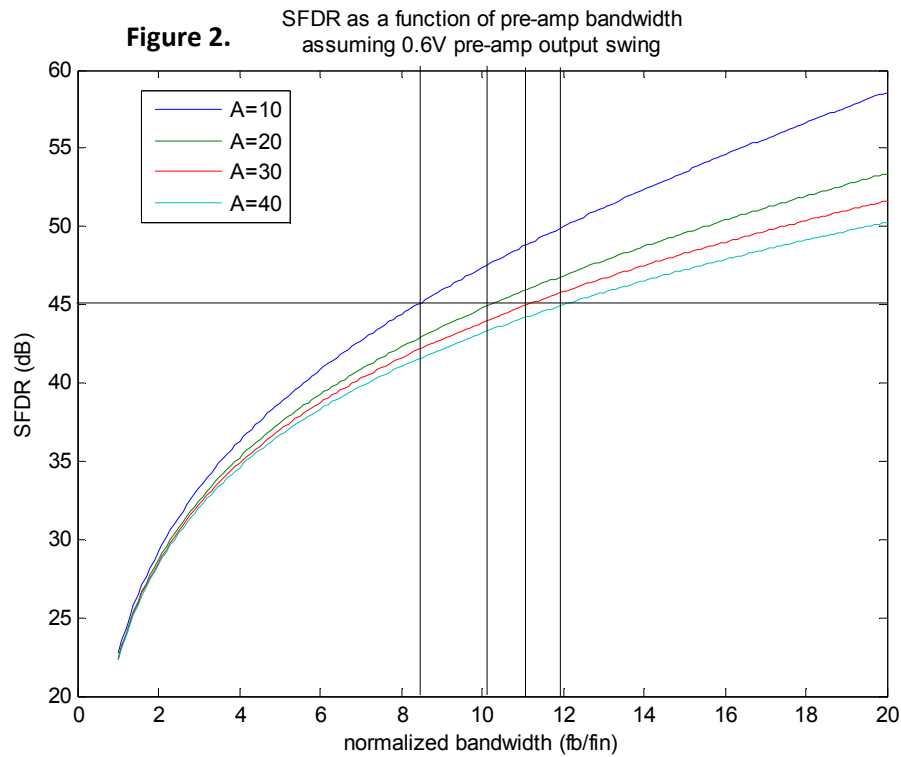
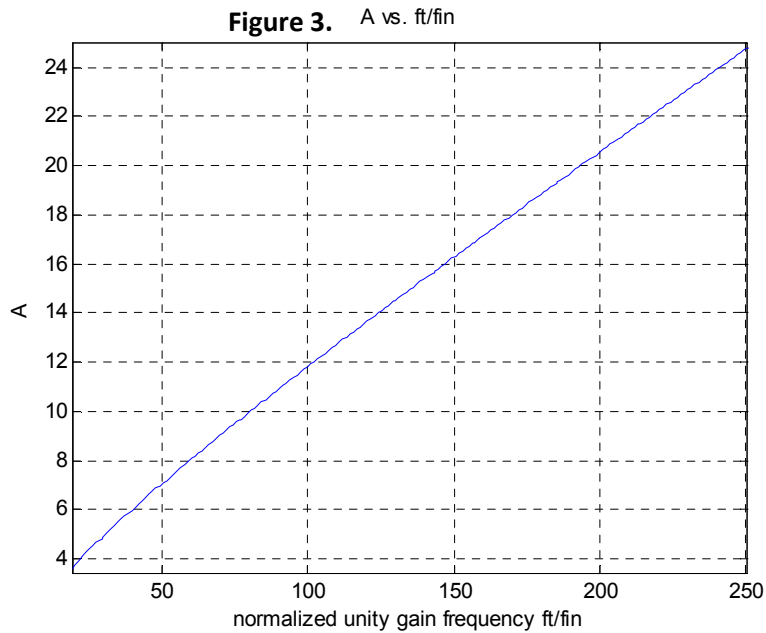


Figure 2. plots SFDR as a function of preamplifier bandwidth for different preamplifier gain, A . It is apparent that a low gain high bandwidth preamp is desirable. Single stage amplifier with resistive load is good fit for this requirement.

For ENOB of 7, SFDR > 44dB, the previous equation became:

$$44 = 20 \cdot \log\left(\frac{3\pi \cdot e^{\frac{0.6}{1.047A^2} \cdot \frac{f_i}{f_{in}} + 1}}{2} \cdot \frac{f_i}{Af_{in}}\right)$$

$$12.74 \cdot A = \frac{f_i}{f_{in}} e^{\frac{1}{1.745A^2} \cdot \frac{f_i}{f_{in}}}$$



The trade-off between A and ft is plotted in Figure 3. Lower A requires lower ft, and therefore lower power. In reality, however, lower A would increase Cg of the device due to offset requirement as shown in the next section, which consequently increase bias current to achieve the targeted ft.

(2) Offset Consideration

For a design of half LSB (4mV) accuracy, 3σ of total input referred offset has to be smaller than 4mV. Total contribution to input referred offset can be broken into preamplifier offset and latch offset. From schematic 1., the input referred offset can be calculated:

$$\sigma_{total}^2 = \sigma_{preamp}^2 + \sigma_{latch}^2 < \left(\frac{4mV}{3}\right)^2$$

$$\frac{(5mV)^2}{WL} + \left(\frac{50mV}{3}\right)^2 \frac{1}{A^2} < \left(\frac{4mV}{3}\right)^2$$

Substitute $WL = C_g / C_{ox}$, where Cg is total gate capacitance in triode mode, and $C_{ox} = 8.83 fF / \mu m^2$ extracted from simulation, the above equation becomes:

$$\left(\frac{4mV}{3}\right)^2 = 8.83 fF \frac{(5mV)^2}{C_g} + \left(\frac{50mV}{3}\right)^2 \frac{1}{A^2}$$

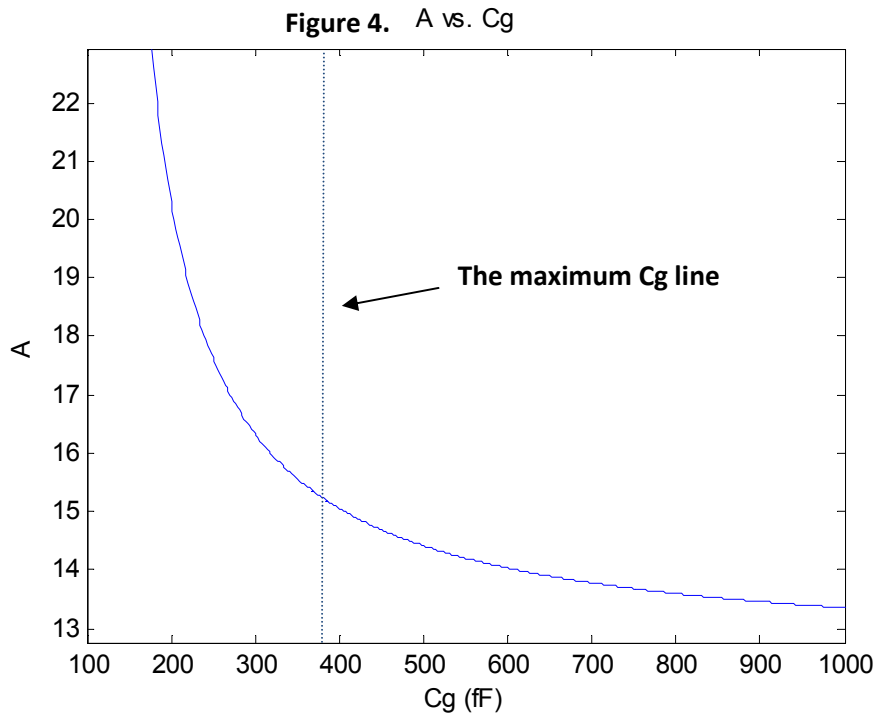


Figure 4. shows the trade-off between A and Cg. the larger input capacitance results in lower tolerable preamplifier gain. When Cg is very large, latch offset dominates in the overall offset. On the other hand, when Cg is very small, preamplifier offset becomes dominant. In addition, 50Ohm source impedance together with input capacitance forms a lower pass filter with the bandwidth of $\omega_{-3dB} = 1/(50Ohm \cdot C_{in}) = 2/(50 \cdot 128 \cdot \frac{2}{3} C_g)$. If the bandwidth of this low pass filter is lower than signal bandwidth (Nyquist frequency), the dynamic range of the system will be decreased due to attenuation of the filter. Therefore,

$$C_g < 2/(2\pi \cdot 200Mhz \cdot 50Ohm \cdot 128 \cdot \frac{2}{3}) = 373 fF \Rightarrow W < 224\mu m.$$

(3) Summary and Design Values

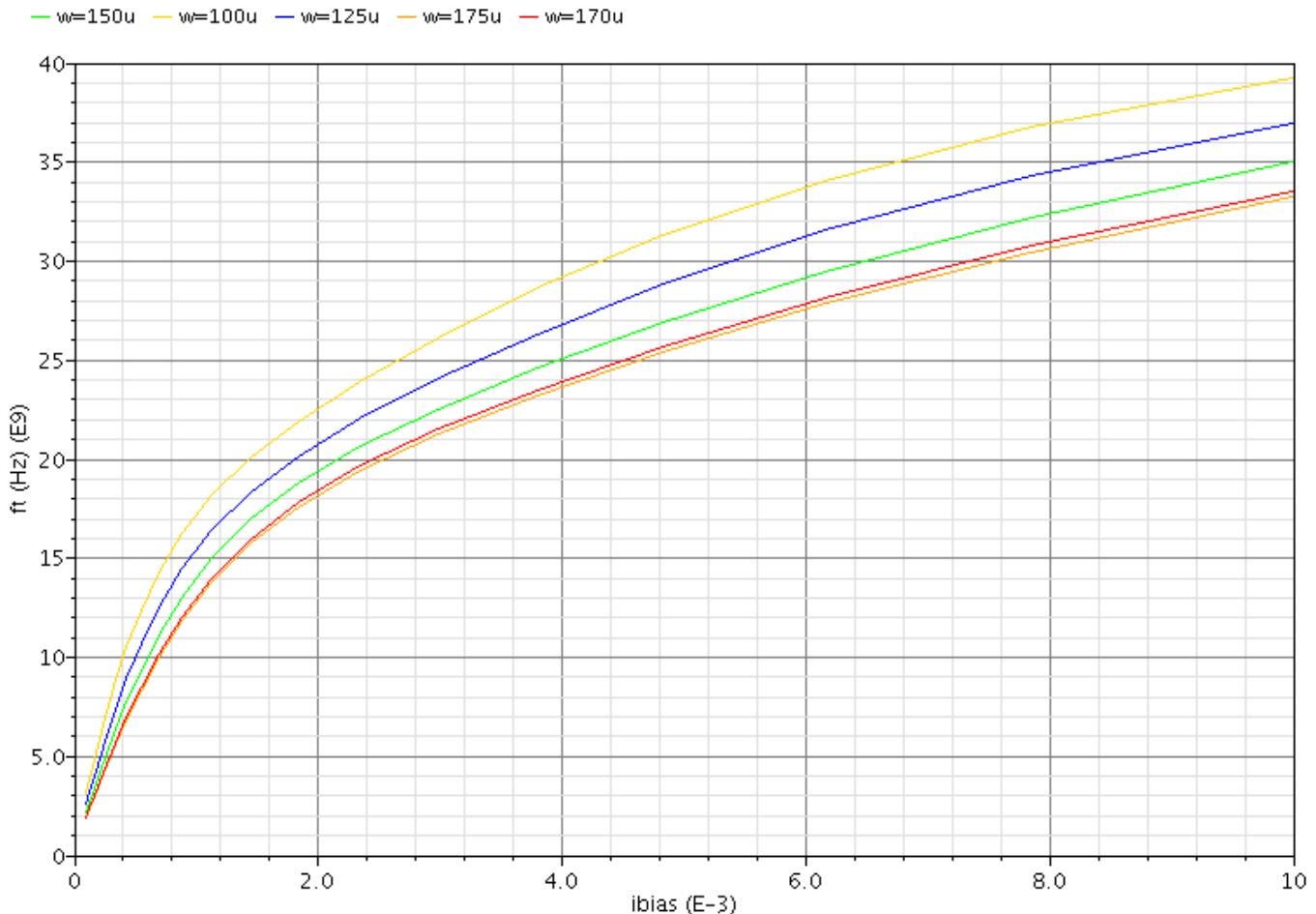
From figure 3. It is clear that the C_g value that optimal power is around the “knee” of the curve ($C_g=200fF\sim 373fF$), because in this region, C_g and A are strongly related. Large C_g would yield smaller required f_t , however, the bias current required to attain such f_t would become larger due to larger device size; while smaller C_g requires larger f_t , but the bias current is smaller because of the smaller device size. Figure 4. shows f_t as a function of bias current with different device width. Due to the complexity of the model, closed form formula of f_t as a function of I_{bias} and W can not be determined, which results an uneasy task for optimization. In order to optimize for power, the following process is used:

- (1) Pick a point around the “knee” in A vs. C_g curve (Figure 3.)
 - (2) Calculate W using $C_g=C_{ox}WL$
 - (3) Obtain f_t from f_t vs. A curve (Figure 2.)
 - (4) Obtain I_{bias} from f_t vs. I_{bias} curves (Figure 4.)
 - (5) Repeat the process for several nearby points on Figure 3., pick the one with lowest I_{bias}
- The final results are summarized in Table 1. Below:

Table 1. Calculation Results

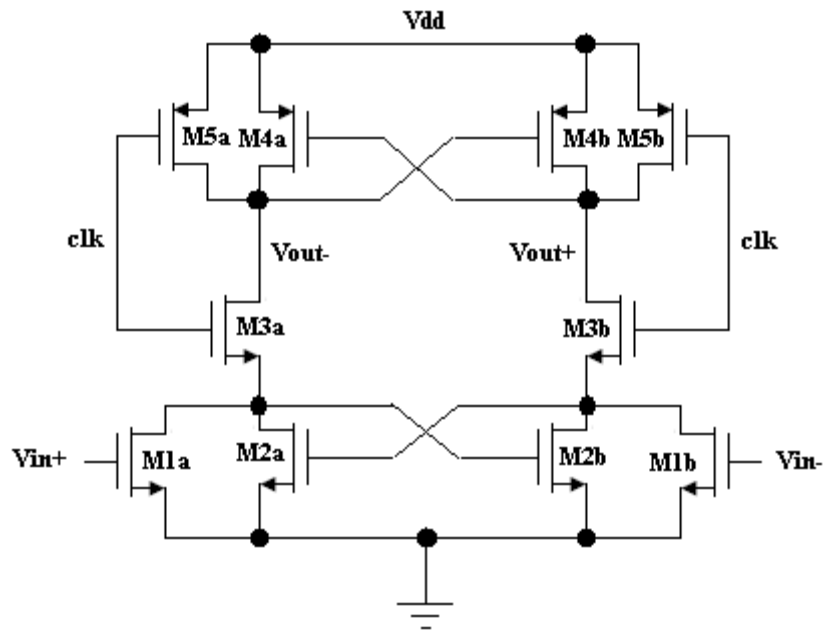
	Calculation Results	Chosen Value	Design Margin
W	-----	170 μm	-----
A	15.5	16	3%
f_t	29 GHz	30 GHz	3%
f_b	1.8125 GHz	1.875 GHz	3%
I_{bias}	7.5 mA	7.5 mA	0%

Figure 5. I_{bias} vs. f_t



Latch Design

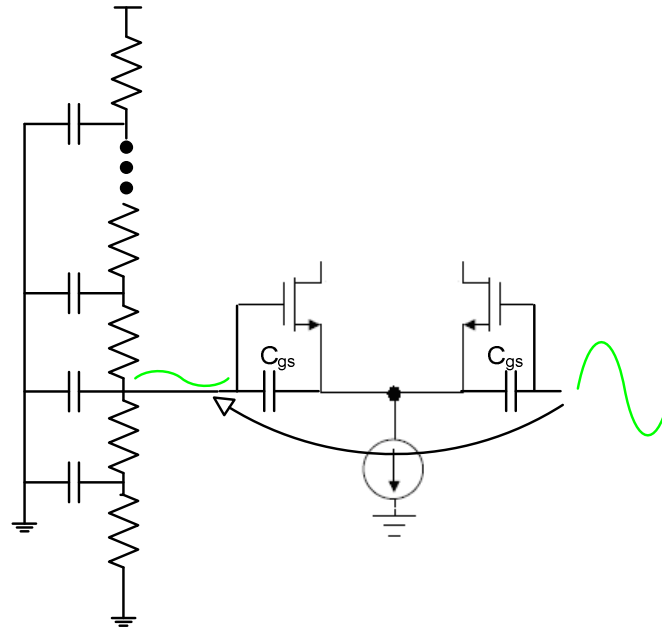
Schematic 2. Latch



Simple Yukawa Latch topology is chosen only because we are familiar with its operation. When clock is high, $M3$'s are in cut-off region, which breaks the regeneration loop; $M5$'s are in linear region, which brings the voltage at node V_{out+} and V_{out-} to V_{dd} , effectively sets the initial condition of the latch to its meta-stable state. When clock is low, $M5$'s are in cut-off region, which breaks the connection from output nodes to V_{dd} ; $M3$'s are in linear region, which closes the regeneration loop. $M1$'s act as input controlled shunt resistors to cause the latch to regenerate to its correct values. Sine offset of the latch is fixed to be 50mV, all NMOS devices are sized to be minimum (0.2um/0.13um) to reduce the load of preamplifiers. PMOS's are sized 3 times larger (0.6um/0.13um) to ensure the robustness of the latch over large common input range.

Resistor Ladder Design

Schematic 3. Resistor Ladder



An ideal reference would provide immovable reference voltages and would dissipate no power. In reality, the signal feedthrough from the input to the nodes of the reference ladder limits the total resistance, and therefore power dissipation, of the resistive ladder. If the power of the resistor ladder is significant compared to the overall power consumption of the converter, then large capacitors can be placed on the nodes of the reference ladder and the resistance can be increased to reduce the power. As the ladder resistance approaches infinite, the capacitance required to keep the feedthrough signal below 0.5LSB becomes 2^B times bigger than $C_{gs}/2$ (series combination of the two input devices).

From reference [2], the worst case feedthrough to the resistor ladder can be calculated based on the equation below:

$$\frac{1}{4} R_{ladder} C_{in, total} \cdot 2\pi \cdot f_{in} \cdot \frac{V_{FS}}{2} < \frac{LSB}{2}$$

$$R_{ladder} = 1.30\Omega$$

This results in significant power dissipation. To reduce power dissipation by the resistor ladder, we put capacitors on every node of the resistive ladder. This allows us to increase the total ladder resistance to 6.35kOhm, which makes its power dissipation negligible comparing to preamplifiers. We adjusted size each capacitor to 16.75pF after simulation order to keep the feedthrough level on the reference nodes below 4mV (0.5 LSB). The only purpose of this capacitor is to keep reference voltage at each resistor tap constant, its linearity does not affect the overall ADC performance. Therefore, the MOS oxide capacitors are used. Each capacitor only occupies an area of 0.00189mm². Table 2. Below summarizes the resistor and capacitor values

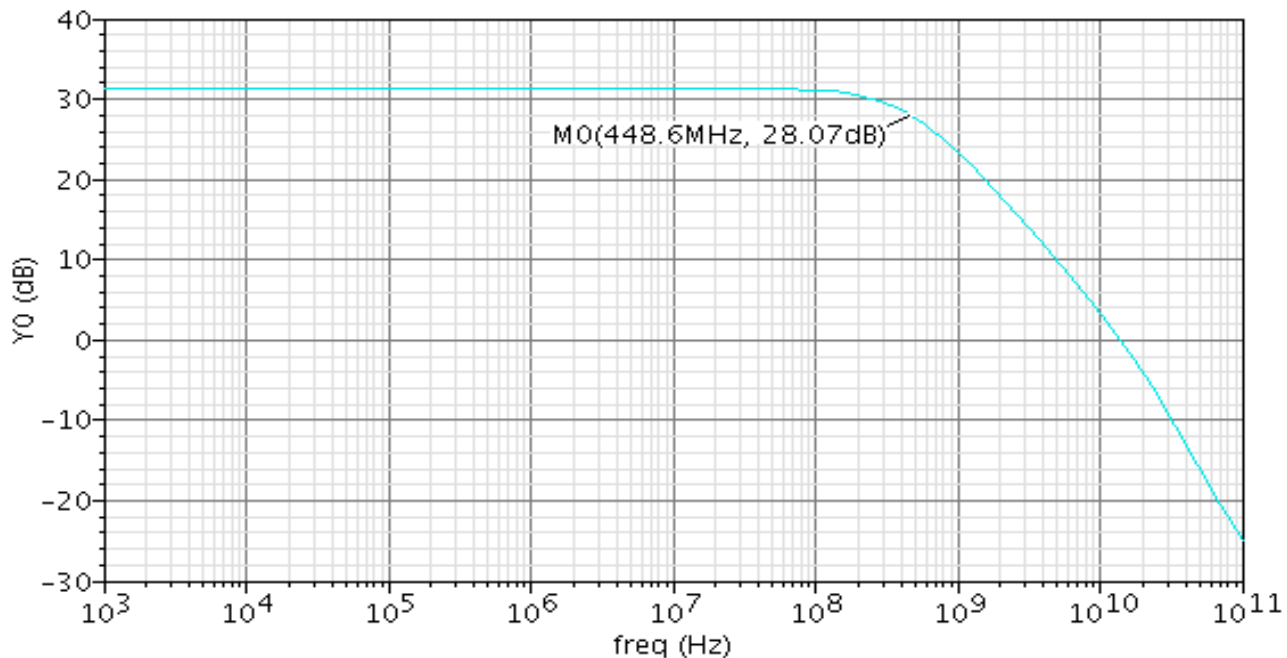
Table 2. Summary of Resistor and Capacitor Values

	Value	Area	Total Number	Total Area
unit size resistor	50 Ohm	0.0001 mm ²	127	0.0127 mm ²
unit size Capacitor	16.75 pF	0.00189 mm ²	126	0.238 mm ²

Simulation Results

(1) AC Response of Preamplifier

Figure 6. AC Response of Preamplifier



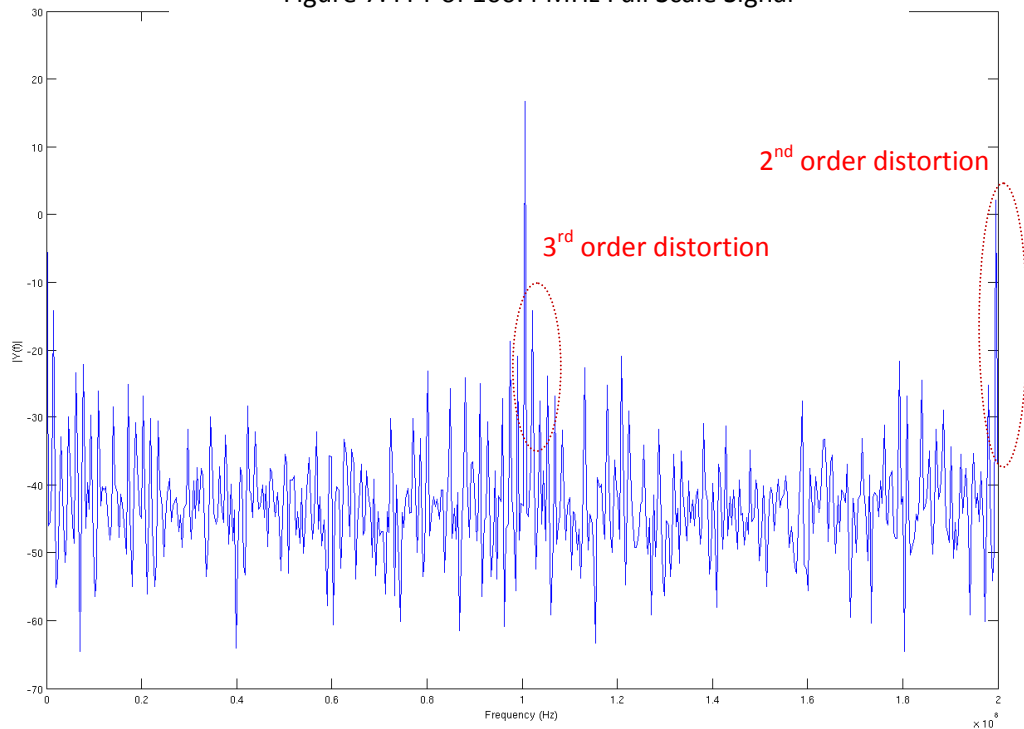
As shown in Figure 6., the DC gain of the simulated preamplifier is 35, and the bandwidth is only 448.6MHz. This result deviates largely from hand calculation, where the bandwidth should be 857MHz. Upon further investigation, it is nearly impossible to increase the bandwidth beyond 1 GHz for a single stage preamplifier. This is actually caused by a bug in model file. The PTM from 70nm to 180nm are developed for digital applications, and little attention is paid to analog behavior.

(2) FFT Test

We simulated the converter using only 4-bits. In order to see the full effect of the delay dependent distortion, the 4-bit converter was set to operate over the full input range of the 7-bit converter and a full-scale sine wave input was provided at 100.390625MHz. This frequency was chosen to produce 1024 unique data points using an integer number of input signal cycles (257).

Figure 7. below shows the results of a simulation with no offsets added. The folded back second and third harmonics can be clearly seen. The second harmonic is the limiting factor due to a flaw in our design. A fully-differential comparator architecture would likely get rid of the second harmonic. With the second harmonic the dynamic range was only 14.65dB; ignoring the second harmonic, the dynamic range was 30.9dB. Even without the second harmonic problem the dynamic range was lower than the targeted 44dB because we were unable to design an amplifier with the gain required by our calculation due to a problem with the model file.

Figure 7. FFT of 100.4 MHz Full Scale Signal



The distortion was measured again with 2.8 sigma and 5 sigma offsets added to four of the comparators. The dynamic range measurements for the three cases are listed below in Table 3. As shown in Figure 6. The 2nd order distortion limits the dynamic range. This 2nd order component is caused by nonlinear filter formed of nonlinear input capacitance and the 500ohm input impedance. This distortion can be easily eliminated by utilizing fully differential structure [2].

Table 3. Dynamic Range Measurements (limited by second order distortion)

Simulation	Dynamic Range
No Offset	14.6 dB
Without HD ₂	30.9 dB
4 x 2.8 Sigma Offset	14.6 dB
4 x 5 Sigma Offset	14.6 dB

The addition of offsets to the above simulations had little effect on the dynamic range because the above simulations had an LSB size of 64 mV and the comparators were to handle 3σ offset for an 8 mV LSB size.

Conclusion

Table 3. Estimated Performance of ADC

Sampling Frequency	400Ms/s
ENOB	2.13
ENOB without HD ₂	4.8
Power (preamplifier only)	2.3 W
Total Area	0.255 mm ²
Input Capacitance	20 pF

Table 3. summarizes the estimated performance of the ADC. Even without HD₂ term, the simulated ENOB is only 4.8, which is way lower than the target value of 7. This is mainly caused by the before mentioned “bug” in model file, which results in much smaller bandwidth of preamplifiers.

Suppose that there is no bug in the model file, and fully difference structure is used, and simulated ENOB is equal to 7, the power dissipation of such an ADC ($2 \times 2.3W = 4.6W$) is still too large comparing to reference [2] (0.6W with a ENOB of 6, and f_s of 1.3Gs/s). One of the reasons for such high power is the fixed latch offset given in the project. In reality, latches are sized accordingly to optimize the overall comparator power. Another reason is that it might not be a good approach to design the ADC without frontend S/H. At such a moderate speed and low resolution, flash ADC without frontend S/H might not be advantageous comparing to other approaches such as flash with frontend S/H and 2 step flash. Since thermal noise and opamp gain are not the dominant error source at this resolution, it is possible to build low power high speed frontend S/H circuit. Again, further investigations are needed to verify this point.

Reference

- [1] “CMOS integrated Analog-to-Digital and Digital-to-Analog Converters” Rudy Van de Plassche, Kluwe Academic Publishers
- [2] “A 1.8V 6-Bit 1.3GHz Flash ADC in 0.25-um CMOS” Koen Uyttenhove and Michiel S. J. Steyaert, IEEE Journal of Solid-state Circuits, Vol. 38, NO. 7, July 2003