RESPONSE SURFACE CHARACTERIZATION OF THE DEPOSITION OF LPCVD SiGe FOR SOLID-PHASE CRYSTALLIZED POLY-TFTS.

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INTRODUCTION

Thin film transistors (TFTs) find wide usage in active matrix liquid crystal displays (AMLCDs) [1]. Currently, most TFTs for display applications are fabricated using amorphous silicon as the active layer of the device [2]. The use of polycrystalline TFTs will enable the fabrication of high-resolution displays with integrated driver circuitry. This will result in a reduction in the overall cost of the display [3]. To fabricate poly-TFTs on large-area glass substrates, process temperatures must not exceed the glass strain point of 600°C for more that a short period of time, to avoid glass warpage. A minimization in overall thermal budget is also highly desirable. Silicon-germanium (SiGe) is an extremely promising material for use in poly-TFTs. SiGe has lower thermal budget requirements than comparable Si films, making its use advantageous in a low-temperature TFT process [4].

The active layer of poly-TFTs is usually deposited in the amorphous phase and subsequently crystallized to form smooth, large grain films. The properties of the crystallized films are critically dependent on the properties of the starting amorphous films [5]. Several crystallization processes are currently under study, including excimer laser crystallization [6] and low temperature solid phase crystallization (SPC) [7]. Excimer laser crystallization produces films of extremely high quality. Unfortunately, process throughput is extremely low, and uniformity is poor. Solid phase crystallization has a low throughput as well, but has excellent uniformity. Device performance is typically worse than that of laser crystallization. The SPC of SiGe will result in reduced thermal budgets and improved process throughput. Therefore, an SPC SiGe technology should enable the fabrication of low-cost large-area AMLCDs using poly-TFTs.

The SiGe deposition system, being binary in nature, is subtantially more complicated than the Si deposition system. A standard factorial design of experiments to characterize and optimize the process is impractical, given the large number of variables involved. In this work, we describe the use of statistical multifactorial techniques to reduce the size of the experiment, and report on optimization strategies developed using such a design. Based on results obtained from the aforementioned experiments, we present a response surface mapping of the system.

EXPERIMENTAL FORMULATION

Given the complex nature of the system, a two-step approach was used - an initial screening experiment was utilized to determine the parameters of primary interest, and a full response surface characterization of the effect of these parameters was performed to map the system. We have previously described the statistical formulation of the screening matrix [8]. A Plackett-Burman [9] design was used to determine major contrasts and interactions. Based on the results of the screening experiment, parameters in need of further study were identified. The screening experiment indicated that the parameters which appeared to have the maximum effect on device performance were deposition temperature, deposition pressure, and seed layer thickness. The first two parameters have already been identified as having a significant effect on the quality of deposited Si films. The third parameter, seed thickness, is unique to the deposition of SiGe. This pure Si under-layer is necessary to ensure smooth deposition of SiGe on SiO_2. The screening experiment used a wide window (10Å-100Å) to examine the effect of seed layer thickness on device performance. Results showed that the lower limit resulted in better performance. Therefore, the window was reduced in size, and characterized more fully. The window for deposition pressure was enlarged, as performance was expected to improve with increasing pressure. Using these definitions, an experimental design was prepared to enable determination of first and second order effects and interactions. The $Si_{0.8}Ge_{0.2}$ system was chosen as it provides a substantial reduction in thermal budget requirements over pure Si, without suffering from the alloy scattering effects, etc. of higher Ge fraction alloys . Data points were placed at various points along the axes and vertices. Multiple observations were made at every measurement point to estimate and correct for system noise. The design is shown in figure 1. Measurement points and measurement ranges are clearly marked.

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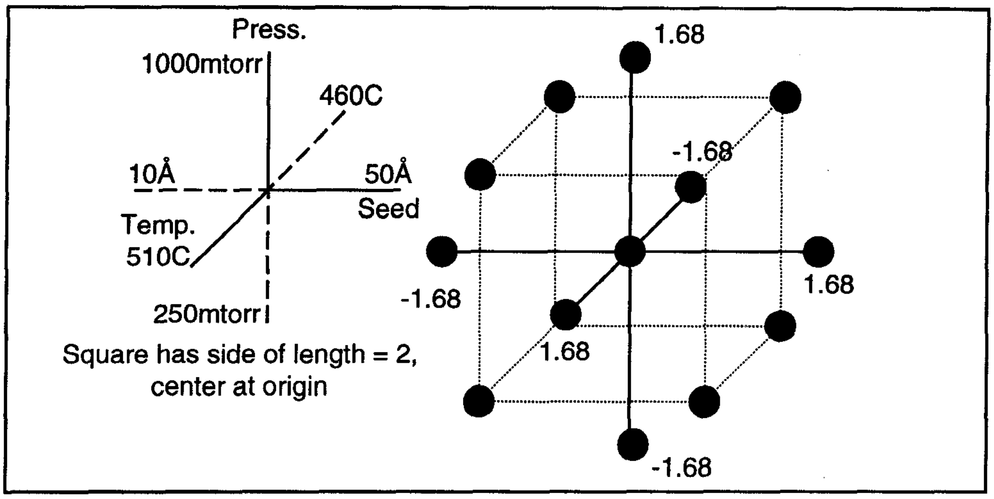


Figure 1: Experimental design showing measurement points and parameter ranges.

EXPERIMENTAL DETAILS

Using the above experimental definition, amorphous SiGe films were deposited on oxidized silicon wafers. The films were crystallized at 600°C. All films crystallized in less than 24hrs. The films were then patterned. 1000Å LPCVD (from SiH_4 and O_2) SiO_2 was deposited at 450°C for use as a gate dielectric. This was followed by a 2500Å $Si_{0.6}Ge_{0.4}$ gate electrode. Gates were defined and the wafers were implanted as appropriate. After dopant activation, devices were passivated with 4000Å SiO_2 and contacts were defined. Metallization was done using 1μm Al. Maximum process temperature was 600°C. The devices were then plasma hydrogenated, and electrical measurements were performed.

RESULTS AND DISCUSSION

From the electrical measurements, various device parameters were extracted. These were field-effect mobility (μ_{FE}), threshold voltage (V_T), sub-threshold slope (sts) and leakage current (I_{MIN}). All device parameters showed variation with deposition conditions. The effects of individual deposition parameters were extracted. The individual dependencies for PMOS are shown below, in figures 2 through 5.

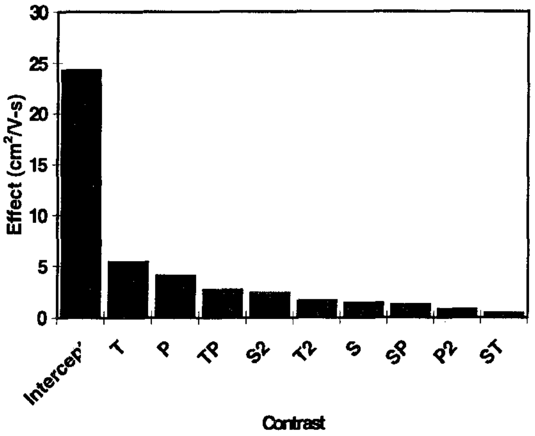


Figure 2: PMOS Field-effect mobility(μ $_{FE}$) contrasts

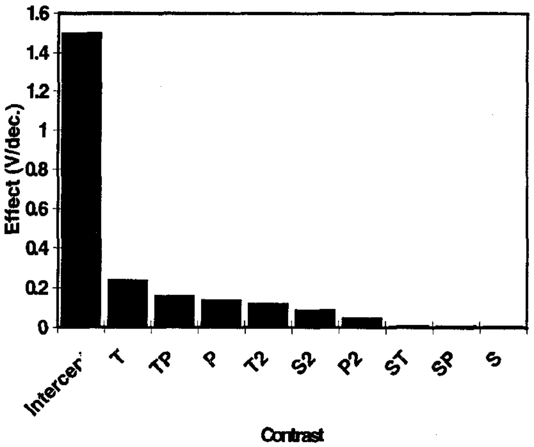


Figure 3: PMOS Sub-threshold slope (sts) contrasts

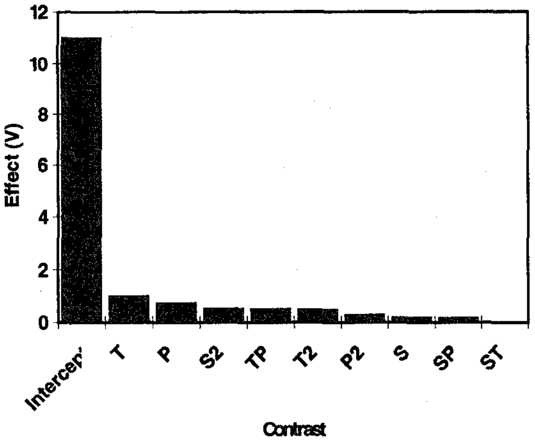


Figure 4: PMOS Threshold voltage (V_T) contrasts

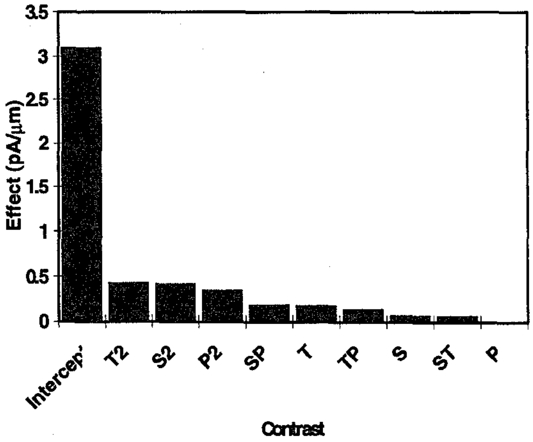
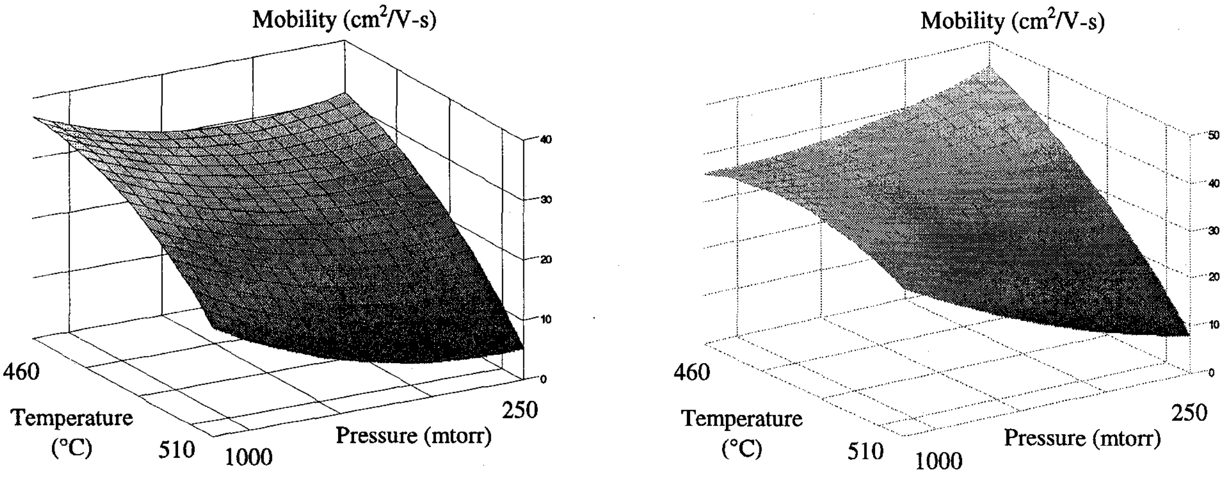


Figure 5: PMOS Leakage current (I_{MIN}) contrasts

From the above graphs, the effects of the individual process parameters are clearly visible. Field-effect mobility shows a substantial dependence on process parameters. The other parameters show a smaller and less definite dependence. This is due to the fact that the TFTs usually exhibit a slow turn-on, unlike single crystal devices. This makes extraction of the sub-threshold slope and threshold voltage difficult, complicating analysis. Leakage current is within the noise range of the experiment, making conclusions about contrasts difficult. The determined contrasts were used to generate surface maps of the various parameters. Clearly, temperature and pressure have the greatest effect on device mobility. Seed layer thickness was found to have little effect on device mobility within the range of thicknesses used. The variations in PMOS and NMOS mobility vs. the dominant parameters are shown below, in figures 6(a) and 6(b).



(a)

(b)

Figure 6: Variation in field effect mobility for (a) NMOS and (b) PMOS devices vs. temperature and pressure.

To test the accuracy of the maps above, spot confirmation experiments were performed near the vertices and off-center. These were compared with the predicted values to estimate model accuracy:

- Numerical accuracy is good near the center of the ranges.
- The model provides excellent trend prediction ability throughout the range of analysis.
- Numerical accuracy deteriorates at the edges of the analysis range.

Further improvement in model accuracy can be obtained by increasing the number of measurement points and using more sophisticated models which include non-linear and non-quadratic effects.

OPTIMIZATION STRATEGIES

A key result of this analysis has been the development of optimization strategies to maximize device performance. The following trends are apparent from the mobility maps above:

- performance improves with increasing pressure at intermediate and high temperatures
- performance saturates or degrades with increasing pressure at low temperatures
- performance improves with decreasing temperatures

These suggest a clear optimization strategy - increase pressure and decrease temperature to locate the optimal deposition conditions. Interestingly, performance improvement with increasing pressure is not saturated for intermediate and high temperatures, and an extension in the analysis range may result in further improvements in performance.

CONCLUSIONS

A multifactorial design of experiments has been used to realize a response surface characterization of the deposition of SiGe for poly-TFTs. Devices have been fabricated demonstrated the best performance achieved to date using a comparable SiGe technology. Optimization strategies have been developed to further improve performance. These should enable the fabrication of high-performance SiGe TFTs for a large-area AMLCD technology.

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