Novel 3-D Structures

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Interconnect delays are increasingly dominating IC performance due to increases in chip size and reduction in the minimum feature size. In spite of new materials like Cu with low-k dielectric interconnect delay is expected to be substantial below 130 nm technology node, thereby severely limiting chip performance [1]. Therefore, the need exists for alternative technologies to overcome this problem. One such promising technique is three-dimensional ICs with multiple active Si layers. In a 3-D structure a large number of information signal paths could be transferred from horizontal to vertical interconnects. 3-D integration of devices in multiple layers of Si (schematically shown in Fig. 1) obtainable through technologies like crystallization of amorphous Si [2, 3] and wafer bonding [4], can potentially reduce chip area through increasing transistor packing density and reducing wiring requirements for wire-pitch limited ICs.

Recently we have estimated chip area for 3D ICs and demonstrated significant reductions in interconnect delay. For a 0.18μm technology chip with 8 million gates [5]. In this work we generalize this analysis using NTRS technology projections down to 50 nm node. The performance analysis incorporates the effects of increasing the number of active layers, moving repeaters from the substrate to upper active layers and optimizing wiring networks. Interconnect delay as a function of technology is calculated (Fig. 2) using data projected by the NTRS for 2-D ICs. Also shown are delays for 3-D ICs with 2 active layers, where wire pitches are increased to match the 2-D IC areas, calculated using the 3-D chip area estimation model described above. Interconnect delay is reduced by 64% as a result. In all these calculations the number of metal layers is conserved between 2-D and 3-D ICs. This assumption can be relaxed such that each active layer in 3-D ICs may have its own associated lower metal tiers with a universal global tier responsible for connecting the active-layer networks. The total number of metal layers is thus increased in this 3-D case. The resulting delays are also shown in Fig. 2. At 50 nm node the delay improvement is an additional 35%. Repeaters used in ICs occupy a significant fraction of chip area and it is seen to increase significantly with scaling as more repeaters are required for large area chips. Such repeaters can be removed from the substrate and placed on upper active Si layers using an appropriate 3-D technology [3]. The area freed up on the substrate can be used for chip area compaction. At 50 nm node the additional reduction in interconnect delay due to this area compaction is approximately 9% (Fig. 2).

In 3D ICs can we get by with TFTs in poly-Si or do we really need single crystal TFTs? To answer this question a new model to connect statistical grain size variation to performance variation in polycrystalline TFTs has been developed [6].The model predicts an increase in device variation as the device and grain sizes converge (Fig. 3). The increase in variation is due to the increased spread in average grain size in such devices, which in turn is due to the random nucleation and growth of the grains. But what happens if grain growth is not random, so that the grain size is always known to have a fixed value for all transistors on a substrate? This model would predict no variation in device performance due to grain size variation. Hence, non-random grain growth would seem to be a promising technique for improving device-to-device uniformity.

There are at least two approaches which have been suggested to obtain non-random grain growth. The first are laser based techniques, such as sequential lateral solidification. However, grain boundaries may still result on a statistical basis. In the second technique a seeding agent, such as germanium [2] or nickel [3] is used to precisely nucleate the grains in amorphous Si films. Low temperature is used for seeding to avoid self nucleation. Solid phase crystallization is then done under conditions to laterally grow the grain with minimal self nucleation (Fig. 4). Using this technique single grain Si islands can be achieved suitable for CMOS device fabrication. Dopant incorporated in amorphous silicon has been shown to be fully activated during crystallization at temperatures as low as 450°C. The process has been used to fabricate high performance 0.1μm CMOS TFTs with high mobilit*y, low leakage and high on/off ratio suitable for 3-D integration applications. Fig. 5 shows an example of I-V characteristics of a Ge seeded single grain NMOS TFT. Also shown are poly-Si TFTs with grain boundaries with deteriorated performance. This process is fully CMOS compatible and has a low thermal budget. It is highly scalable to deep-submicron technologies and, with suitable optimization, should enable the production of high performance, high density, vertically integrated 3-D ULSI.

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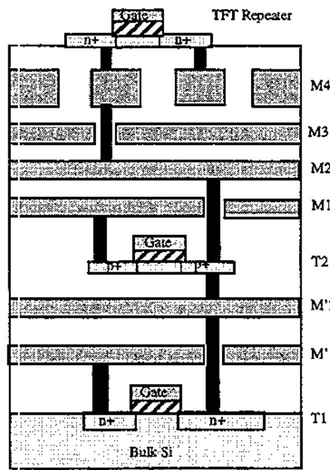

Figure 1. Schematic representation of 3D integration with multilevel wiring network

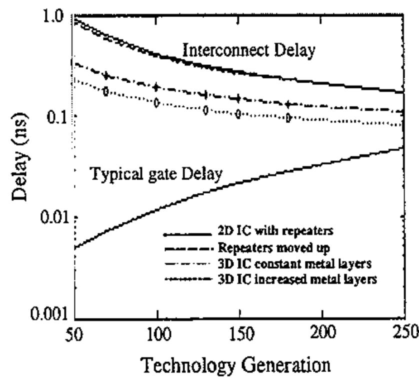

Fig. 2. Interconnect and device delay as a function of technology scaling. Moving repeaters to upper active tiers reduces interconnect delay by 9%. 3D (2 active layers) shows significant delay reduction (64%). Increasing the number of metal levels in 3D reduces interconnect delay by a further 35%.

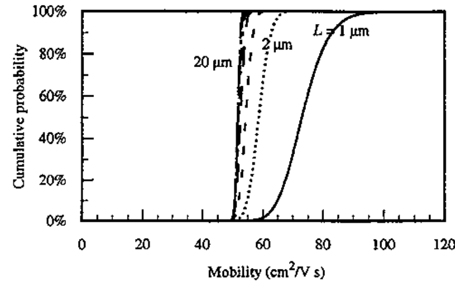

Fig. 3: Cumulative distribution for poly-Si TFT mobility; with avarage grain size of 0.1 µm, [6]

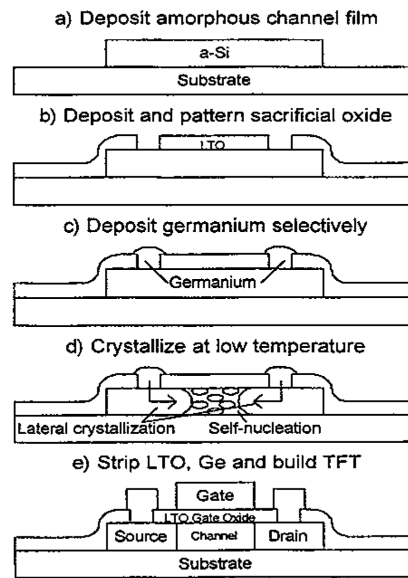

Fig. 4. Process flow for Ge-seeded laterally crystallized TFT fabrication

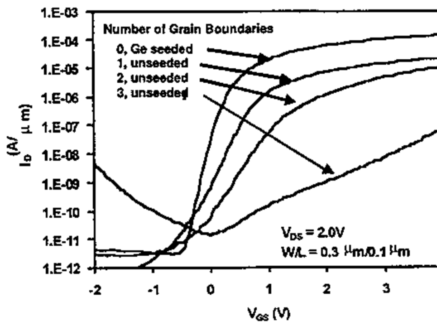

Fig. 5. Variation in electrical performance of NMOS TFT's with presence of grain-boundaries. Also shown is a Ge seeded single grain transistor.