

Laterally Crystallized Polysilicon TFTs Using Patterned Light Absorption Masks

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Introduction

The channel of polysilicon thin film transistors (TFTs) is commonly formed by crystallizing amorphous silicon (α -Si) using low temperature solid-phase crystallization (LT-SPC). This occurs through nucleation and subsequent grain growth. Nucleation has a higher activation energy than grain growth. Large grains can be achieved by maximizing the grain-growth to nucleation ratio. We demonstrate a new method of fabricating laterally-crystallized TFTs using patterned light absorption masks. These are used to locally nucleate films in specified locations through increased local heating. Subsequently, the grains are grown laterally.

Lateral crystallization is a promising means of achieving single-grain devices. Unfortunately, most seeding agents such as metals [1] degrade device performance. The technique described here is simple and entirely non-contact, making it promising for the fabrication of single-grain devices.

Device Fabrication

100nm α -Si was deposited on fused-silica substrates, followed by 20nm SiO₂ (etch stop) and 300nm α -Si (masking layer). This was patterned to form islands over the TFT drains. An acoustic temperature / crystallinity sensor [2] previously showed that unmasked wafers crystallized in 380 seconds during RTA (substrate temperature of 850°C), while wafers with an unpatterned masking layer crystallized in 75 seconds (approximately the same substrate temperature, due to vertical gradient). Wafers were annealed using RTA for 300 seconds to nucleate the channel films under the mask and then crystallized at 500°C. The over-layers were removed and TFTs were fabricated using a low-temperature ($\leq 600^\circ\text{C}$) top-gate process. This is shown in figure 1. Control devices were fabricated using standard LT-SPC only.

Results and Discussion

Seeded device perform better than control devices. The improvement increases for small devices, as shown in figures 2 and 3. Results are summarized in table I. The variation in improvement with device size is shown in figures 4 and 5. As the laterally-crystallized region becomes a larger fraction of the device, performance improves dramatically. These low-temperature devices are useful for large-area electronics. A high-temperature process should result in high-performance devices for 3-D integrated VLSI and SOI applications.

Heating of the silica wafers during RTA is inefficient due to the poor light absorption by the thin Si, and due to heat loss to the surroundings. The masks increase local heating efficiency, and a temperature gradient develops from the drain outwards. Hence, nucleation occurs first in the drain, and grains grow laterally into the channel. The extent of lateral crystallization is a function of the temperature gradient, and can be increased by optimizing the heating profile. This should enable the fabrication of single-grain devices.

Conclusions

We present a novel technique to fabricate laterally-crystallized TFTs. Thick Si is placed over the drain of the TFT. This is then subjected to an RTA step to nucleate the film in the drain region, and then to an LT-SPC grain-growth step. This results in a substantial device performance improvement. The simplicity and non-contact nature of this technique makes it promising for the fabrication of high-performance TFTs. Optimization, and the use of a high temperature process, should enable near single-crystal performance using a simple, low-cost process.

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References

- [1] S.-W. Lee and S.-K. Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization", *IEEE Electron Device Letters*, vol. 17, no. 4, pp. 160-2, 1996.
- [2] V. Subramanian, L. Degertekin, P. Dankoski, B. T. Khuri-Yakub, and K. C. Saraswat, "A Novel Technique for In-Situ Monitoring of Crystallinity and Temperature during Rapid Thermal Annealing of Thin Si/Si-Ge on Quartz/Glass", presented at Flat Panel Display Materials II, MRS Symposium, San Francisco, CA Spring 1996.

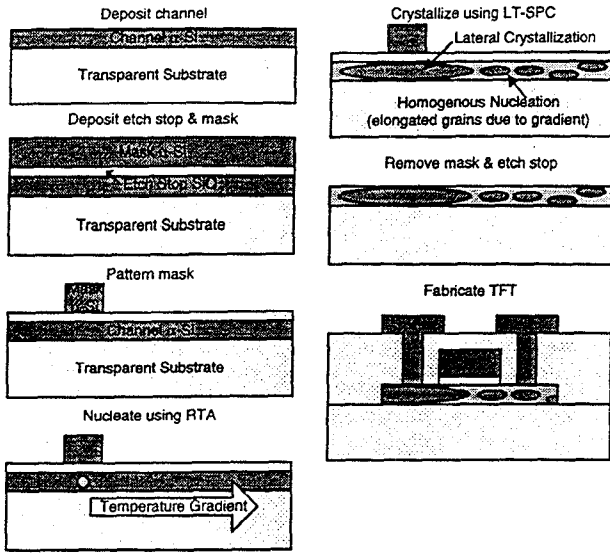


Figure 1: Process flow and final device structure

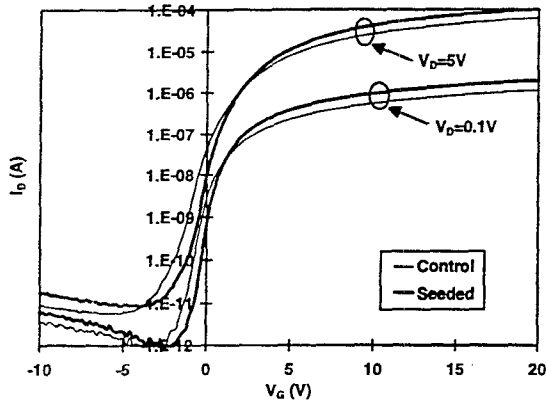


Figure 2: NMOS I-V characteristics (W/L=2μm/2μm)

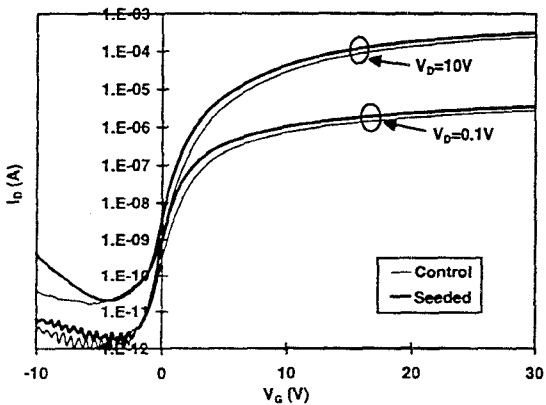


Figure 3: NMOS I-V characteristics (W/L=20μm/20μm)

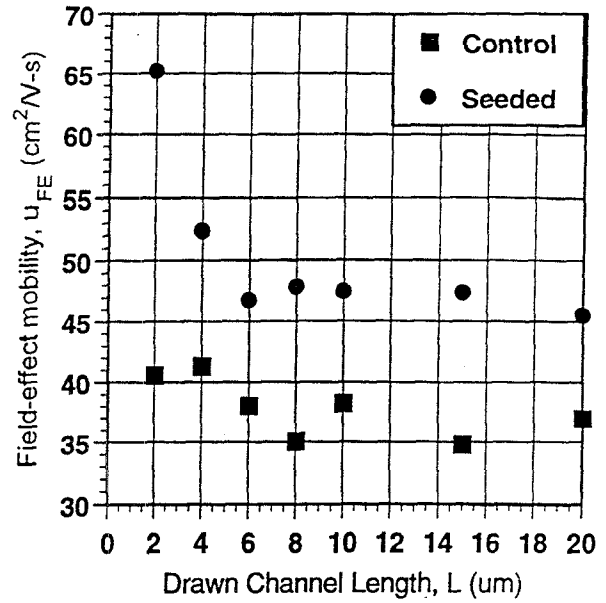


Figure 4: Mobility vs. L (W=1μm)

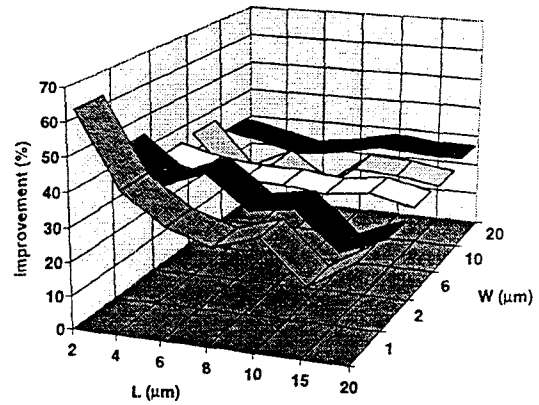


Figure 5: Variation in improvement with device size

Table I: Summary of Device Characteristics (W/L=2μm/2μm)

Parameter	NMOS		PMOS	
	Control	Seeded	Control	Seeded
μ_{FE} (cm ² /V-s)	41	65	15	24
I_{MIN} (pA)	6	8	-8	-6
sts (V/dec.)	0.64	0.49	-1.0	-0.77